AS3709

µPMIC with 5 DCDC and 2 LDOs

General Description

The AS3709 is an ultra compact µPMIC containing 5 high-efficiency, constant-frequency synchronous buck converters in addition with two universal IO LDOs are available for lower current power rails. The wide input voltage range (2.7V to 5.5V), automatic power-save mode and minimal external component requirements make the AS3709 perfect for any single Li-Ion battery-powered or fixed 3.3V/5V supply application. Typical supply current with no load is 110µA and decreases to ≤ 7µA in shutdown mode. An internal synchronous switch increases efficiency and eliminates the need for an external Schottky diode. The internally fixed switching frequency (2MHz, 3MHz or 4MHz) allows the use of small surface mount external components. Very low output voltages can be delivered with the internal 0.6V feedback reference voltage. The AS3709 is available in a 32-pin QFN 4x4mm package and in a very compact CSP36 with 0.4mm pitch.

For further understanding in regards to the contents of the datasheet, please refer to the Reference Guide located at the end of the document.

Key Benefits & Features

The benefits and features of AS3709, µPMIC with 5 DCDC and 2 LDOs are listed below:

Figure 1:
Added Value of using AS3709

Benefits	Features
Compact design due to small coils for IO and memory voltage generation	5 DCDC step down regulators (2-4MHz)
Independent voltage rails for general purpose IO supplies	2 universal IO LDOs
Flexible and fast adaptation to different processors/applications	OTP programmable Boot and Power-down sequence
Power saving control according to the processor's needs.	Stand-by function with programmable sequence and voltages
Self-contained start-up and control for single-cell battery applications. Safety shutdown feature.	Control Interface I^2C/SPI control lines ON key with 4/8s emergency shut-down POR with RESET I/O
Dedicated packages for specific applications. Optimization for PCB cost or size.	32-pin QFN (4x4mm), 0.4mm pitch 36-ball WL-CSP 0.4mm pitch

Applications

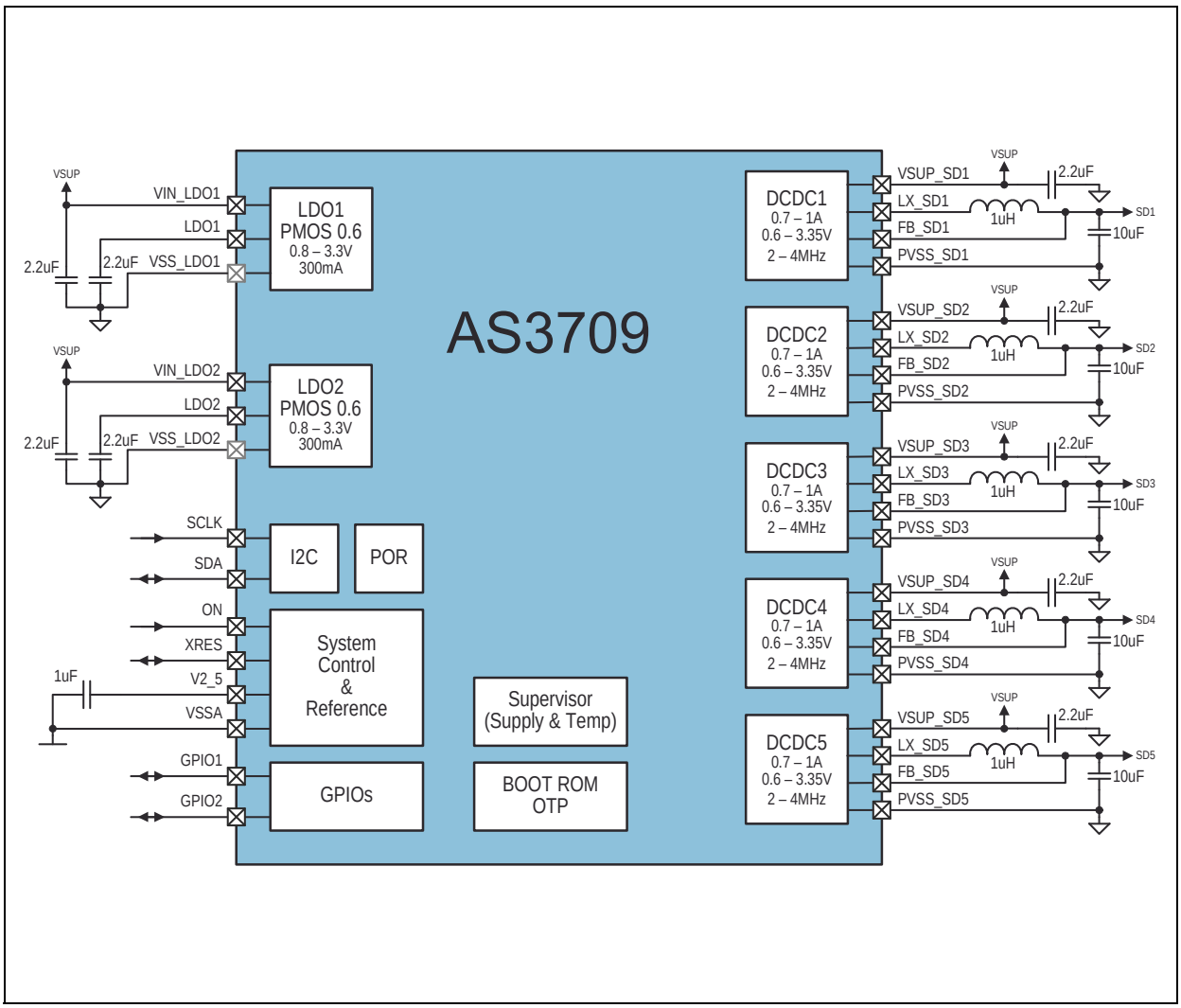
The device is ideal for:

- SSDs, mobile communication devices
- Laptops and PDAs
- Ultra-low-power systems
- Medical instruments or any other space-limited application with low power-consumption requirements.

Block Diagram

The functional blocks of this device for reference are shown below:

Figure 2:
AS3709 Block Diagram



Pin Assignment

The AS3709 pin assignments are described below.

Ball Assignments: Shows the top view ball assignment of the AS3709 WL-CSP.

Figure 3:
36 balls WL-CSP with 0.4mm Pitch

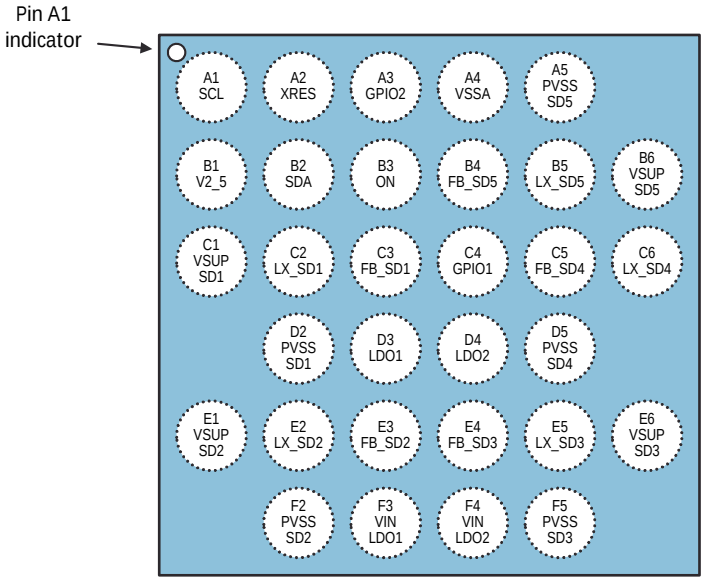


Figure 4:
32 pins QFN 4x4 with 0.4mm Pitch

Pin Assignment: Shows the top view pin assignment of the AS3709 QFN package.

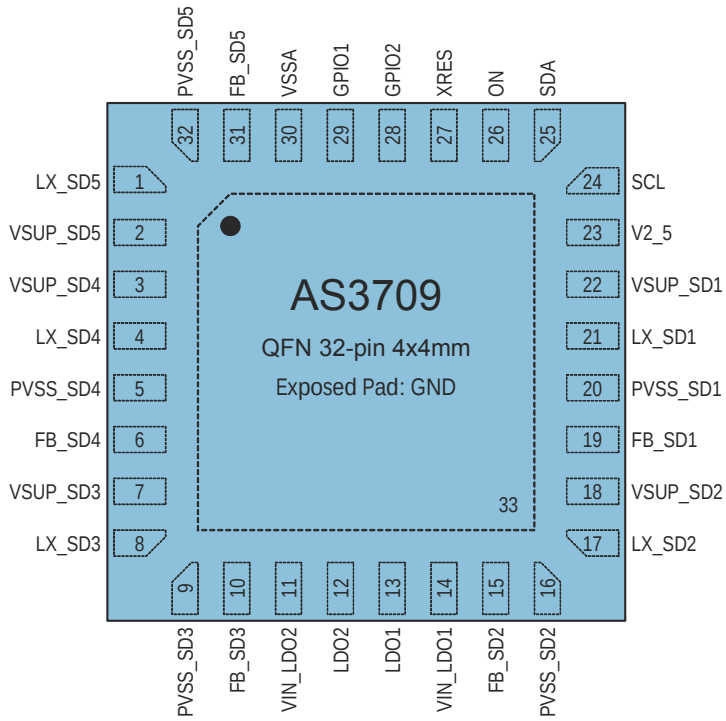


Figure 5:
Pin Description

Pin Number		Pin Name	Pin Type	Description	If not Used
QFN	WLP				
1	B5	LX_SD5	DIG OUT	DCDC SD5 switch output to coil	Open
2	B6	VSUP_SD5	SUP IN	DCDC SD5 pos supply terminal	Always needed
3	B6	VSUP_SD4	SUP IN	DCDC SD4 pos supply terminal	Always needed
4	C6	LX_SD4	DIG OUT	DCDC SD4 switch output to coil	Open
5	D5	PVSS_SD4	GND	DCDC SD4 neg supply terminal	Always needed
6	C5	FB_SD4	ANA IN	DCDC SD4 Feedback pin	Open
7	E6	VSUP_SD3	SUP IN	DCDC SD3 pos supply terminal	Always needed
8	E5	LX_SD3	DIG OUT	DCDC SD3 switch output to coil	Open
9	F5	PVSS_SD3	GND	DCDC SD3 neg supply terminal	Always needed
10	E4	FB_SD3	ANA IN	DCDC SD3 Feedback pin	Open
11	F4	VIN_LDO2	SUP IN	Supply pin for LDO2	Always needed
12	D4	LDO2	ANA OUT	Output Voltage of LDO2	Open
13	D3	LDO1	ANA OUT	Output Voltage of LDO1	Open
14	F3	VIN_LDO1	SUP IN	Supply pin for LDO1	Always needed
15	E3	FB_SD2	ANA IN	DCDC SD2 Feedback pin	Open
16	F2	PVSS_SD2	GND	DCDC SD2 neg supply terminal	Always needed
17	E2	LX_SD2	DIG OUT	DCDC SD2 switch output to coil	Open
18	E1	VSUP_SD2	SUP IN	DCDC SD2 pos supply terminal	Always needed
19	C3	FB_SD1	ANA IN	DCDC SD1 Feedback pin	Open
20	D2	PVSS_SD1	GND	DCDC SD1 neg supply terminal	Always needed
21	C2	LX_SD1	DIG OUT	DCDC SD1 switch output to coil	Open
22	C1	VSUP_SD1	SUP IN	DCDC SD1 pos supply terminal	Always needed
23	B1	V2_5	ANA OUT	Internal 2.5V regulator output	Always needed
24	A1	SCL	DIG IN	2-wire Serial IF Clock Input	Open
25	B2	SDA	DIG IO	2-wire Serial IF Data IO	Open
26	B3	ON	DIG IN	Power Up Input	Open
27	A2	XRES	DIG IO	Reset IO, external pull-up resistor needed	Always needed

Pin Number		Pin Name	Pin Type	Description	If not Used
QFN	WLP				
28	A3	GPIO2	ANA IO	General Purpose IO 2	Open
29	C4	GPIO1	ANA IO	General Purpose IO 1	Open
30	A4	VSSA	GND	GND Reference for analog blocks	Always needed
31	B4	FB_SD5	ANA IN	DCDC SD5 Feedback pin	Open
32	A5	PVSS_SD5	GND	DCDC SD5 neg supply terminal	Always needed
33		VSS	GND	Exposed Pad	Always needed

Absolute Maximum Ratings

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Figure 6:
Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units	Comments
Electrical Parameters					
	Supply Voltage to Ground 5V pins	-0.5	7.0	V	Applicable for pins: VSUP_SDx, VIN_LDOx, SCLK, SDA, ON, XRES, GPIOx, LX_SDx
	Supply Voltage to Ground 3V pins	-0.5	5.0	V	Applicable for pins: V2_5, LDOx, FB_SDx
	Voltage Difference between Ground Terminals	-0.3	0.3	V	Applicable for pins: VSSA, PVSS_SDx, Exposed Pad
	Input Current (latch-up immunity)	-100	100	mA	Norm: JEDEC JESD78
Continuous Power Dissipation (T_A = +70°C)					
P_T	Continuous power dissipation		1.2	W	P_T [(1)] for QFN32 package (R_{THJA} ~ 45K/W)
			1.1	W	P_T [(1)] for WL-CSP36 package (RTHJA ~ 50K/W)
Electrostatic Discharge					
$V_{ESD-HBM}$	Electrostatic Discharge HBM		±2	kV	Norm: JEDEC JESD22-A114F
Temperature Ranges and Storage Conditions					
T_{AMB}	Operating Temperature	-40	+85	°C	
T_J	Junction Temperature		+125	°C	
	Storage Temperature Range	-55	+150	°C	QFN
	Storage Temperature Range	-55	+125	°C	WL-CSP
	Humidity non-condensing		85	%	

Symbol	Parameter	Min	Max	Units	Comments
Temperature (Soldering)					
T_{BODY}	Package Body Temperature		+260	°C	32-pin QFN: Norm IPC/JEDEC J-STD-020 (2) The lead finish for Pb-free leaded packages is matte tin (100% Sn)
T_{BODY}	Package Body Temperature		+260	°C	36-ball WL-CSP: Norm IPC/JEDEC J-STD-020 (2)
MSL_{QFN}	Moisture Sensitive Level	3			Represents a maximum floor life time of 168h
MSL_{WL-CSP}	Moisture Sensitive Level	1			Represents an unlimited floor life time

Note(s) and/or Footnote(s):

1. Depending on actual PCB layout and PCB used.
2. The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020 "Moisture/Reflow Sensitivity Classification for Non hermetic Solid State Surface Mount Devices

Electrical Characteristics

All limits are guaranteed. The parameters with min and max values are guaranteed with production tests or SQC (Statistical Quality Control) methods.

Figure 7:
Electrical Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage range	Pin V_{SUP}	2.7		5.5	V
I_Q	Quiescent Current	Normal operating current. With bit Low_power_on = 0; only V2_5 active		155	200	µA
$I_{LOWPOWER}$	Low-Power Quiescent Current	Normal operating current. With bit Low_power_on = 1; only V2_5 active		110		
$I_{POWEROFF}$	Shutdown Current	With bit power_off = 1; only V2_5 is active in power OFF mode. Not tested, guaranteed by design		7	20	

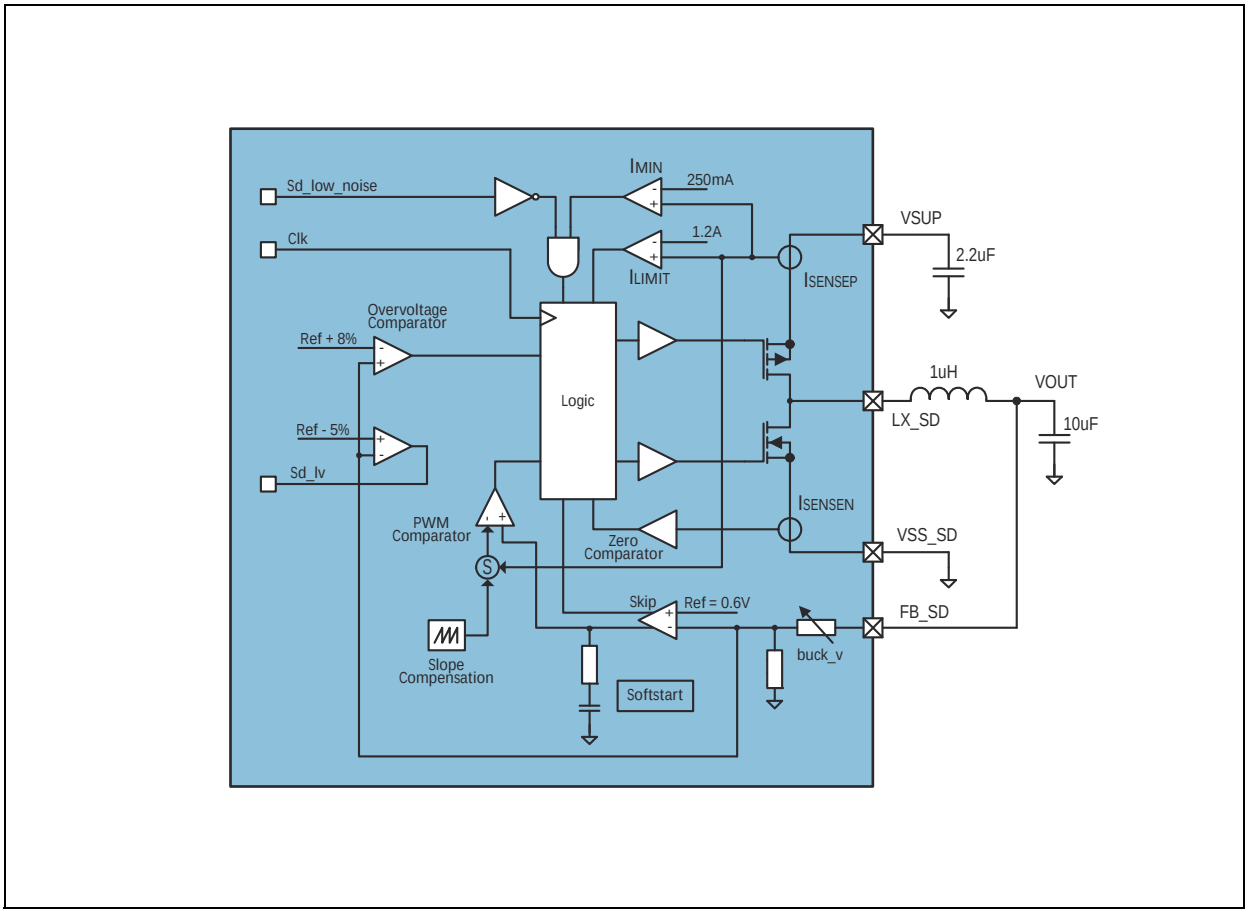
Electrical Characteristics: V_{SUP} = 3.7V, $V_{OUT} < V_{IN} - 0.5V$, T_{AMB} = -40°C to +85°C, typ. values @ T_{AMB} = +25°C (unless otherwise specified)

Detailed Description - Power Management Functions

Step Down DCDC Converter

The step-down converter is a high-efficiency fixed frequency current mode regulator. By using low resistance internal PMOS and NMOS switches, efficiency up to 95% can be achieved. The fast switching frequency allows using small inductors, without increasing the current ripple. The unique feedback and regulation circuit guarantees optimum load and line regulation over the whole output voltage range, up to an output current of 1A, with an output capacitor of only 10µF. The implemented current limitation protects the DCDC Converter and the coil during overload condition.

Figure 8:
Step Down DC/DC Converter Block Diagram



Mode Settings

To allow optimized performance in different applications, there are bit settings possible, to get the best compromise between high efficiency and low input/output ripple.

Low-Ripple, Low-Noise Operation

Low-ripple, low-noise operation can be enabled by setting bit *sd_low_noise* = 1.

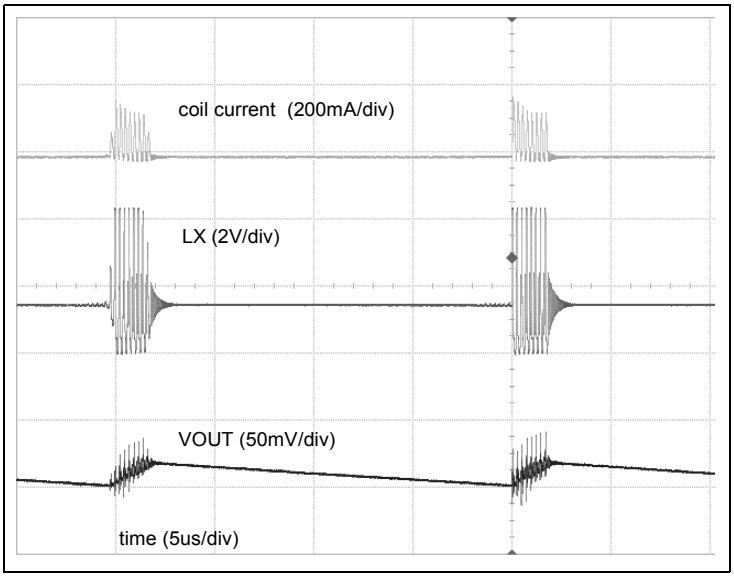
In this mode there is no minimum coil current necessary before switching OFF the PMOS. As long as the load current is superior to the ripple current, the device operates in continuous mode. When the load current gets lower, the discontinuous mode is triggered. Resultant the auto-zero comparator stops the NMOS conduction to avoid load discharger and the duty cycle is reduced down to t_{MIN_ON} to keep the regulation loop stable. This results in a very low ripple and noise, but decreased efficiency at light loads, especially at low input to output voltage differences.

Only in the case the load current gets so small, that less than the minimum on time of the PMOS would be needed to keep the loop in regulation, the regulator will enter low power mode operation.

The crossover point is about 15mA for V_{IN} = 3V, V_{OUT} = 1.2V, 1µH, 4MHz.

Figure 9:
DC/DC Buck Low Noise Mode

DC/DC buck burst mode: Shows the DC/DC switching waveforms for low noise operation.



High-Efficiency Operation (Default Setting)

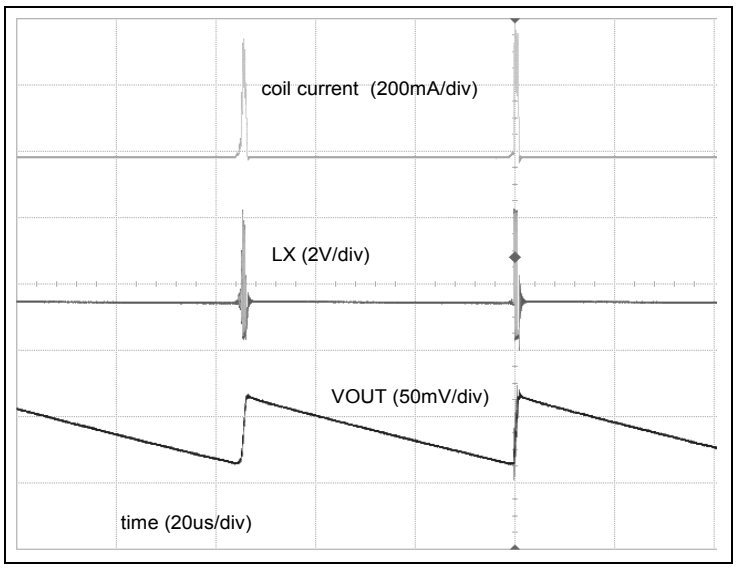
High-efficiency operation is enabled by setting bit *sd_low_noise* = 0.
In this mode there is a minimum coil current necessary before switching OFF the PMOS. Resultant there are less pulses

necessary at low output loads, and therefore the efficiency increases. As drawback, this mode increases the ripple up to a higher output current.

The crossover point to low power mode is already reached at reasonable high output currents. (e.g. @110mA for V_{IN} = 3V, V_{OUT} = 1.2V, 1µH, 4MHz)

Figure 10:
DC/DC Buck High Efficiency Mode

DC/DC buck burst mode: Shows the DC/DC switching waveforms for high efficiency operation



Low Power Mode Operation (Automatically Controlled)

As soon as the output voltage stays above the desired target value for a certain time, some internal blocks will be powered down leaving the output floating to lower the power consumption. Normal operation starts as soon as the output drops below the target value for a similar amount of time. To minimize the accuracy error some internal circuits are kept powered to assure a minimized output voltage ripple.

Two addition guard bands, based on comparators, are set at ±5% of the target value to react quickly on large over/undershoots by immediately turning on the output drivers without the normal time delays. This ensures a minimized ripple also in very extreme load conditions.

DVM (Dynamic Voltage Management)

To minimize the over-/undershoot during a change of the output voltage, the DVM can be enabled. With DVM the output voltage will ramp up/down with a selectable slope after the new value was written to the registers. Without DVM the slew rate of the output voltage is only determined by external components like the coil and load capacitor as well as the load current.

DVM can be selected for all step-down converters, but only for one at a time. (see *sd_dvm_select* and *dvm_time* description)

Fast Regulation Mode

This mode can be used to react faster on sudden load changes and thus minimize the over-/undershoot of the output voltage. This mode needs a 22uF output capacitor instead the 10uF one to guarantee the stability of the regulator.

The mode is enabled by setting *sd_fast* =1.

Selectable Frequency Operation

Especially for very low load conditions, e.g. during a sleep mode of a processor, the switching frequency can be reduced to achieve a higher efficiency. The frequency can be set to 2, 3 or 4MHz and this mode is selected by setting *sd_freq* and *sd_fsel* to the appropriate values.

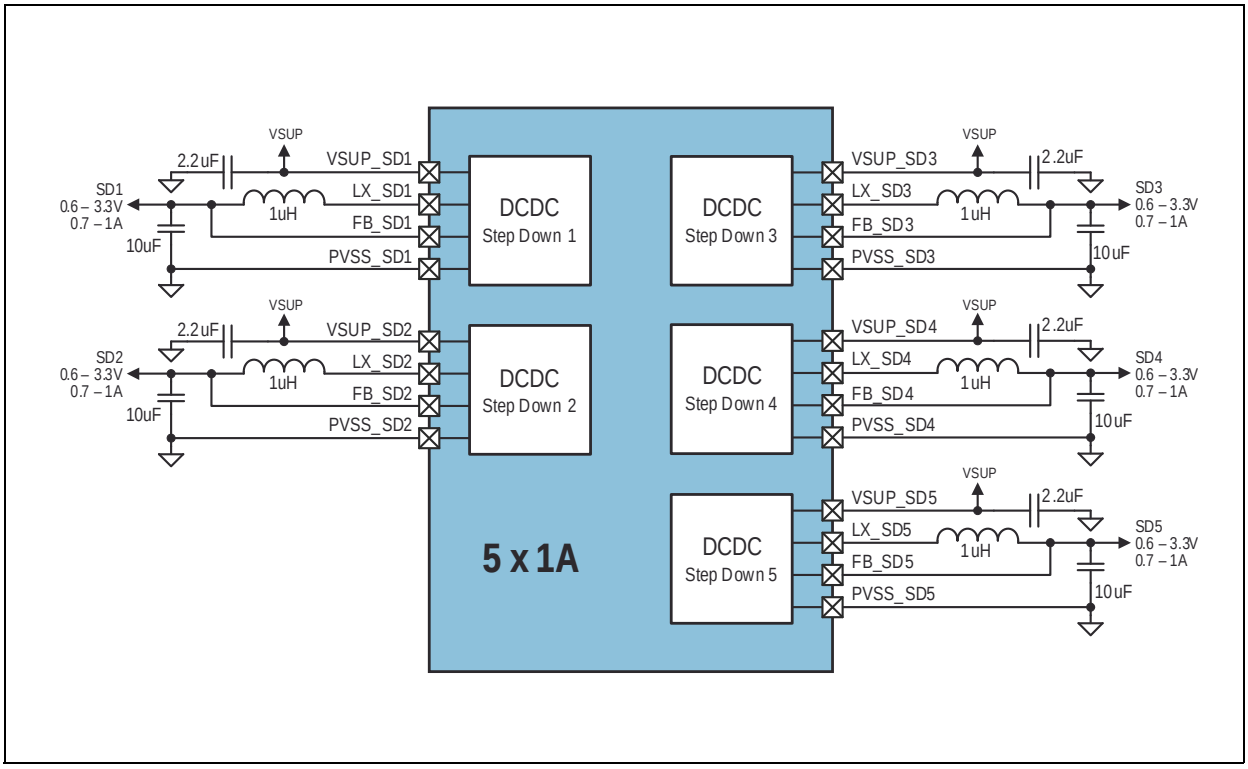
100% PMOS ON Mode for Low Dropout Regulation

For low input to output voltage difference the DCDC converter can use 100% duty cycle for the PMOS transistor, which is then in LDO mode.

Step Down Converter Configuration Modes

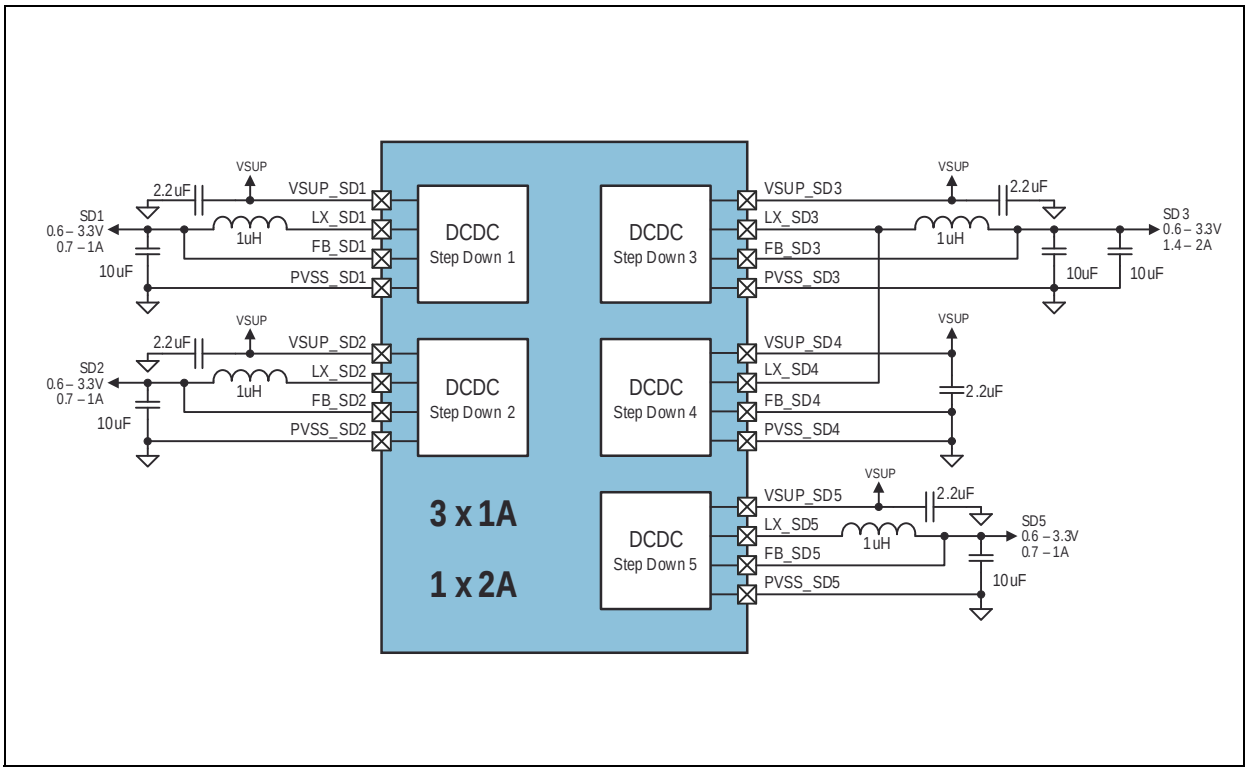
The step down dc/dc converters have two configuration modes to deliver different output currents for the applications. The operating mode is selected by setting the bit *sd2_slave*, *sd4_slave* and *sd5_slave* (the default is set by the Boot-OTP).

Figure 11:
DCDC Step Down Normal Operating Mode



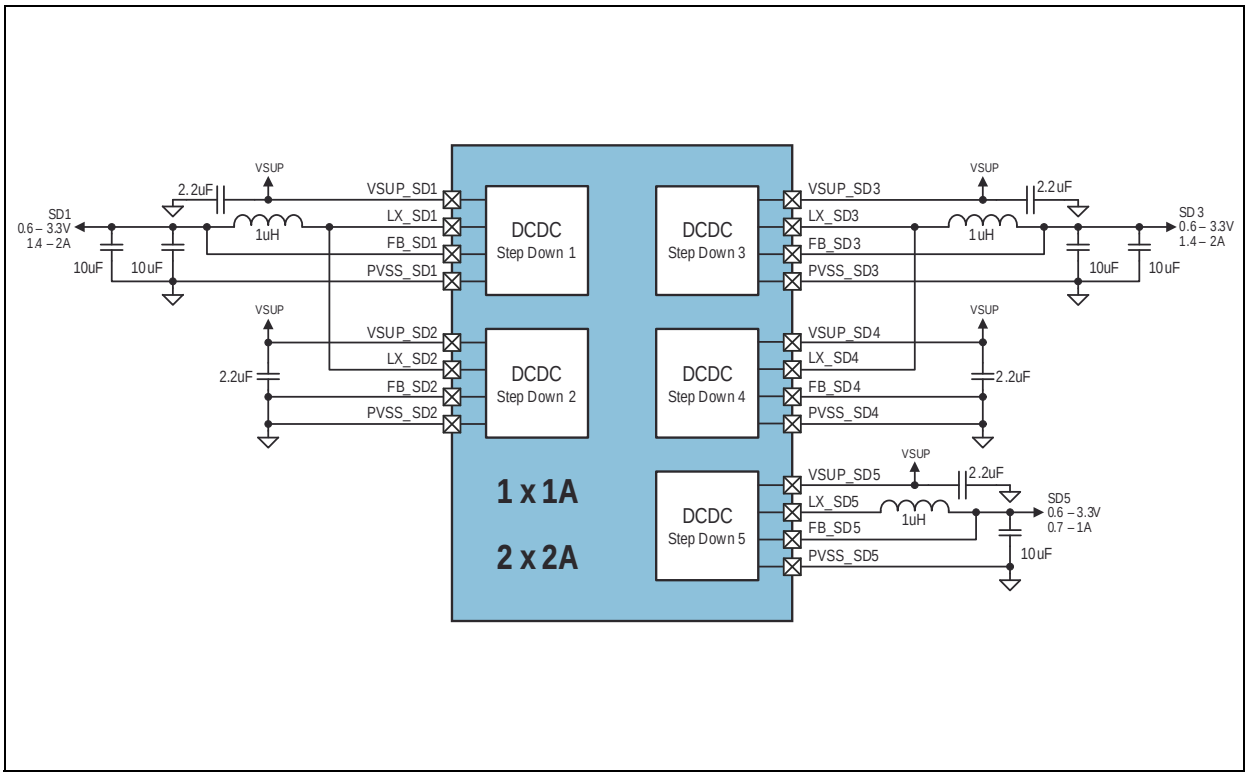
Normal Operating Mode: sd2_slave = 0, sd4_slave = 0, sd5_slave = 0

Figure 12:
DCDC Step Down SD3/SD4 Operating Mode



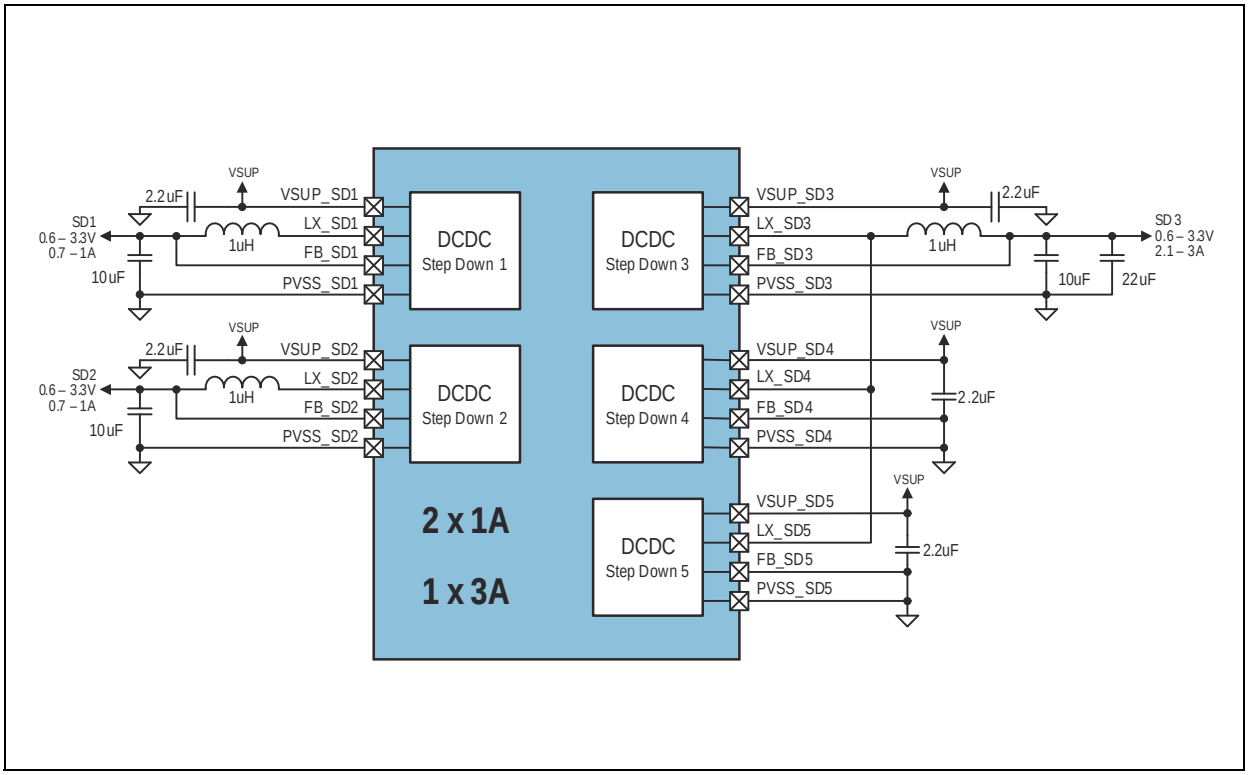
SD3/SD4 Operating Mode: sd2_slave = 0, sd4_slave = 1, sd5_slave = 0

Figure 13:
DCDC Step Down SD1/SD2 & SD3/SD4 Operating Mode



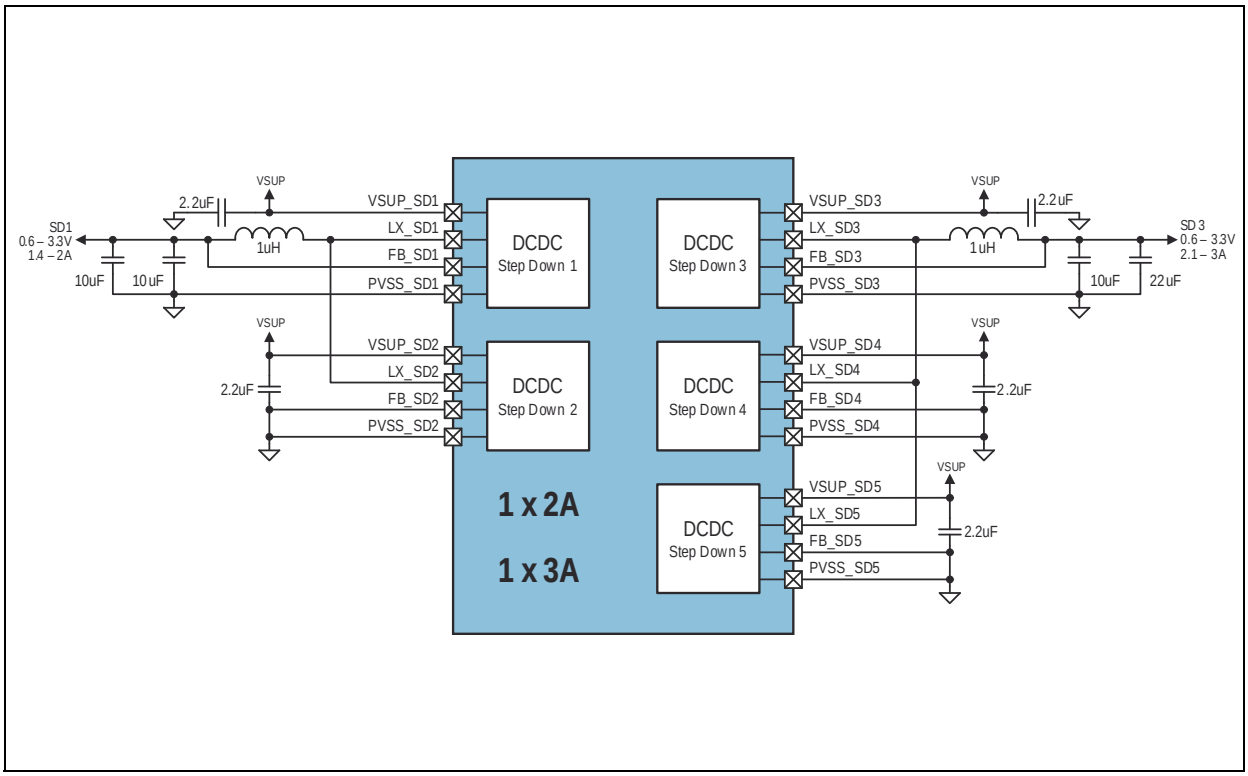
SD3/SD4 & SD4/SD5 Operating Mode: sd2_slave = 1, sd4_slave = 1, sd5_slave = 0

Figure 14:
DCDC Step Down SD3/SD4/SD5 Operating Mode



SD3/SD4/SD5 Operating Mode: sd2_slave = 0, sd4_slave = 1, sd5_slave = 1

Figure 15:
DCDC Step Down SD1/SD2 & SD3/SD4/SD5 Operating



SD1/SD2 & SD3/SD4/SD5 Operating Mode: sd2_slave = 1, sd4_slave = 1, sd5_slave = 1

Parameters

Figure 16:
Step Down DCDC Converter Electrical Characteristics

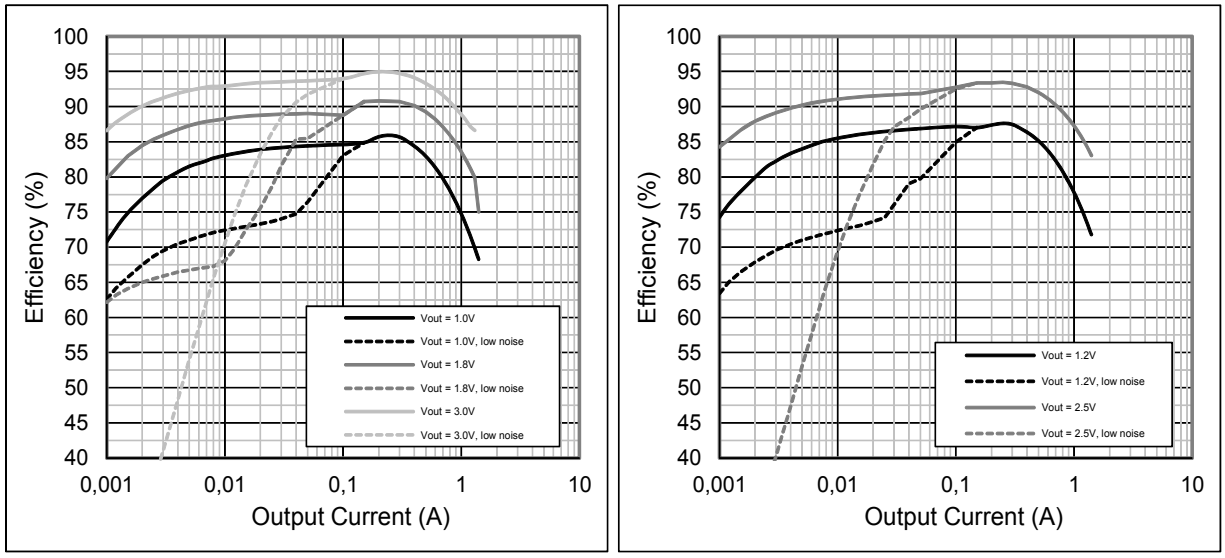
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	Input Voltage	Pin V_{SUP}	2.7		5.5	V
V_{OUT}	Regulated Output Voltage		0.6125		3.35	V
V_{OUT_TOL}	Output Voltage Tolerance	min. 40mV	-3		+3	%
I_{LIMIT}	Current Limit			1.2		A
R_{PMOS}	P-switch ON resistance			0.25	0.5	Ω
R_{NMOS}	N-switch ON resistance			0.25	0.5	Ω
f_{SW}	Switching Frequency	*sdX_frequ* = 1 *sdX_fsel* = 1 *fclk_int* = 4MHz		4		MHz
		sdX_frequ = 1 *sdX_fsel* = 0 *fclk_int* = 4MHz		3		MHz
		sdX_frequ = 0 *sdX_fsel* = 0 *fclk_int* = 4MHz		2		MHz
I_{LOAD}	Load Current	$V_{OUT} \leq 1.8V$	0		1	A
		$V_{OUT} > 1.8V$	0		0.7	
I_{SUP_DCDC}	Current Consumption	Operating Current without Load		60		µA
		Shutdown Current		0.1		
t_{MIN_ON}	Minimum ON Time			40		ns
η_{EFF}	Efficiency	See figures below				%

Figure 17:
Step Down DCDC External Components

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{FB_SDx}	Output Capacitor	Ceramic X5R or X7R	8	10		µF
C_{VSUP_SDx}	Input Capacitor	Ceramic X5R or X7R		2.2		µF

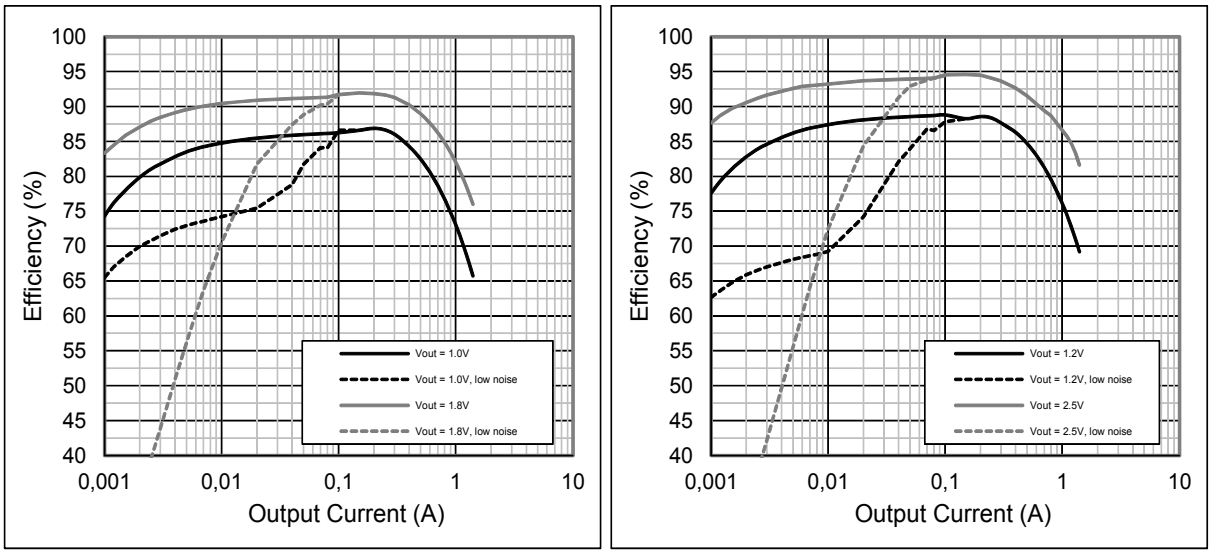
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
L_{SDx}	Inductor	4MHz operation		1		µH
		3MHz operation		1		
		2MHz operation		2.2		

Figure 18:
DCDC SD1 Efficiency vs. Output Current



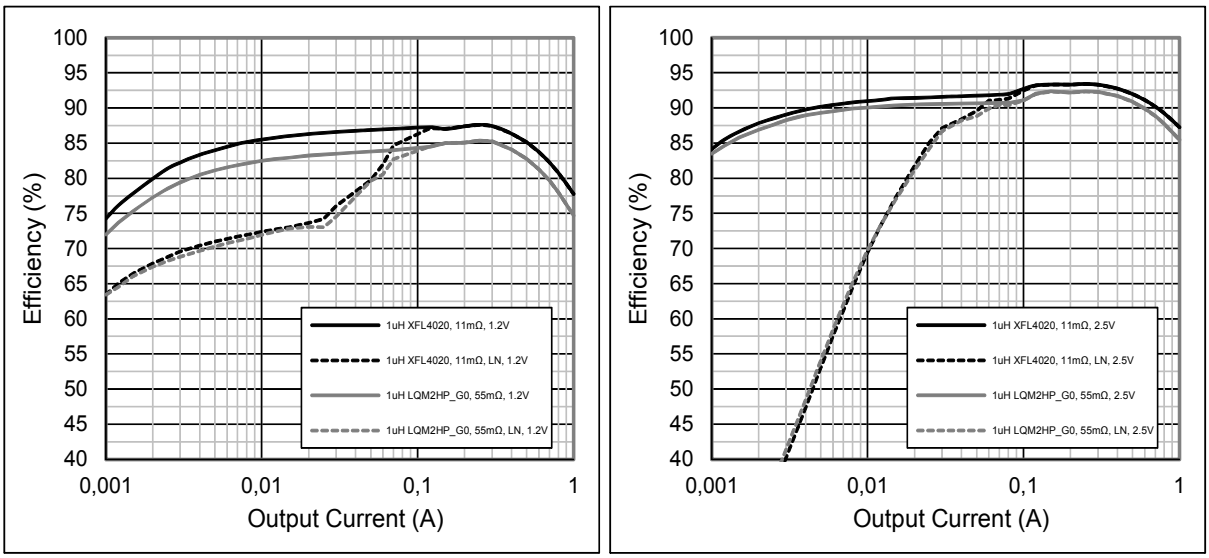
SD1 Efficiency vs. Output Current: V_{IN} = 3.7V, 3MHz operation, XFL4020 1uH coil, T_A = +25°C

Figure 19:
DCDC SD1 Efficiency vs. Output Current



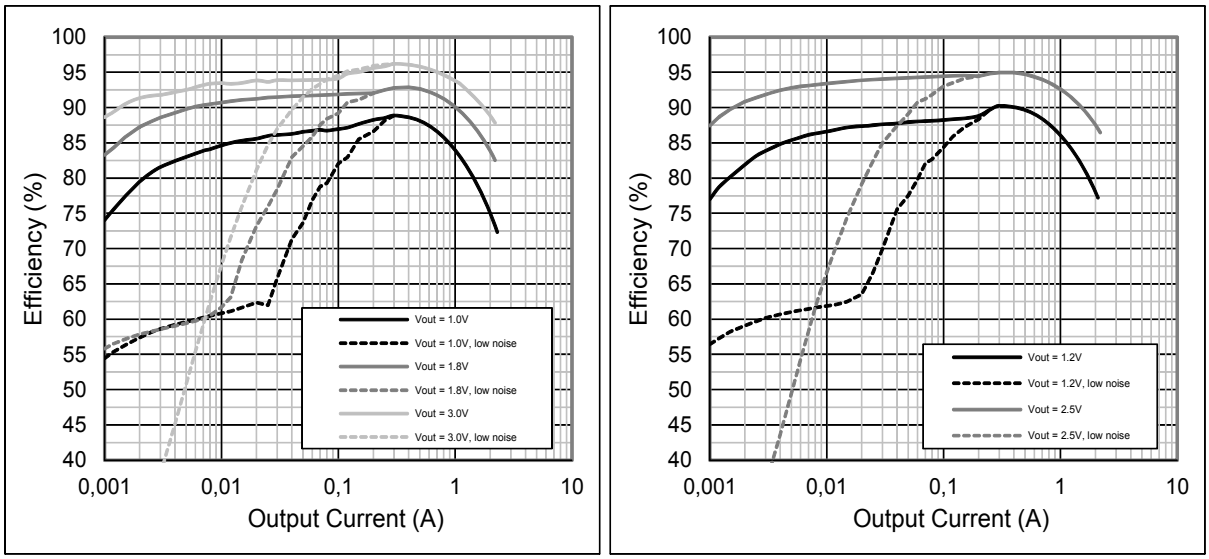
SD1 Efficiency vs. Output Current: V_{IN} = 3.0V, 3MHz operation, XFL4020 1µH coil, T_A = +25°C

Figure 20:
DCDC SD1 Efficiency vs. Output Current



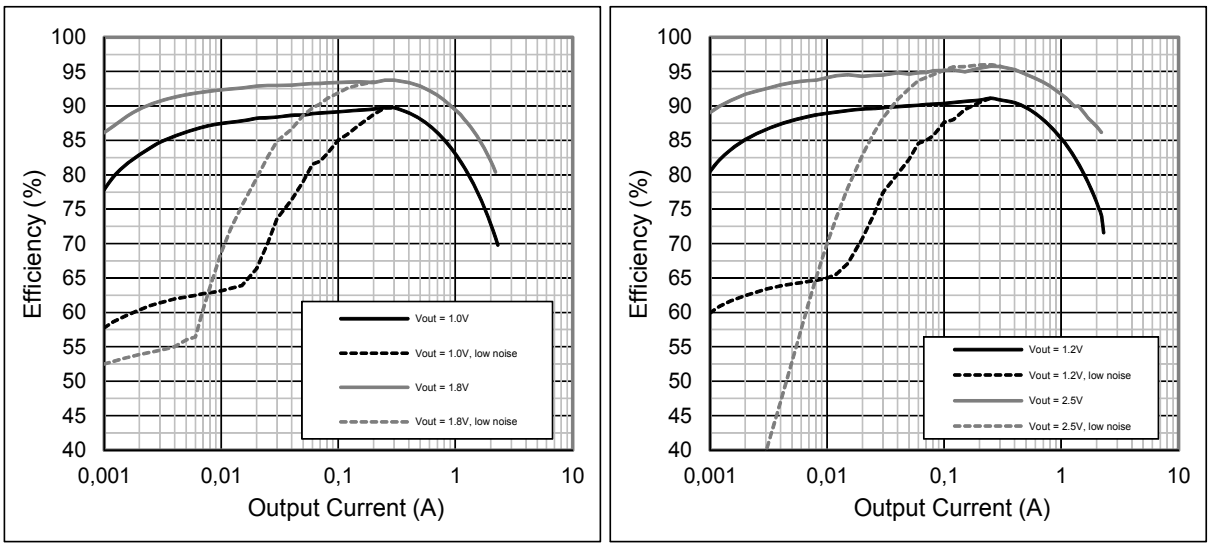
SD1 Efficiency vs. Output Current: V_{IN} = 3.7V, V_{OUT} = 1.2V/2.5V, 3MHz operation, T_A = +25°C

Figure 21:
DCDC SD1 + SD2 Efficiency vs. Output Current



SD1 + SD2 Efficiency vs. Output Current: V_{IN} = 3.7V, 3MHz operation, XFL4020 1µH coil, T_A = +25°C

Figure 22:
DCDC SD1 + SD2 Efficiency vs. Output Current



SD1 + SD2 Efficiency vs. Output Current: V_{IN} = 3.0V, 3MHz operation, XFL4020 1µH coil, T_A = +25°C

Figure 23:
DCDC SD1 + SD2 Efficiency vs. Output Current

SD1 + SD2 Efficiency vs. Output Current: V_{IN} = 3.7V, V_{OUT} = 1.2V, 3MHz operation, T_A = +25°C

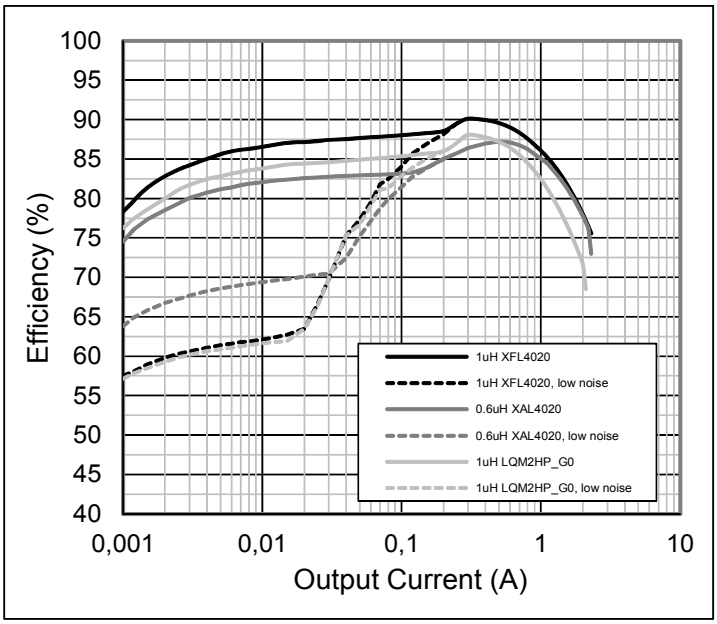
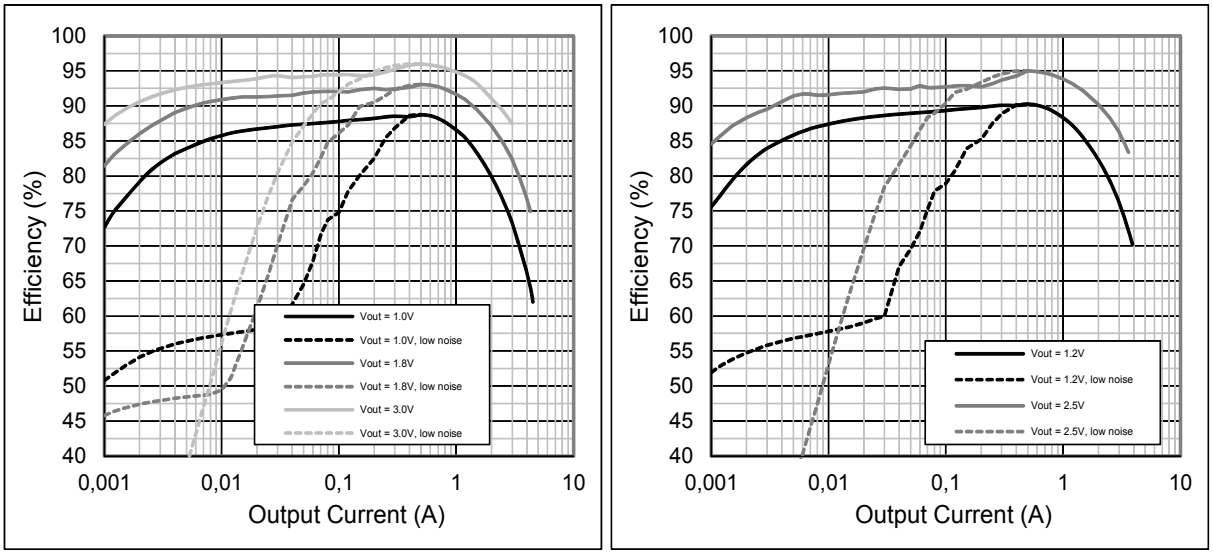
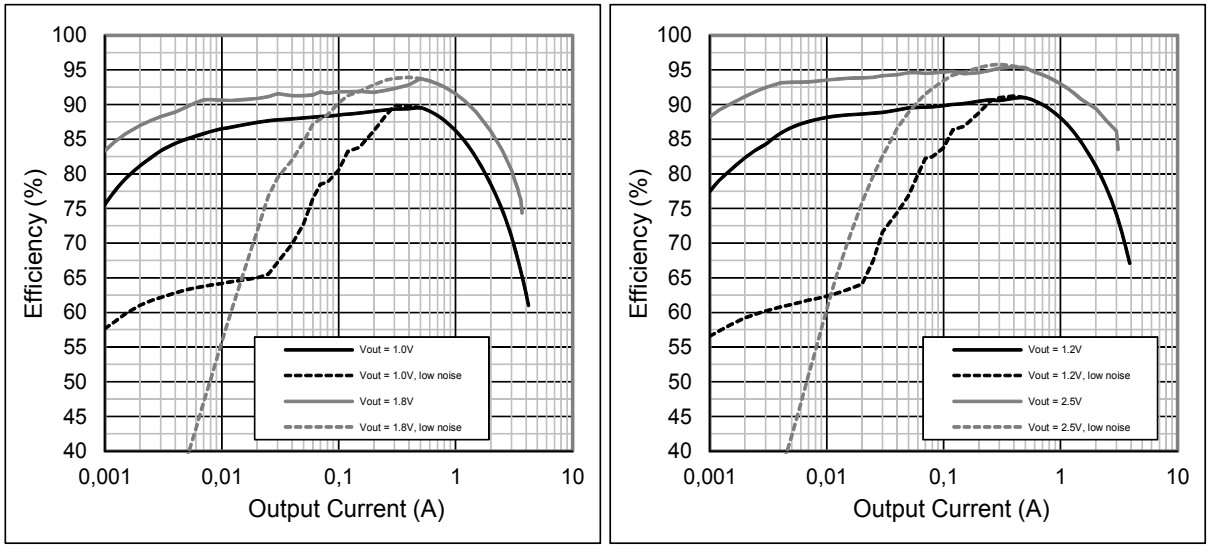


Figure 24:
DCDC SD3 + SD4 + SD5 Efficiency vs. Output Current



SD3 + SD4 + SD5 Efficiency vs. Output Current: V_{IN} = 3.7V, 3MHz operation, XFL4020 1µH coil, T_A = +25°C

Figure 25:
DCDC SD3 + SD4 + SD5 Efficiency vs. Output Current



SD3 + SD4 + SD5 Efficiency vs. Output Current: V_{IN} = 3.0V, 3MHz operation, XFL4020 1µH coil, T_A = +25°C

Figure 26:
DCDC SD3 + SD4 + SD5 Efficiency vs. Output Current

SD3 + SD4 + SD5 Efficiency vs. Output Current: V_{IN} = 3.7V, V_{OUT} = 1.2V, 3MHz operation, T_A = +25°C

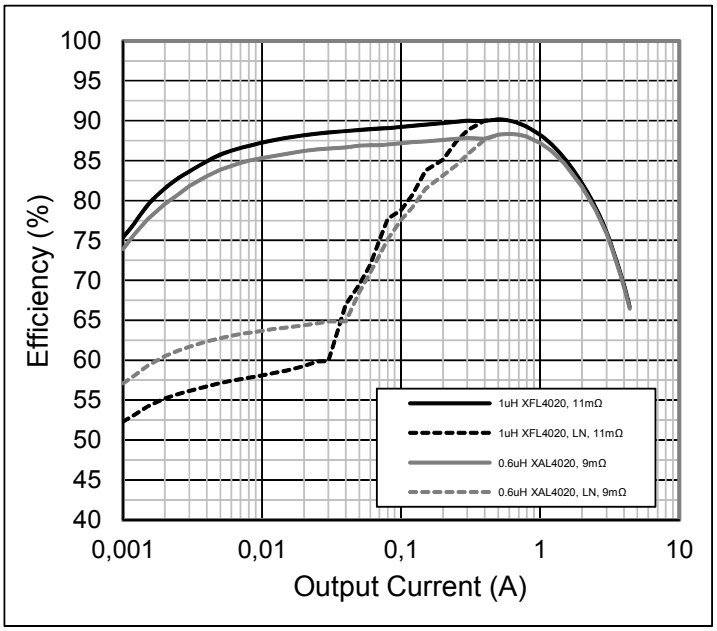
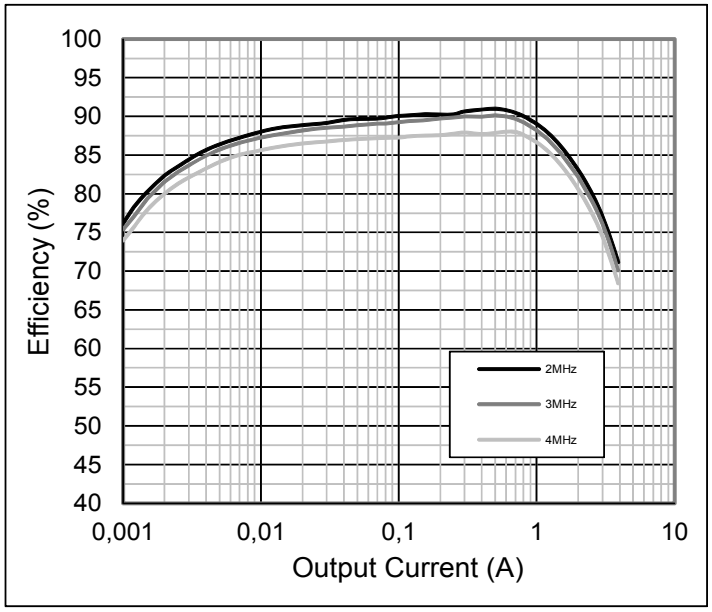


Figure 27:
DCDC SD3 + SD4 + SD5 Efficiency vs. Output Current

SD3 + SD4 + SD5 Efficiency vs. Output Current: V_{IN} = 3.7V, V_{OUT} = 1.2V, XFL4020 1µH coil, T_A = +25°C

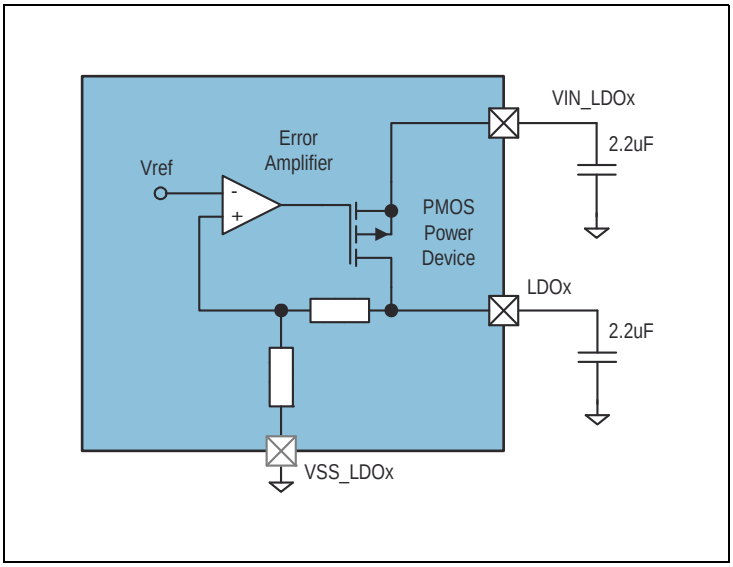


Universal IO LDO Regulators

2 universal IO range LDOs offer a wide input (1.8V to 5.5V) as well as a wide output (0.8 to 3.3V) voltage range to be used for general purpose peripheral supply. Up to 300mA possible output currents are offered with good noise and regulation performance and very low quiescent current even suitable for stand-by power supply.

Figure 28:
Universal IO LDO Block Diagram

AS3709 LDO: Shows the detailed Universal IO LDO Block Diagram



Parameter

Figure 29:
Universal IO LDO Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{IN}	Input Voltage Range	Pin VIN_LDOx	1.75		5.5	V
V_{OUT_TOL}	Output Voltage Tolerance	Min. 40mV	-3		+3	%
V_{OUT}	Output Voltage Range	Pin LDOx I_{OUT} < 150mA, 25mV steps	0.825		3.3	V
I_{OUT_L}	Output current (Note:)	ldoX_ilimit = 0 (150mA)	0		150	mA
I_{LIMIT_L}	Current limit (Note:)			300		mA
I_{OUT_H}	Output current (Note:)	ldoX_ilimit = 1 (300mA)	0		300	mA
I_{LIMIT_H}	Current limit (Note:)			500		mA
R_{ON}	On resistance	LDO1, LDO2		0.6		Ω
PSRR	Power supply rejection ratio	f=1kHz	60			dB
		f=100kHz	30			
I_{OFF}	Shut down current			100		nA
I_Q	Quiescent Current	Without load		30	43	µA
t_{START}	Startup time	Low current used during start-up			500	us
V_{LNR}	Line Regulation	Static		0.07		%/V
		Transient; Slope: tr=15µs; delta 1V		20		mV
V_{LDR}	Load Regulation	Static		0.014		%/mA
		Transient; Slope: tr=15µs; 1mA -> 300mA		30		mV

Note: Guaranteed by design and verified by laboratory evaluation and characterization; not production tested

Figure 30:
Universal IO LDO Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{OUT_LDOx}	Output Capacitor	Ceramic X5R or X7R	0.7	2.2		µF
C_{VIN_LDOx}	Input Capacitor	Ceramic X5R or X7R	1	2.2		µF

Low Power LDO V2_5 Regulator

The low power LDO V2_5 is needed to supply the chip core (analog and digital) of the device. It is designed to get the lowest possible power consumption and still offering reasonable characteristics. To ensure high PSRR and stability, a low-ESR ceramic capacitor of min. 0.7µF must be connected to the output.

Parameter

Figure 31:
Low Power V2_5 LDO Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
	Supply Voltage Range	See V_{SUP}				
V_{OUT}	Output Voltage		2.4	2.5	2.6	V
R_{ON}	On resistance	Guaranteed by design		50		Ω
I_{OFF}	Shut down current			100		nA
I_Q	Quiescent Current	Guaranteed by design, consider chip internal load for measurements		3		µA
t_{START}	Startup time			200		µs

Figure 32:
Universal IO LDO Electrical Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
C_{V2_5}	Output Capacitor	Ceramic X5R or X7R	0.7	1		µF

Detailed Description - System Functions

Start-up

Normal Start-up

During a normal reset cycle (e.g. after the battery is inserted), after V2_5 is above V_{POR} and V_{SUP} is above ResVoltRise a normal startup happens:

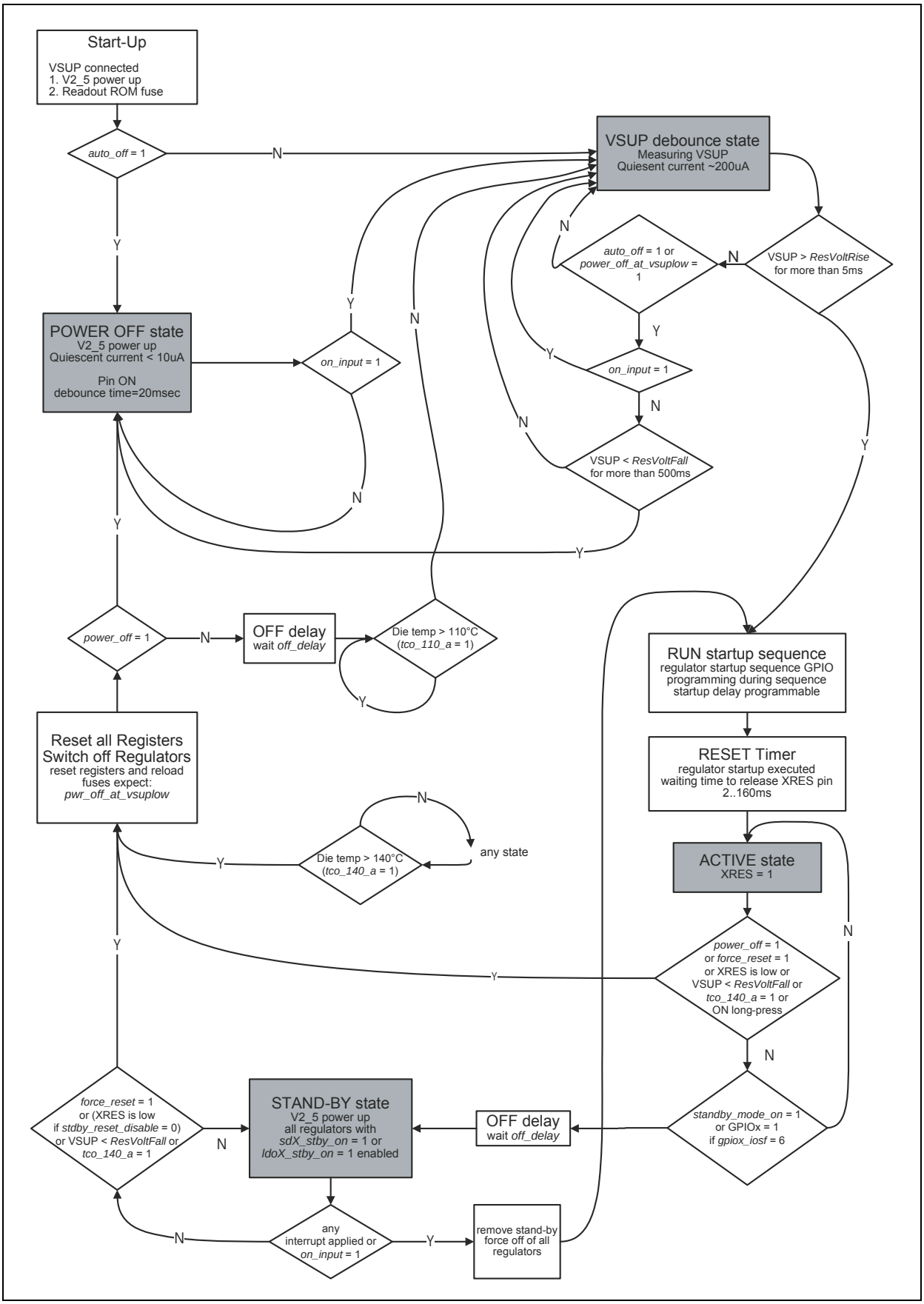
- Configuration of DCDCs (combined mode or separated) is read from the Boot-OTP
- Startup State machine reads out the internal Boot-OTP
- Reset-Timer is set by the Boot-OTP
- The reset is released when the Reset Timer expires (external pin XRES)

Parameter

Figure 33:
ON Input Start-up Condition

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{ON_IL}	ON Low Level Voltage				0.4	V
V_{ON_IH}	ON High Level Voltage		1.4			V
I_{ON_PD}	ON Pull Down Current		4	12		µA

Figure 34:
Start-up Flowchart



Reset

XRES is a low active bi-directional pin. An external pull-up to the periphery supply has to be added. During each reset cycle the following states are controlled by the AS3709:

- Pin XRES is forced to GND
- Normal startup with programmable power-on sequence and regulator voltages
- Reset is active until the programmable reset timer (set by register bits *res_timer<2:0>*) expires
- All registers are set to their default values after power-on, except the reset control- and status-registers

RESET Reasons

Reset can be activated from 7 different sources:

- V_{POR} has been reached (V_{SUP} reached POR level)
- ResVoltFall was reached (V_{SUP} drops below ResVoltFall)
- Software forced reset
- Power off mode
- External triggered through the pin XRES
- Over-temperature
- ON-key long press

Voltage Detection

There are two types of voltage dependent resets: V_{POR} and V_{XRES}. V_{POR} monitors the voltage on V2_5 and V_{XRES} monitors the voltage on V_{SUP}. The linear regulator for V2_5 is always on and uses the voltage V_{SUP} as its source. The pin XRES is only released if V2_5 is above V_{POR} and V_{SUP} is above ResVoltRise.

Power OFF

To put the chip into ultralow power mode, write '1' into *power_off*.
The chip stays in power off mode until

- The external pin ON is pulled high
- The V_{POR} level is touched to start a complete reset cycle

The bit *power_off* is automatically cleared by this reset cycle.

During *power_off* state all circuits are shut-off except the Low Power LDO (V2_5). Thus the current consumption of AS3709 is reduced to less than 7µA. The digital part is supplied by V2_5, all other circuits are turned off in this mode, including references and oscillator. Except the reset control registers, all other registers are set to their default value after power-on.

Software Forced Reset

Writing '1' into the register bit *force_reset* immediately starts a reset cycle. The bit *force_reset* is automatically cleared by this reset.

External Triggered Reset

If the pin XRES is pulled from high to low by an external source (e.g. microprocessor or button) a reset cycle is started as well.

Over-temperature Reset

The reset cycle can be started by over-temperature conditions.

Long ON-key Press

When applying a high level on the ON input pin for 4s/8s (depending on *on_reset_delay*) a reset is initiated. This is thought as a safety feature when the SW hangs up.

Parameter

Figure 35:
XRES Input Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{XRES_IL}	RESET Low Level Voltage				0.4	V
V_{XRES_IH}	RESET High Level Voltage		1.4			V

Figure 36:
RESET Levels

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{POR}	Overall Power On Reset	Monitor voltage on V2_5 power on reset for all internal functions	1.5	2.0	2.3	V
V_{RES_RISE}	RESET Level for V_{SUP} rising	Monitor voltage on V_{SUP} rising level		ResVoltRise (1)		V
V_{RES_FALL}	RESET Level for V_{SUP} falling	Monitor voltage on V_{SUP} falling level		2.7		V
		if *SupResEn* = 1 only		ResVoltFall (2)		V

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{RES_MASK}	Mask time for V_{XRES_fall} Duration for V_{SUP} < ResVoltFall until a reset cycle is started (3)	*FastResEn* = 0		3		ms
		FastResEn = 1		4		µs

Note(s) and/or Footnote(s):

1. The selection of the range and level is done via OTP. It's recommended to set the ResVoltRise level 200mV above the ResVoltFall level to have a hysteresis.
2. 2.7V is the default value, other levels can be set via SW.
3. XRES signal is debounced with the specified mask time for rising- and falling slope of VSUP
4. VRES_FALL is only accepted if the reset condition is longer than VRES_MASK. This guard time is used to avoid a complete reset of the system in case of short drops of VSUP.

Figure 37:
ResVoltRise/ResVoltFall Levels

Mode	000	001	010	011	100	101	110	111
3.3V	2.7V	2.8V	2.9V	3.0V	3.1V	3.2V	3.3V	3.4V
5.0V	3.6V	3.7V	3.8V	3.9V	4.0V	4.1V	4.2V	4.4V

Note: If bit reslevel_5V is "1", then the 5.0V mode is selected.

Stand-by

Stand-by allows shutting down a part or the complete system. Stand-by can be terminated by every possible interrupt or GPIO of the PMU. The interrupt has to be enabled and GPIO has to be configured before going to stand-by.

Figure 38:
Stand-by

State	Description
Enter via GPIO	To enter stand-by mode the following settings have to be done: • Enable just these IRQ sources which should lead to leave stand-by mode. • Make sure that IRQ is inactive (IRQ flags get cleared by register reading) • Set the GPIO to input (*gpioX_mode* = 0) • Set the GPIO for stand-by control (*gpioX_iosf* = 6) • Set *regX_select* to define the sequence for going into stand-by for up to 3 regulators • Set *regX_voltage_stby* if another voltage is needing during stand-by • Define which regulators should be kept powered during stand-by (*sdX_stby_on* and *ldoX_stby_on*) • Activate the selected GPIO
Enter via SW	To enter stand-by mode the following settings have to be done: • Enable just these IRQ sources which should lead to leave stand-by mode. • Make sure that IRQ is inactive (IRQ flags get cleared by register reading) • Define which regulators should be kept powered during stand-by (*sdX_stby_on* and *ldoX_stby_on*) • Set the delay for going into stand-by after the SW command *(off_delay*) • Set *standby_mode_on* to 1
Stand-by	V2_5 chip supply is kept ON All other regulators are switched OFF dependent on the bits *sdX_stby_on* and *ldoX_stby_on* XRES goes active (can be disabled with *standby_reset_disable*) and pwr_good goes inactive
Leave	The chip will come out of stand-by with • IRQ activation or • GPIO control (if entered via GPIO) Start-Up sequence is provided defined by the boot ROM.

Internal References

Low Power Mode

Use bit *low_power_on* to activate the Low Power Mode. In this mode the on-chip voltage reference and the temperature supervision comparators are operating in pulsed mode. This reduces the quiescent current of the AS3709 by 45µA (typ.). Because of the pulsed function some specifications are not fulfilled in this mode (e.g. increased noise), but still the full functionality is available.

Note(s): Low power mode can be controlled by the serial interface.

Figure 39:
Reference Parameter

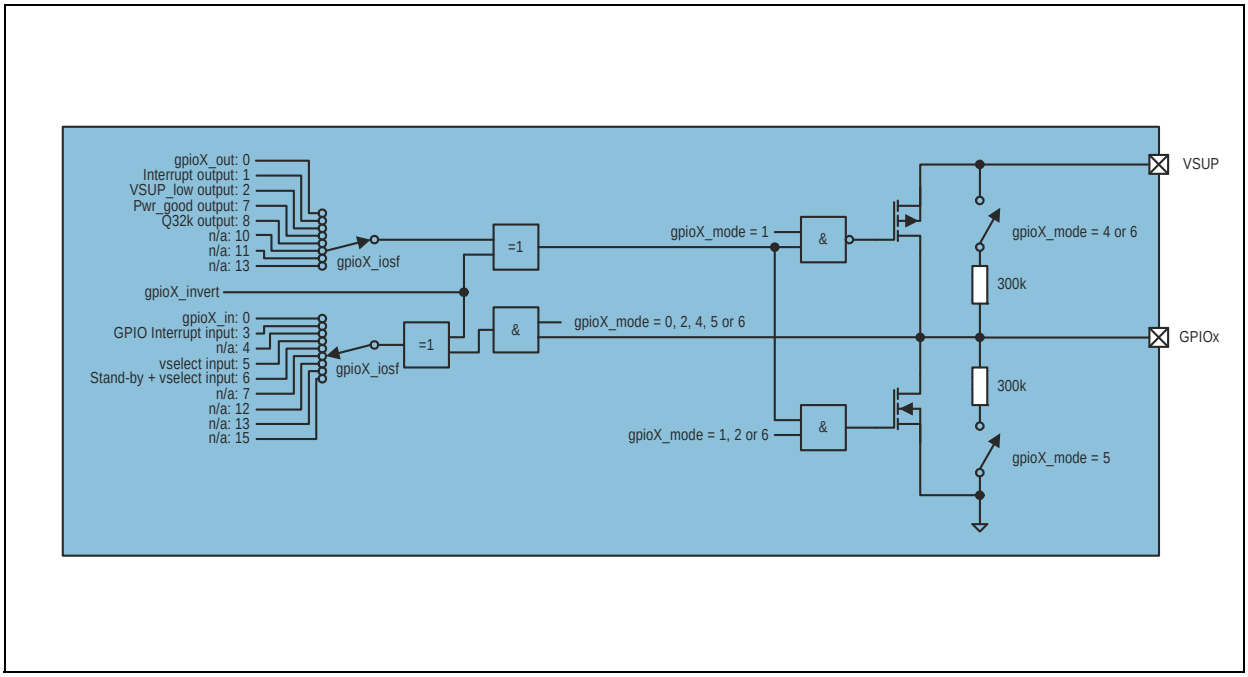
Symbol	Parameter	Note	Min	Typ	Max	Unit
f_{CLK}	Accuracy of Internal reference clock	Adjustable by serial interface register clk_int	-12	f_{CLK}	+12	%

GPIO Pins

The device contains 2 GPIO pins. Each of the pins can be configured as digital input, digital input (with pull-up or pull-down), push-pull output or open drain output (with or without pull-up). When configured as output the output source can be a register bit, or the PWM generator.

The polarity of the input and output signals can be inverted with the corresponding *gpioX_invert* bit, all further descriptions refer to normal (non-inverted) mode.

Figure 40:
GPIO Block Diagram



GPIO block diagram: Shows the internal structure of the IO pads

Figure 41:
GPIO Pin Characteristics

Symbol	Parameter	Note	Min	Typ	Max	Unit
V_{GPIO_max}	Max. voltage on GPIO1/2 pins	Pin V_{SUP} is used as supply for the GPIO pins			V_{SUP} + 0.3	V
V_{OL}	Low level output voltage	I_{OL}=+1mA digital output			+0.4	V
V_{OH}	High level output voltage	I_{OH}=–1mA; digital push-pull output	0.8*V_{SUP}			V
V_{IL}	Low level input voltage	Digital input			0.4	V
V_{IH}	High level input voltage	Digital input	1.4			V
$I_{LEAKAGE}$	Leakage current	High impedance			10	µA
$R_{pull-up}$	Pull-up resistance	if enabled; V_{SUP} = 3.6V		300		kΩ
$R_{pull-down}$	Pull-down resistance	if enabled; V_{SUP} = 3.6V		300		kΩ

GPIO Pins: Shows the key electrical parameter of the GPIO pins. V_{SUP}=2.7 to 5.5V; unless otherwise mentioned.

IO Functions

Normal IO Operation:

If set to input, the logic level of the signal present at the GPIOx pin can be read from *gpioX_in*. If the output mode is chosen, *gpioX_out* specifies the logic level of the GPIOx pin.

This mode is also used for the on/off control of the DCDC and LDOs. The selection which regulator is controlled by which GPIO, is done with the *gpio_ctrl_sdX* or *gpio_ctrl_ldoX* bits. The *gpioX_mode* should be set to input.

Interrupt Output

GPIOx pin logic state is derived from the interrupt signal XINT. Whenever an interrupt is present the GPIOx pin will be pulled high.
The *gpioX_mode* should be set to output.

VSUP_low Output

GPIOx pin will go high if V_{SUP} falls below ResVoltFall and SupResEn = 0.
The *gpioX_mode* should be set to output.

GPIO Interrupt Input

A falling or rising edge will set the *gpio_int* bit.
The *gpioX_mode* should be set to input.

Vselect Input

As long as the GPIOx pin is high the DCDC/LDOs operate with the normal register settings. If the GPIOx pin goes low the settings will change to the ones stored in *regX_voltage*.
The *gpioX_mode* should be set to input.

Figure 42:
GPIO Vselect Modes

gpio1_iosf	gpio2_iosf	Vselect mode
<> 5	<> 5	No voltage select by GPIO for regulator
<> 5	5	GPIO2 controls regulator selected by *reg1_select* and *reg2_select*
5	<> 5	GPIO1 controls regulator selected by *reg1_select* and *reg2_select*
5	5	GPIO1 controls regulator selected by *reg1_select* GPIO2 controls regulator selected by *reg2_select*

IO Functions: Shows the 4 different Vselect modes, depending on the setting of gpioX_iosf

Stand-by and Vselect Input

This mode is very similar to the Vselect mode described in the previous paragraph. In addition to switch between 2 register settings of 2 regulators the chip is set into stand-by mode when the GPIOx pin goes low and wakes up again when the pin is pulled high.
The *gpioX_mode* should be set to input.

GPIO1 and GPIO2 may be used to control two regulators separately.

Figure 43:
Stand-by and Vselect Modes

gpio1_iosf	gpio2_iosf	Vselect Mode	Stand-by Control
<> 6	<> 6	no voltage select by GPIO for regulator	No
<> 6	6	GPIO2 controls regulator selected by *reg1_select* and *reg2_select*	Yes
6	<> 6	GPIO1 controls regulator selected by *reg1_select* and *reg2_select*	Yes
6	6	GPIO1 controls regulator selected by *reg1_select* GPIO2 controls regulator selected by *reg2_select*	Yes

IO Functions: Shows the 4 different Vselect and Stand-by control modes, depending on the setting of gpioX_iosf

PWRGOOD Output

This signal will go high at the end of the start-up sequence. This can be used as a second reset signal to the processor to e.g. start oscillators.
The *gpioX_mode* should be set to output.

Supervisor

All Step-Down DCDCs have an integrated over-current protection.
An over-temperature protection of the chip is also integrated which can be switched on with the serial interface signal *temp_pmc_on* (enabled by default; it is not recommended to disable the over-temperature protection).

Temperature Supervision

The chip has two signals for the serial interface: *ov_temp_110* and *ov_temp_140*.
The flag *ov_temp_110* is automatically reset if the overtemperature condition is removed, whereas *ov_temp_140* has to be reset by the serial interface with the signal *rst_ov_temp_140*. If the flag *ov_temp_140* is set, an automatic reset of the complete chip is initiated. The chip will only start-up when the temperature falls below the T110 level (including hysteresis). The flag *ov_temp_140* is not affected by this reset cycle allowing the software to detect the reason for this unexpected shutdown.

Figure 44:
Over-Temperature Protection

Symbol	Parameter	Min	Typ	Max	Unit
T_{110}	ov_temp_110 rising threshold	95	110	125	°C
T_{140}	ov_temp_140 rising threshold	125	140	155	°C
T_{HYST}	ov_temp_110 and ov_temp_140 hysteresis		5		°C

Interrupt Generation

The interrupt controller generates an interrupt request for the host controller as soon as one or more of the bits in the *Interrupt* 1…2 register are set by pulling low pin XINT (XINT has to be selected as a GPIO output function). All the interrupt sources can be enabled in the Interrupt Mask 1…2 register. The Interrupt 1…2 registers are cleared automatically after the host controller has read them. To prevent the AS3709 device from losing an interrupt event, the register that is read is captured before it is transmitted to the host controller via the serial interface. As soon as the transmission of the captured value is complete a logical AND operation with the bit wise inverted captured value is applied to the register to clear all interrupt bits that have already been transmitted. Clearing the read interrupt bits takes 2 clock cycles, a read access to the same register before the clearing process has completed will yield a value of '0'. Note that an interrupt that has been present at the previous read access will be cleared as well in case it occurs again before the clearing process has completed.

During a read access to one of the interrupt registers, the GPIO pin (GPIO output function) will be released. As soon as the transferred bits of the interrupt register have been cleared the GPIO pin (GPIO output function) will be pulled low in case a new interrupt has occurred in the meantime. By doing so, the interrupt controller will work correctly with host controllers that are edge- and level-sensitive on their interrupt request input. Multiple byte read access is recommended to avoid reading the *Interrupt 1* register over and over again in response to a new interrupt that has occurred in the same register (and thus pulling low the GPIO pin) before the Interrupt 2 register has been read.

2-Wire-Serial Control Interface

Feature List

- Fast-mode capability (max. SCL-frequency is 400 kHz)
- 7+1-bit addressing mode
- 60h x 8-bit data registers (word address 0x00 - 0x60)
- Write formats: Single-Byte-Write, Page-Write
- Read formats: Current-Address-Read, Random-Read, Sequential-Read
- SDA input delay and SCL spike filtering by integrated RC-components

I²C Protocol

Figure 45:
2-Wire Serial Symbol Definition

Symbol	Definition	RW	Note
S	Start condition after Stop	R	1 bit
Sr	Repeated Start	R	1 bit
DW	Device address for Write	R	1000 0010b (80h)
DR	Device address for Read	R	1000 0011b (81h)
WA	Word address	R	8 bit
A	Acknowledge	W	1 bit
N	No Acknowledge	R	1 bit
reg_data	Register data/write	R	8 bit
data (n)	Register data/read	W	8 bit
P	Stop condition	R	1 bit
WA++	Increment word address internally	R	During acknowledge
	AS3709 (= slave) receive data		
	AS3709 (= slave) transmits data		

I²C Write Access

Byte Write and Page Write formats are used to write data to the slave.

Figure 46:
I²C Byte Write

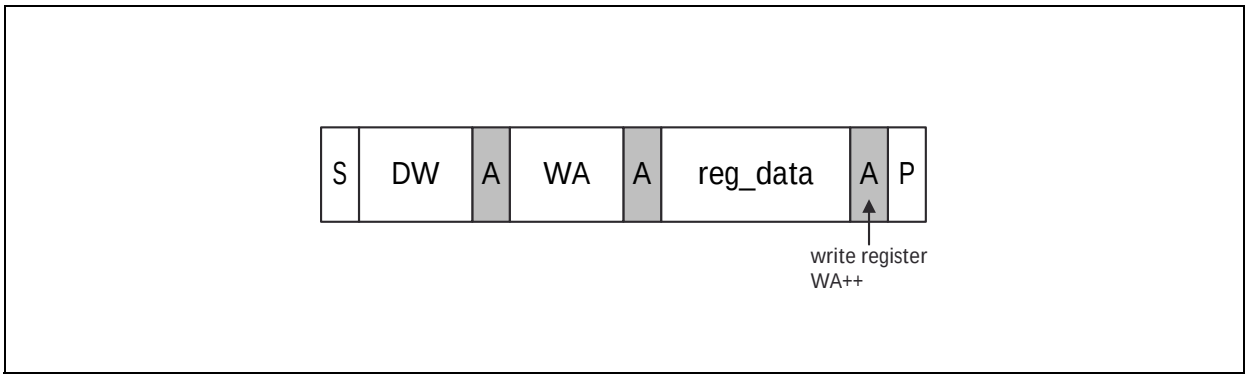
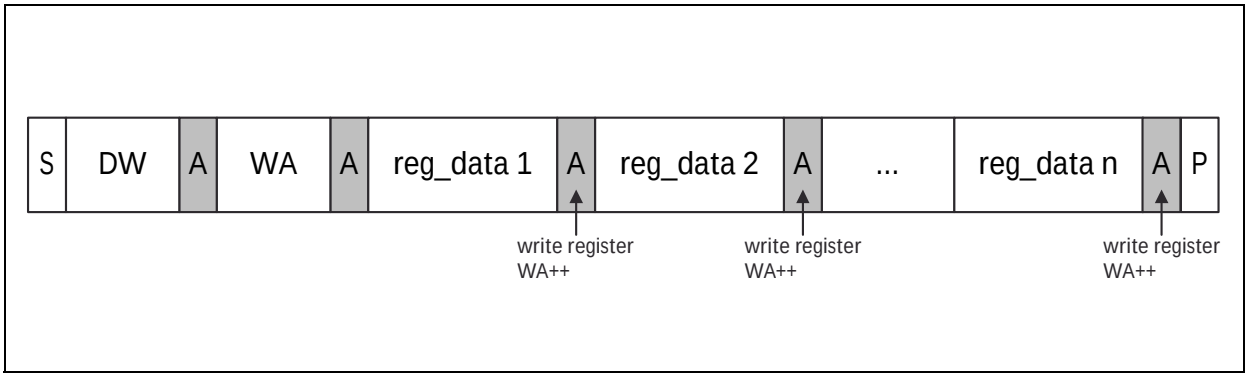


Figure 47:
I²C Page Write



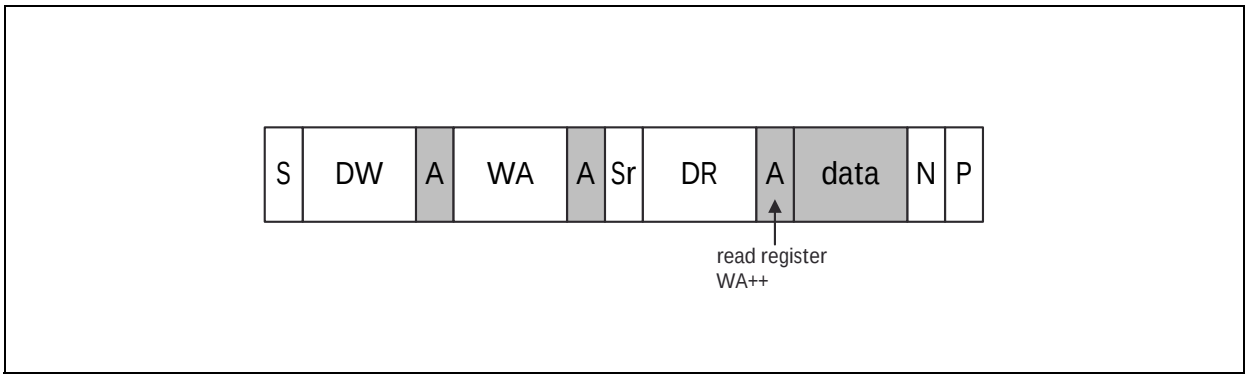
The transmission begins with the START condition, which is generated by the master when the bus is in IDLE state (the bus is free). The device-write address is followed by the word address. After the word address any number of data bytes can be sent to the slave. The word address is incremented internally, in order to write subsequent data bytes on subsequent address locations.

For reading data from the slave device, the master has to change the transfer direction. This can be done either with a repeated START condition followed by the device-read address, or simply with a new transmission START followed by the device-read address, when the bus is in IDLE state. The device-read address is always followed by the 1st register byte transmitted from the slave. In Read Mode any number of subsequent register bytes can be read from the slave. The word address is incremented internally.

I²C Read Access

Random, Sequential and Current Address Read are used to read data from the slave.

Figure 48:
I²C Random Read

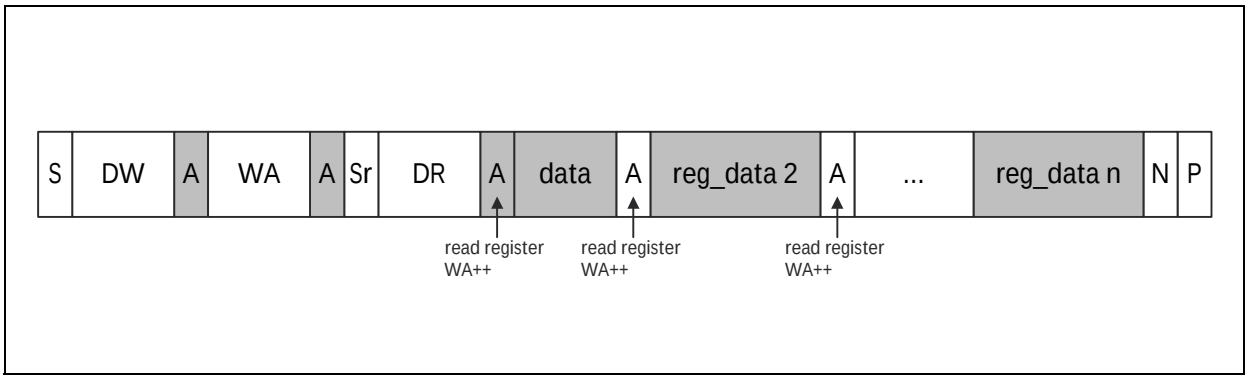


Random Read and Sequential Read are combined formats. The repeated START condition is used to change the direction after the data transfer from the master.

The word address transfer is initiated with a START condition issued by the master while the bus is idle. The START condition is followed by the device-write address and the word address.

In order to change the data direction a repeated START condition is issued on the 1st SCL pulse after the acknowledge bit of the word address transfer. After the reception of the device-read address, the slave becomes the transmitter. In this state the slave transmits register data located by the previous received word address vector. The master responds to the data byte with a not-acknowledge, and issues a STOP condition on the bus.

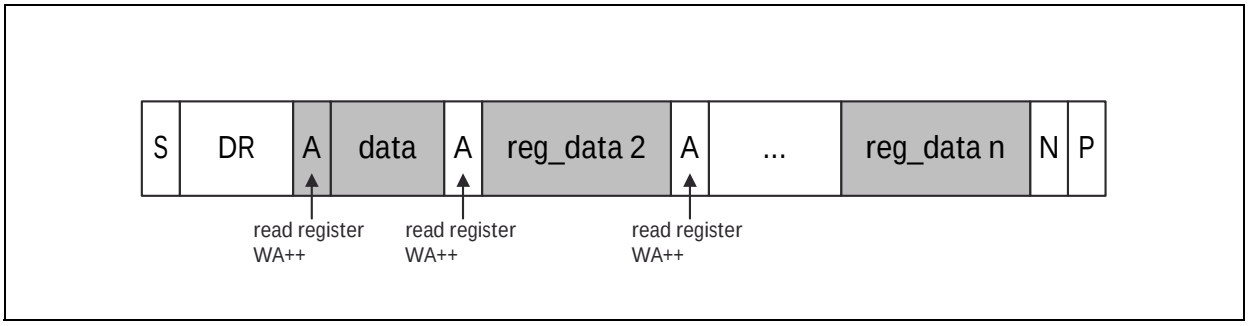
Figure 49:
I²C Sequential Read



Sequential Read is the extended form of Random Read, as more than one register-data bytes are transferred subsequently. In difference to the Random Read, for a sequential read the transferred register-data bytes are responded by an acknowledge from the master. The number of data bytes transferred in one sequence is unlimited (consider the behavior

of the word-address counter). To terminate the transmission the master has to send a not-acknowledge following the last data byte and generate the STOP condition subsequently.

Figure 50:
I²C Current Address Read



To keep the access time as small as possible, this format allows a read access without the word address transfer in advance to the data transfer. The bus is idle and the master issues a START condition followed by the Device-Read address. Analogous to Random Read, a single byte transfer is terminated with a not-acknowledge after the 1st register byte. Analogous to Sequential Read an unlimited number of data bytes can be transferred, where the data bytes has to be responded with an acknowledge from the master. For termination of the transmission the master sends a not-acknowledge following the last data byte and a subsequent STOP condition.

I²C Parameter

Figure 51:
I²C SDA/SCL Characteristics

Symbol	Parameter	Min	Typ	Max	Unit
V_{IL}	SCL,SDA Low Level input voltage			0.4	V
V_{IH}	SCL,SDA High Level input voltage	1.4			V

Register Description

Figure 52:
Register Overview

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
00h	SD1Voltage	sd1_frequ	sd1_vsel<6:0>						
01h	SD2Voltage	sd2_frequ	sd2_vsel<6:0>						
02h	SD3Voltage	sd3_frequ	sd3_vsel<6:0>						
03h	SD4Voltage	sd4_frequ	sd4_vsel<6:0>						
04h	SD5Voltage	sd5_frequ	sd5_vsel<6:0>						
05h	LDO1Voltage	ldo1_ilimit	ldo1_vsel<6:0>						
06h	LDO2Voltage	ldo2_ilimit	ldo2_vsel<6:0>						
0ch	GPIO1control	gpio1_invert	gpio1_iosf<6:3>				gpio1_mode<2:0>		
0dh	GPIO2control	gpio2_invert	gpio2_iosf<6:3>				gpio2_mode<2:0>		
10h	SDcontrol	-	ldo2_enable	ldo1_enable	sd5_enable	sd4_enable	sd3_enable	sd2_enable	sd1_enable
20h	GPIOsignal_out	-				-	-	gpio2_out	gpio1_out
21h	GPIOsignal_in	-				-	-	gpio2_in	gpio1_in
22h	Reg1_Voltage	reg1_voltage<7:0>							
23h	Reg2_Voltage	reg2_voltage<7:0>							
24h	Reg_control	reg2_select<7:4>				reg1_select<3:0>			
25h	GPIOctrl_sd	gpio_ctrl_sd4<7:6>		gpio_ctrl_sd3<5:4>		gpio_ctrl_sd2<3:2>		gpio_ctrl_sd1<1:0>	

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
26h	GPIOctrl_ldo	-	-	gpio_ctrl_ldo2<5:4>		gpio_ctrl_ldo1<3:2>		gpio_ctrl_sd5<1:0>	
29h	SD_control3	sd5_slave	sd4_slave	sd2_slave	sd5_fsel	sd5_fast	sd5_low_noise	-	
30h	SD_control1	sd4_low_noise	sd3_low_noise	sd2_low_noise	sd1_low_noise	sd4_fast	sd3_fast	sd2_fast	sd1_fast
31h	SD_control2	sd_dvm_select<7:6>		dvm_time<5:4>		sd4_fsel	sd3_fsel	sd2_fsel	sd1_fsel
32h	Supply_voltage_monitor	FastResEn	SupResEn	ResVoltFall<5:3>			ResVoltRise<2:0>		
33h	Startup_control	-						reslevel_5v	power_off_at_vsuplow
34h	ResetTimer	-	stby_reset_disable	auto_off	off_delay<4:3>		res_timer<2:0>		
35h	ReferenceControl	on_reset_delay	-	clk_div2	standby_mode_on	clk_int<3:1>			low_power_on
36h	ResetControl	onkey_reset	reset_reason<6:3>				on_input	power_off	force_reset
37h	OvertemperatureControl	tco_140_a	tco_110_a	temp_test<5:4>		rst_ov_temp_140	ov_temp_140	ov_temp_110	temp_pmc_on
39h	Reg_standby_mod1	disable_regpd	ldo2_stby_on	ldo1_stby_on	sd5_stby_on	sd4_stby_on	sd3_stby_on	sd2_stby_on	sd1_stby_on
73h	RegStatus	-			sd5_lv	sd4_lv	sd3_lv	sd2_lv	sd1_lv
74h	InterruptMask1	LowVsup_int_m	ovtmp_int_m	onkey_int_m	sd5_lv_int_m	sd4_lv_int_m	sd3_lv_int_m	sd2_lv_int_m	sd1_lv_int_m
75h	InterruptMask2	-						gpio_restart_int_m	gpio_int_m

Addr	Name	<D7>	<D6>	<D5>	<D4>	<D3>	<D2>	<D1>	<D0>
77h	InterruptStatus1	LowBat_int_i	ovtmp_int_i	onkey_int_i	sd5_lv_int_i	sd4_lv_int_i	sd3_lv_int_i	sd2_lv_int_i	sd1_lv_int_i
78h	InterruptStatus2	-						gpio_restart_int_i	gpio_int_i
90h	ASIC_ID1	asic_id1<7:0>							
91h	ASIC_ID2	fab_id<7:4>				revision<3:0>			

Detailed Register Description

Figure 53:
SD1Voltage Register (Address 00h)

Addr: 00h		SD1Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd1_frequ	0	RW	Selects between high and low frequency dependent on *sd1_fsel* **0 :** 2MHz if sd1_fsel=0, 3MHz if sd1_fsel=1 **1 :** 3MHz if sd1_fsel=0, 4MHz if sd1_fsel=1
6:0	sd1_vsel	'b0000000	RW	The voltage select bits set the SD1 output voltage level and power the SD1 converter down. **00h :** SD1 powered down **01h-40h :** V_SD1=0.6V+sd1_vsel*12.5mV **41h-70h :** V_SD1=1.4V+(sd1_vsel-40h)*25mV **71h-7Fh :** V_SD1=2.6V+(sd1_vsel-70h)*50mV

Figure 54:
SD2Voltage Register (Address 01h)

Addr: 01h		SD2Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd2_frequ	0	RW	Selects between high and low frequency dependent on *sd2_fsel* **0 :** 2MHz if sd2_fsel=0, 3MHz if sd2_fsel=1 **1** : 3MHz if sd2_fsel=0, 4MHz if sd2_fsel=1
6:0	sd2_vsel	'b000 0000	RW	The voltage select bits set the SD2 output voltage level and power the SD2 converter down. **00h :** SD2 powered down **01h-40h :** V_SD2=0.6V+sd2_vsel*12.5mV **41h-70h :** V_SD2=1.4V+(sd2_vsel-40h)*25mV **71h-7Fh :** V_SD2=2.6V+(sd2_vsel-70h)*50mV

Figure 55:
SD3Voltage Register (Address 02h)

Addr: 02h		SD3Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd3_frequ	0	RW	Selects between high and low frequency dependent on *sd3_fsel* **0 :** 2MHz if sd3_fsel=0, 3MHz if sd3_fsel=1 **1 :** 3MHz if sd3_fsel=0, 4MHz if sd3_fsel=1
6:0	sd3_vsel	'b000 0000	RW	The voltage select bits set the SD3 output voltage level and power the SD3 converter down. **00h :** SD3 powered down **01h-40h :** V_SD3=0.6V+sd3_vsel*12.5mV **41h-70h :** V_SD3=1.4V+(sd3_vsel-40h)*25mV **71h-7Fh :** V_SD3=2.6V+(sd3_vsel-70h)*50mV

Figure 56:
SD4Voltage Register (Address 03h)

Addr: 03h		SD4Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd4_frequ	0	RW	Selects between high and low frequency dependent on *sd4_fsel* **0 :** 2MHz if sd3_fsel=0, 3MHz if sd3_fsel=1 **1 :** 3MHz if sd3_fsel=0, 4MHz if sd3_fsel=1
6:0	sd4_vsel	'b000 0000	RW	The voltage select bits set the SD4 output voltage level and power the SD4 converter down. **00h :** SD4 powered down **01h-40h :** V_SD4=0.6V+sd4_vsel*12.5mV **41h-70h :** V_SD4=1.4V+(sd4_vsel-40h)*25mV **71h-7Fh :** V_SD4=2.6V+(sd4_vsel-70h)*50mV

Figure 57:
SD5Voltage Register (Address 04h)

Addr: 04h		SD5Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd5_frequ	0	RW	Selects between high and low frequency dependent on *sd5_fsel* **0 :** 2MHz if sd3_fsel=0, 3MHz if sd3_fsel=1 **1 :** 3MHz if sd3_fsel=0, 4MHz if sd3_fsel=1
6:0	sd5_vsel	'b000 0000	RW	The voltage select bits set the SD5 output voltage level and power the SD5 converter down. **00h :** SD5 powered down **01h-40h :** V_SD4=0.6V+sd4_vsel*12.5mV **41h-70h :** V_SD4=1.4V+(sd4_vsel-40h)*25mV **71h-7Fh :** V_SD4=2.6V+(sd4_vsel-70h)*50mV

Figure 58:
LDO1Voltage Register (Address 05h)

Addr: 05h		LDO1Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo1_ilimit	0	RW	Sets limit of LDO1 **0 :** 150mA operating range **1 :** 300mA operating range
6:0	ldo1_vsel	'b00 0000	RW	The voltage select bits set the LDO1 output voltage 0.825V...3.3V, 25mV steps **00h :** LDO1 off **01h-24h :** V_LDO1=0.8V+ldo1_vsel*25mV **25h-3fh :** Do not use **40h-7Fh :** V_LDO1=1.725V+(ldo1_vsel-40h)*25mV

Figure 59:
LDO2Voltage Register (Address 06h)

Addr: 06h		LDO2Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	ldo2_ilimit	0	RW	Sets limit of LDO2 **0 :** 150mA operating range **1 :** 300mA operating range
8:0	ldo2_vsel	'b00 0000	RW	The voltage select bits set the LDO2 output voltage 0.825V...3.3V, 25mV steps **00h :** LDO2 off **01h-24h :** V_LDO2=0.8V+ldo2_vsel*25mV **25h-3fh :** Do not use **40h-7Fh :** V_LDO2=1.725V+(ldo2_vsel-40h)*25mV

Figure 60:
GPIO1control Register (Address 0ch)

Addr: 0ch		GPIO1control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio1_invert	0	RW	Invert GPIO1 input/output **0 :** Normal mode **1 :** Invert input or output
6:3	gpio1_iosf	'b0000	RW	Select the GPIO1 special function **0 :** Normal I/O operation **1 :** Interrupt output **2 :** VSUP_low output **3 :** GPIO interrupt input **4 :** NA **5 :** Vselect input, (apply on reg1_select and reg2_select, if gpio2_iosf =5 then apply on reg1_select only) **6 :** standby + Vselect + restart interrupt input **7 :** pwr_good output **8 :** NA **9 :** NA **10 :** NA **11 :** NA **12 :** NA **13 :** NA **14 :** NA **15 :** NA
2:0	gpio1_mode	'b011	RW	Selects the GPIO1 mode (I, I/O, Tri, Pulls) **0 :** Input **1 :** Output (push and pull) **2 :** IO (open drain, only NMOS is active) **3 :** NA **4 :** Input with pullup **5 :** Input with pulldown **6 :** IO (open drain (NMOS) with pullup) **7 :** NA

Figure 61:
GPIO2control Register (Address 0dh)

Addr: 0dh		GPIO2control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	gpio2_invert	0	RW	Invert GPIO2 input/output **0 :** Normal mode **1 :** Invert input or output
6:3	gpio2_iosf	'b0000	RW	Select the GPIO2 special function **0 :** Normal i/o operation **1 :** Interrupt output **2 :** VSUP_low output **3 :** GPIO interrupt input **4 :** NA **5 :** Vselect input, (apply on reg1_select and reg2_select, if gpio1_iosf=5 then apply on reg2_select only) **6 :** standby + Vselect + restart interrupt input **7 :** pwr_good output **8 :** NA **9 :** NA **10 :** NA **11 :** NA **12 :** NA **13 :** NA **14 :** NA **15 :** NA
2:0	gpio2_mode	'b011	RW	Selects the GPIO2 mode (I, I/O, Tri, Pulls) **0 :** Input **1 :** Output (push and pull) **2 :** IO (open drain, only NMOS is active) **3 :** NA **4 :** Input with pullup **5 :** Input with pulldown **6 :** IO (open drain (NMOS) with pullup) **7 :** NA

Figure 62:
SDcontrol Register (Address 10h)

Addr: 10h		SDcontrol		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	'b0	N/A	Do not use
6	ldo2_enable	'b1	RW	Global LDO2 enable **0 :** LDO2 off **1 :** LDO2 on
5	ldo1_enable	'b1	RW	Global LDO1 enable **0 :** LDO1 off **1 :** LDO1 on
4	sd5_enable	'b1	RW	Global stepdown5 enable **0 :** SD off **1 :** SD on
3	sd4_enable	'b1	RW	Global stepdown4 enable **0 :** SD off **1 :** SD on
2	sd3_enable	'b1	RW	Global stepdown3 enable **0 :** SD off **1 :** SD on
1	sd2_enable	'b1	RW	Global stepdown2 enable **0 :** SD off **1 :** SD on
0	sd1_enable	'b1	RW	Global stepdown1 enable **0 :** SD off **1 :** SD on

Figure 63:
GPIOsignal_out Register (Address 20h)

Addr: 20h		GPIOsignal_out		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	-	'b0000	N/A	Do not use
1	gpio2_out	0	RW	This bit determines the output signal of the GPIO2 pin when selected as output source.
0	gpio1_out	0	RW	This bit determines the output signal of the GPIO1 pin when selected as output source.

Figure 64:
GPIOsignal_in Register (Address 21h)

Addr: 21h		GPIOsignal_in		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	-	'b0000	N/A	Do not use
1	gpio2_in	0	RO	This bit reflects the logic level of the GPIO2 pin when configured as digital input pin.
0	gpio1_in	0	RO	This bit reflects the logic level of the GPIO1 pin when configured as digital input pin.

Figure 65:
Reg1_Voltage Register (Address 22h)

Addr: 22h		Reg1_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reg1_voltage	'b0000 0000	RW	This register is mapped to the register address 0h+Reg1_select , if gioX_iosf = 5 or 6 (Vselect input), and input = 1. This feature allows voltage switching of a predefined regulator with just one GPIO input. **0 ..FFh :** Selects voltage and frequency bits of DCDC

Figure 66:
Reg2_Voltage Register (Address 23h)

Addr: 23h		Reg2_Voltage		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:0	reg2_voltage	'b0000 0000	RW	This register is mapped to the register address 0h+Reg1_select, if gioX_iosf=5 or 6 (Vselect input), and input = 1, This feature allows voltage switching of a predefined regulator with just one GPIO input **0 ..FFh :** Selects voltage and frequency bits of DCDC

Figure 67:
Reg_control Register (Address 24h)

Addr: 24h		Reg_control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	reg2_select	'b1111	RW	Selects regulator for mapping feature; if reg_select2 ≥ 0Ch, then feature is disabled.
3:0	reg1_select	'b1111	RW	Selects regulator for mapping feature; if reg_select1 ≥ 0Ch, then feature is disabled.

Figure 68:
GPIOctrl_sd Register (Address 25h)

Addr: 25h		GPIOctrl_sd		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	gpio_ctrl_sd4	'b00	RW	Enable GPIO control of DCDC SD4. GPIO ctrl only enabled, if sd4_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** NA
5:4	gpio_ctrl_sd3	'b00	RW	Enable GPIO control of DCDC SD3. GPIO ctrl only enabled, if sd3_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** NA
3:2	gpio_ctrl_sd2	'b00	RW	Enable GPIO control of DCDC SD2. GPIO ctrl only enabled, if sd2_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** NA
1:0	gpio_ctrl_sd1	'b00	RW	Enable GPIO control of DCDC SD1. GPIO ctrl only enabled, if sd1_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** NA

Figure 69:
GPIOctrl_ldo Register (Address 26h)

Addr: 26h		GPIOctrl_ldo		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	-	'b00	N/A	-
5:4	gpio_ctrl_ldo2	'b00	RW	Enable GPIO control of LDO2. GPIO ctrl only enabled, if ldo2_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** NA
3:2	gpio_ctrl_ldo1	'b00	RW	Enable GPIO control of LDO1. GPIO ctrl only enabled, if ldo1_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** NA
1:0	gpio_ctrl_sd5	'b00	RW	Enable GPIO control of SD5. GPIO ctrl only enabled, if sd5_vsel > 0 **0 :** No GPIO control **1 :** Controlled by GPIO1 **2 :** Controlled by GPIO2 **3 :** NA

Figure 70:
SD_control3 Register (Address 29h)

Addr: 29h		SD_control3		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd5_slave	0	RW	Enables slave mode of SD5 **0 :** Normal mode of SD5 **1 :** SD5 is slave of SD3
7	sd4_slave	0	RW	Enables slave mode of SD4 **0 :** Normal mode of SD4 **1 :** SD4 is slave of SD3
5	sd2_slave	0	RW	Enables slave mode of SD2 **0 :** Normal mode of SD2 **1 :** SD2 is slave of SD1
4	sd5_fsel	0	RW	Selects between high and low frequency range **0 :** 2 or 3MHz frequency (selectable by sd5_frequ) **1 :** 3 or 4MHz frequency (selectable by sd5_frequ)
3	sd5_fast	0	RW	Selects a faster regulation mode for SD5 suitable for larger load changes. **0 :** Normal mode, Cext=10µF **1 :** Fast mode, Cext=22µF required
2	sd5_low_noise	0	RW	Enables low noise mode of SD5. If enabled smaller current pulses and output ripple is activated. **0 :** Normal mode. Minimum current pulses of >100mA applied in skip mode. **1 :** Low noise mode. Only minimum on time applied in skip mode.
1:0	-	'b00	N/A	-

Figure 71:
SD_control1 Register (Address 30h)

Addr: 30h		SD_control1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	sd4_low_noise	0	RW	Enables low noise mode of SD4. If enabled smaller current pulses and output ripple is activated. **0 :** Normal mode. Minimum current pulses of >100mA applied in skip mode. **1 :** Low noise mode. Only minimum on time applied in skip mode.
6	sd3_low_noise	0	RW	Enables low noise mode of SD3. If enabled smaller current pulses and output ripple is activated. **0 :** Normal mode. Minimum current pulses of >100mA applied in skip mode. **1 :** Low noise mode. Only minimum on time applied in skip mode.
5	sd2_low_noise	0	RW	Enables low noise mode of SD2. If enabled smaller current pulses and output ripple is activated. **0 :** Normal mode. Minimum current pulses of >100mA applied in skip mode. **1 :** Low noise mode. Only minimum on time applied in skip mode.
4	sd1_low_noise	0	RW	Enables low noise mode of SD1. If enabled smaller current pulses and output ripple is activated. **0 :** Normal mode. Minimum current pulses of >100mA applied in skip mode. **1 :** Low noise mode. Only minimum on time applied in skip mode.
3	sd4_fast	0	RW	Selects a faster regulation mode for SD4 suitable for larger load changes. **0 :** Normal mode, Cext=10µF **1 :** Fast mode, Cext=22µF required
2	sd3_fast	0	RW	Selects a faster regulation mode for SD3 suitable for larger load changes. **0 :** normal mode, Cext=10µF **1 :** fast mode, Cext=22µF required
1	sd2_fast	0	RW	Selects a faster regulation mode for SD2 suitable for larger load changes. **0 :** Normal mode, Cext=10µF **1 :** Fast mode, Cext=22µF required
0	sd1_fast	0	RW	Selects a faster regulation mode for SD1 suitable for larger load changes. **0 :** Normal mode, Cext=10µF **1 :** Fast mode, Cext=22µF required

Figure 72:
SD_control2 Register (Address 31h)

Addr: 31h		SD_control2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:6	sd_dvm_select	'b00	RW	Apply DVM counter to the following DCDC converter **0 :** Select SD1 for DVM **1 :** Select SD2 for DVM **2 :** Select SD3 for DVM **3 :** Select SD5 for DVM
5:4	dvm_time	'b00	RW	Time steps of DVM voltage change of selected step down, if voltage of step Down is changed during operation (sdx_vsel) voltage is decreased/increased by single steps 12.5mV **0 :** 0 µsec, immediate change (no DVM) **1 :** 4 µsec time delay between steps **2 :** 8 µsec time delay between steps **3 :** 16 µsec time delay between steps
3	sd4_fsel	0	RW	Selects between high and low frequency range **0 :** 2 or 3MHz frequency (selectable by sd4_frequ) **1 :** 3 or 4MHz frequency (selectable by sd4_frequ)
2	sd3_fsel	0	RW	Selects between high and low frequency range **0 :** 2 or 3MHz frequency (selectable by sd3_frequ) **1 :** 3 or 4MHz frequency (selectable by sd3_frequ)
1	sd2_fsel	0	RW	Selects between high and low frequency range **0 :** 2 or 3MHz frequency (selectable by sd2_frequ) **1 :** 3 or 4MHz frequency (selectable by sd2_frequ)
0	sd1_fsel	0	RW	Selects between high and low frequency range **0 :** 2 or 3MHz frequency (selectable by sd1_frequ) **1 :** 3 or 4MHz frequency (selectable by sd1_frequ)

Figure 73:
Supply_voltage_monitor Register (Address 32h)

Addr: 32h		Supply_voltage_monitor		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	FastResEn	0	RW	**0 :** ResVoltFall debounce time = 3msec **1 :** ResVoltFall debounce time = 4µsec (tbd)
6	SupResEn	0	RW	**0 :** A reset is generated if V_{SUP} falls below 2.7V ** **1 :** A reset is generated if V_{SUP} falls below ResVoltFall ** If V_{SUP} falls below ResVoltFall only an interrupt is generated (if enabled) and the µProcessor can shut down the system
5:3	ResVoltFall	'b000	RW	This value determines the reset level ResVoltFall for falling V_{SUP}. It is recommended to set this value at least 200mV lower than ResVoltRise (the levels differ between 3.3V and 5V supply) **0 :** 2.7V / 3.6V **1 :** 2.8V / 3.7V **2 :** 2.9V / 3.8V **3 :** 3.0V / 3.9V **4 :** 3.1V / 4.0V **5 :** 3.2V / 4.1V **6 :** 3.3V / 4.2V **7 :** 3.4V / 4.4V
2:0	ResVoltRise	'b000	RO (OTP)	This value determines the reset level ResVoltRise for rising V_{SUP}. It is recommended to set this value at least 200mV higher than ResVoltFall (the levels differ between 3.3V and 5V supply) **0 :** 2.7V / 3.6V **1 :** 2.8V / 3.7V **2 :** 2.9V / 3.8V **3 :** 3.0V / 3.9V **4 :** 3.1V / 4.0V **5 :** 3.2V / 4.1V **6 :** 3.3V / 4.2V **7 :** 3.4V / 4.4V

Figure 74:
Startup_Control Register (Address 33h)

Addr: 33h		Startup_Control		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	-	'b000 0000	N/A	Do not use
1	reslevel_5v	0	RW	Selects the 5V supply reset level (see ResVoltRise and ResVoltFall) **0 :** 3.3V level **1 :** 5.0V level
0	power_off_ at_vsuplow	0	RW	Switch on Power off mode if low V_{SUP} is detected during active or standby mode (Pin ON= low and bit auto_off=0) **0 :** If low V_{SUP} is detected, V_{SUP} is continuously monitored and chip startup initiated if V_{SUP} is above ResVoltRise **1 :** If low V_{SUP} is detected, enter power off mode

Figure 75:
ResetTimer Register (Address 34h)

Addr: 34h		ResetTimer		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	-	'b0	N/A	Do not use
6	stby_reset_disable	0	RW	Disable Reset output signal (pin XRES) in standby mode. **0 :** Normal mode, reset is active in standby mode **1 :** No reset in standby mode and during exit of stand-by mode
5	auto_off	0	RO	Defines startup behavior at first V_{SUP} connection **0 :** Startup of chip if V_{SUP}>ResVoltRise **1 :** Enter power off mode (Startup with ON key)
4:3	off_delay	'b01	RW	Set delay between I^2C command, GPIO or Reset signal for power_off, standby mode or reset and execution of that command. **0 :** No delay **1 :** 8 msec **2 :** 16 msec **3 :** 32 msec
2:0	res_timer	'b000	RW	Set Reset Time, after the last regulator has started **0 :** RESTIME = 2ms **1 :** RESTIME = 4ms **2 :** RESTIME = 8ms **3 :** RESTIME = 16ms **4 :** RESTIME = 32ms **5 :** RESTIME = 64ms **6 :** RESTIME = 128ms **7 :** RESTIME = 160ms

Figure 76:
ReferenceControl Register (Address 35h)

Addr: 35h		ReferenceControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	on_reset_delay	0	RW	Sets the on reset delay time **0 :** 8 sec (if onkey_reset=1) **1 :** 4 sec (if onkey_reset=1)
6	-	0	RW	-
5	clk_div2	0	RW	Divide internal clock oscillator by 2 to reduce quiescent current for low power operation **0 :** Normal mode **1 :** Internal clock frequency divided by two. All timings are increased by two. Switching frequency of all DCDC converters are divided by two. Reduced transient performance of DCDC converters.
4	standby_mode_on	0	RW	Setting to 1 sets the PMU into standby mode. All regulators are disabled except those regulators enabled by register Reg standby mode. XRES will be pulled to low. A normal startup of all regulators will be done with any interrupt (has to be enabled before entering standby mode). During this startup, regulators defined by Reg standby mode register are continuously on.
3:1	clk_int	'b000	RW	Sets the internal CLK frequency f_{CLK} used for fuel gauge, DCDCs, PWM, ... **0 :** 4 MHz (default) **1 :** 3.8 MHz **2 :** 3.6 MHz **3 :** 3.4 MHz **4 :** 3.2 MHz **5 :** 3.0 MHz **6 :** 2.8 MHz **7 :** 2.6 MHz All frequencies, timings and delays in this datasheet are based on 4MHz clk_int
0	low_power_on	0	RW	Enable low power mode of internal reference. **0 :** Standard mode **1 :** Low power mode - all specification except noise parameters are still valid. Iq reduced by approx. 30µA

Figure 77:
ResetControl Register (Address 36h)

Addr: 36h		ResetControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	onkey_reset	0	RW	**0 :** Reset after 4/8 seconds ON pressed disabled **1 :** Reset after 4/8 seconds ON pressed enabled
6:3	reset_reason	'b0000	RW	Flags to indicate to the software the reason for the last reset **0 :** V_{POR} has been reached (V_{SUP} connection from scratch) **1 :** ResVoltFall was reached (V_{SUP} drop below 2.75V) **2 :** Software forced by force_reset **3 :** Software forced by power_off and ON was pulled high **4 :** Software forced by power_off and charger was detected **5 :** External triggered through the pin XRES **6 :** Reset caused by overtemperature T140 **7 :** NA **8 :** Reset caused by 4/8 seconds ON press **9 :** NA **10 :** NA **11 :** Reset caused by interrupt in standby mode **12 :** Reset caused by ON pulled high in standby mode
2	on_input	0	R_PUSH	**Read:** This flag represents the state of the ON pad directly **Write:** Setting to 1 resets the 4/8 sec. onkey_reset timer
1	power_off	0	RW	Setting to 1 starts a reset cycle, but waits after the Reg_off state for a falling edge on the pin ON
0	force_reset	0	RW	Setting to 1 starts a complete reset cycle

Figure 78:
OvertemperatureControl Register (Address 37h)

Addr: 37h		OvertemperatureControl		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:4	-	'b0000	N/A	Do not use
3	rst_ov_temp_140	0	RWP	If the over-temperature threshold 2 has been reached, the flag ov_temp_140 is set and a reset cycle is started. ov_temp_140 should be reset by writing 1 and afterward 0 to rst_ov_temp_140.
2	ov_temp_140	0	RO	Flag that the over-temperature threshold 2 (T140) has been reached - this flag is not reset by an over-temperature caused reset and has to be reset by rst_ov_temp_140.
1	ov_temp_110	0	RO	Flag that the over-temperature threshold 1 (T110) has been reached
0	temp_pmc_on	1	RO	Switch on / off the temperature supervision; default: on - all other bits are only valid if set to 1 leave at 1, do not disable

Figure 79:
Reg_standby_mod1 Register (Address 39h)

Addr: 39h		Reg_standby_mod1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	disable_regpd	0	RW	This bit disables the pulldown of all regulators **0 :** Normal operation approx. 1kΩ pulldown of all regulators **1 :** Pulldown disabled >100kΩ of all regulators
6	ldo2_stby_on	0	RW	Enable LDO2 in standby mode
5	ldo1_stby_on	0	RW	Enable LDO1 in standby mode
4	sd5_stby_on	0	RW	Enable Step down 4 in standby mode
3	sd4_stby_on	0	RW	Enable Step down 4 in standby mode
2	sd3_stby_on	0	RW	Enable Step down 3 in standby mode
1	sd2_stby_on	0	RW	Enable Step down 2 in standby mode
0	sd1_stby_on	0	RW	Enable Step down 1 in standby mode

Figure 80:
RegStatus Register (Address 73h)

Addr: 73h		RegStatus		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:5	-	'b000	N/A	Do not use
4	sd5_lv	0	RO	Bit is set when voltage of SD5 drops below low voltage threshold (-5%) (1msec debounce time default)
3	sd4_lv	0	RO	Bit is set when voltage of SD4 drops below low voltage threshold (-5%) (1msec debounce time default)
2	sd3_lv	0	RO	Bit is set when voltage of SD3 drops below low voltage threshold (-5%) (1msec debounce time default)
1	sd2_lv	0	RO	Bit is set when voltage of SD2 drops below low voltage threshold (-5%) (1msec debounce time default)
0	sd1_lv	0	RO	Bit is set when voltage of SD1 drops below low voltage threshold (-5%) (1msec debounce time default)

Figure 81:
InterruptMask1 Register (Address 74h)

Addr: 74h		InterruptMask1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LowVsup_int_m	1	RW	Set to 0 to enable the interrupt
6	ovtmp_int_m	1	RW	Set to 0 to enable the interrupt
5	onkey_int_m	1	RW	Set to 0 to enable the interrupt
4	sd5_lv_int_m	1	RW	Set to 0 to enable the interrupt
3	sd4_lv_int_m	1	RW	Set to 0 to enable the interrupt
2	sd3_lv_int_m	1	RW	Set to 0 to enable the interrupt
1	sd2_lv_int_m	1	RW	Set to 0 to enable the interrupt
0	sd1_lv_int_m	1	RW	Set to 0 to enable the interrupt

Figure 82:
InterruptMask2 Register (Address 75h)

Addr: 75h		InterruptMask2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	-	'b0000 00	N/A	Do not use
1	gpio_restart_int_m	1	RW	Set to 0 to enable the interrupt
0	gpio_int_m	1	RW	Set to 0 to enable the interrupt

Figure 83:
InterruptStatus1 Register (Address 77h)

Addr: 77h		InterruptStatus1		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7	LowBat_int_i	0	POP	Bit is set when V_{SUP} drops below vres_fall rising edge only
6	ovtmp_int_i	0	POP	Bit is set when 110deg is exceeded rising edge only
5	onkey_int_i	0	POP	Rising and falling edge
4	sd5_lv_int_i	0	POP	Rising edge only
3	sd4_lv_int_i	0	POP	Rising edge only
2	sd3_lv_int_i	0	POP	Rising edge only
1	sd2_lv_int_i	0	POP	Rising edge only
0	sd1_lv_int_i	0	POP	Rising edge only

Figure 84:
InterruptStatus2 Register (Address 78h)

Addr: 78h		InterruptStatus2		
Bit	**Bit Name**	**Default**	**Access**	**Bit Description**
7:2	-	'b0000 00	N/A	Do not use
1	gpio_restart_int_i	0	POP	Falling edge
0	gpio_int_i	0	POP	Rising and falling edge

Figure 85:
ASIC_ID1 Register (Address 90h)

Addr: 90h		ASIC_ID1		
Bit	Bit Name	Default	Access	Bit Description
7:0	ID1	'b10001110	RO	-

Figure 86:
ASIC_ID2 Register (Address 91h)

Addr: 91h		ASIC_ID2		
Bit	Bit Name	Default	Access	Bit Description
3:0	revision	'b0010	RO	Note: Metal fuse!!!

Application Information

Figure 87:
Application Schematic

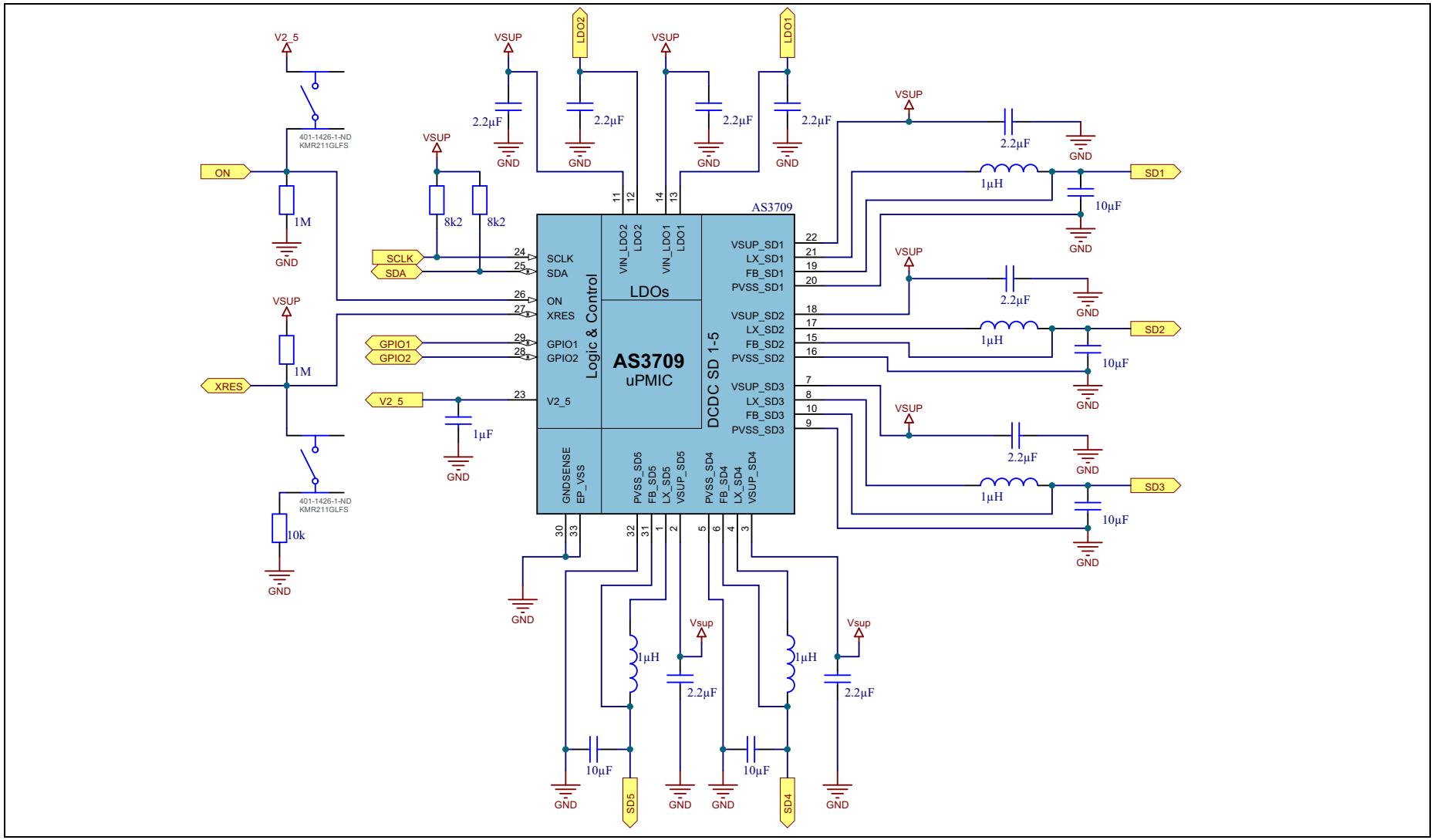
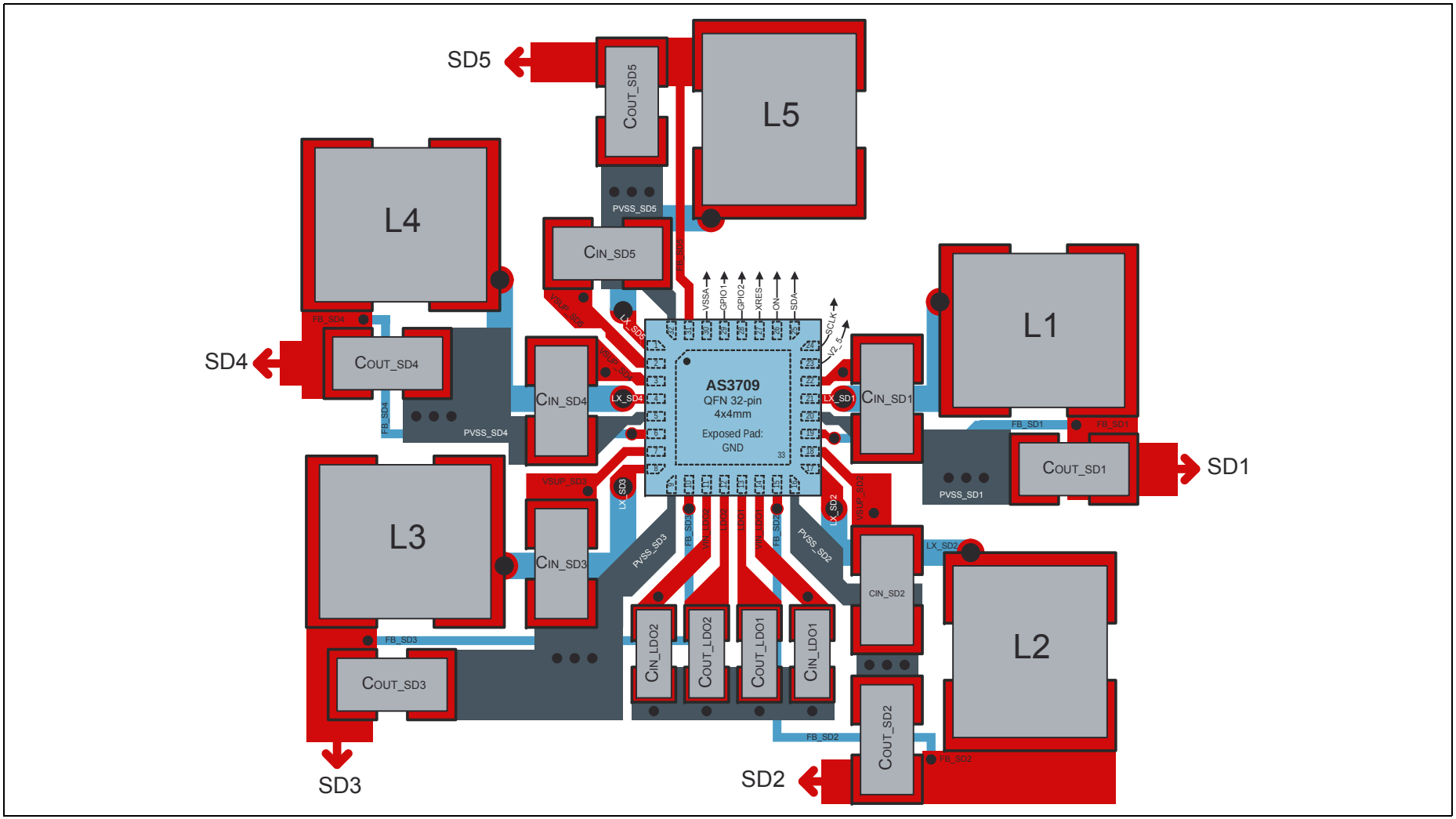


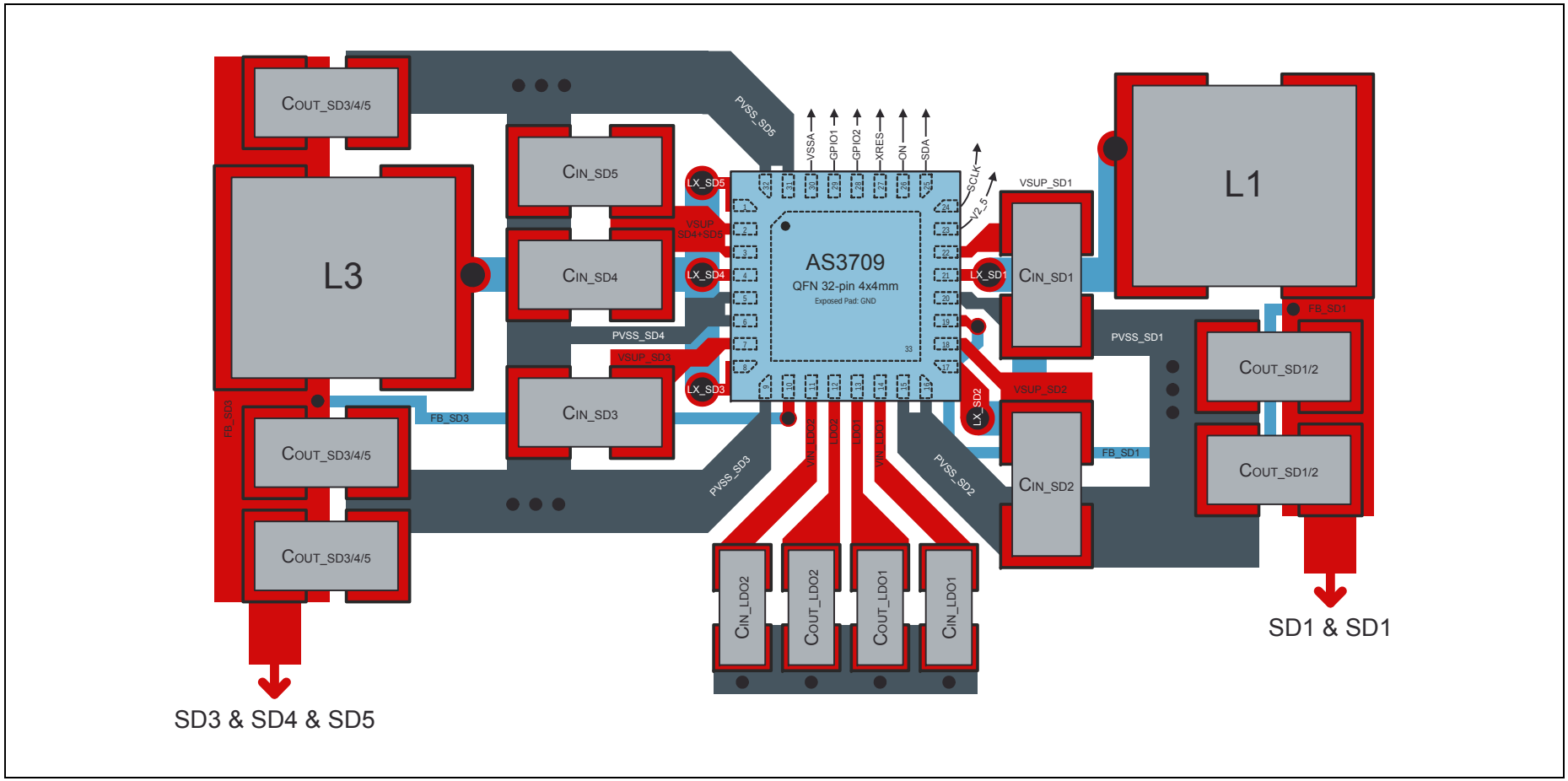
Figure 88:
Layout Guidelines 1/2



Layout Guidelines 1/2: This figure shows the recommended layout and placement of the external components for the 5 x 1A application circuit. Red lines and areas are connections on TOP layer. Grey lines and areas are GND and PVSS connections on TOP layer. Light blue lines and areas are connections on an inner layer or BOTTOM layer. Black round dots are vias. VSUP areas should be connected to an inner VSUP plane via vias. GND and PVSS areas should be connected to an inner GND plane via vias. A

PCB with minimum 4 layers is recommended.

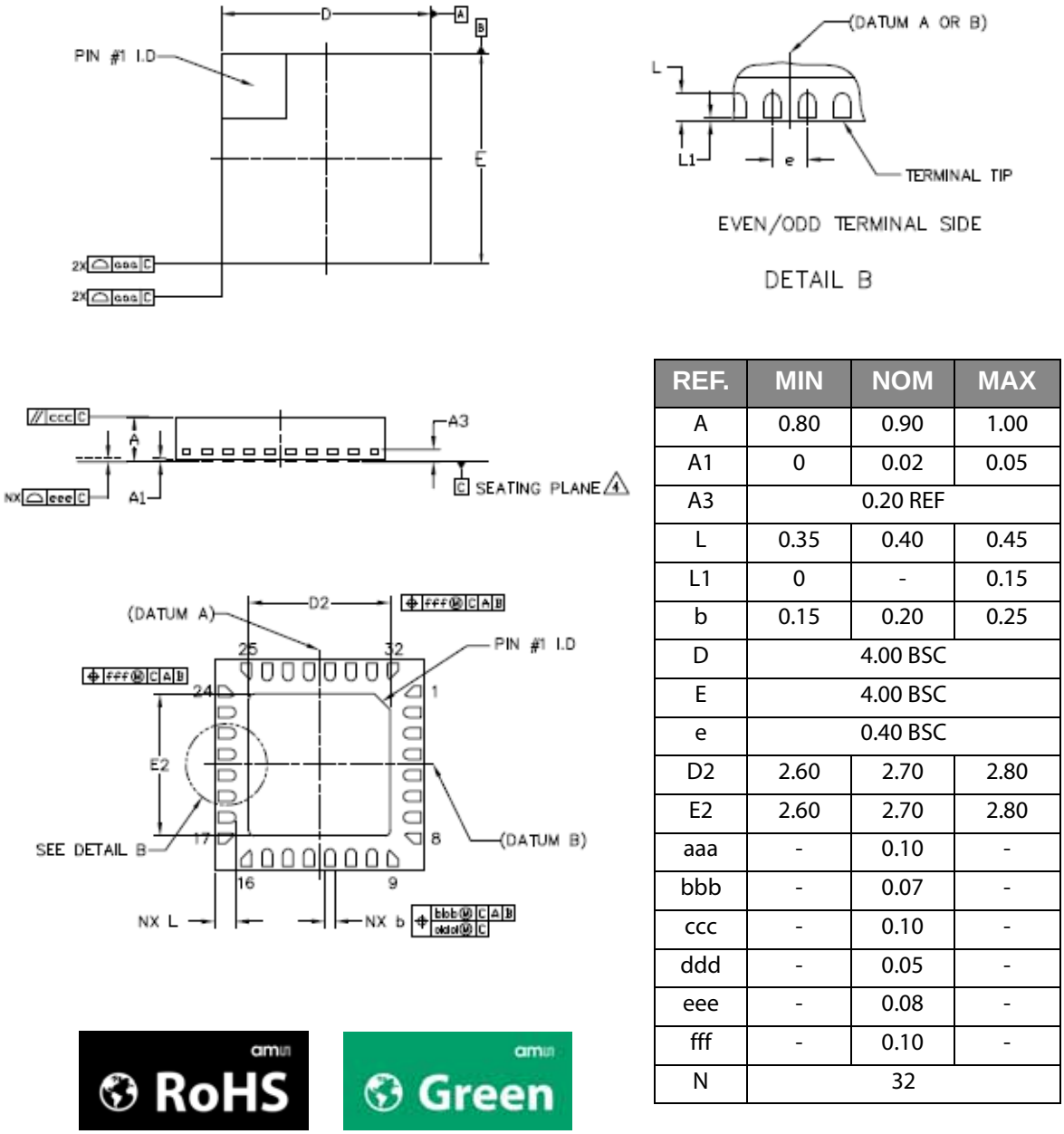
Figure 89:
Layout Guidelines 2/2



Layout Guidelines 2/2: Layout Guidelines 2/2: This figure shows the recommended layout and placement of the external components for the 1 x 2A & 1 x 3A application circuit. Red lines and areas are connections on TOP layer. Grey lines and areas are GND and PVSS connections on TOP layer. Light blue lines and areas are connections on an inner layer or BOTTOM layer. Black round dots are vias. VSUP areas should be connected to an inner VSUP plane via vias. GND and PVSS areas should be connected to an inner GND plane via vias. A PCB with minimum 4 layers is recommended.

Package Drawings & Markings

Figure 90:
QFN32 4x4 0.4mm Pitch Package Drawing

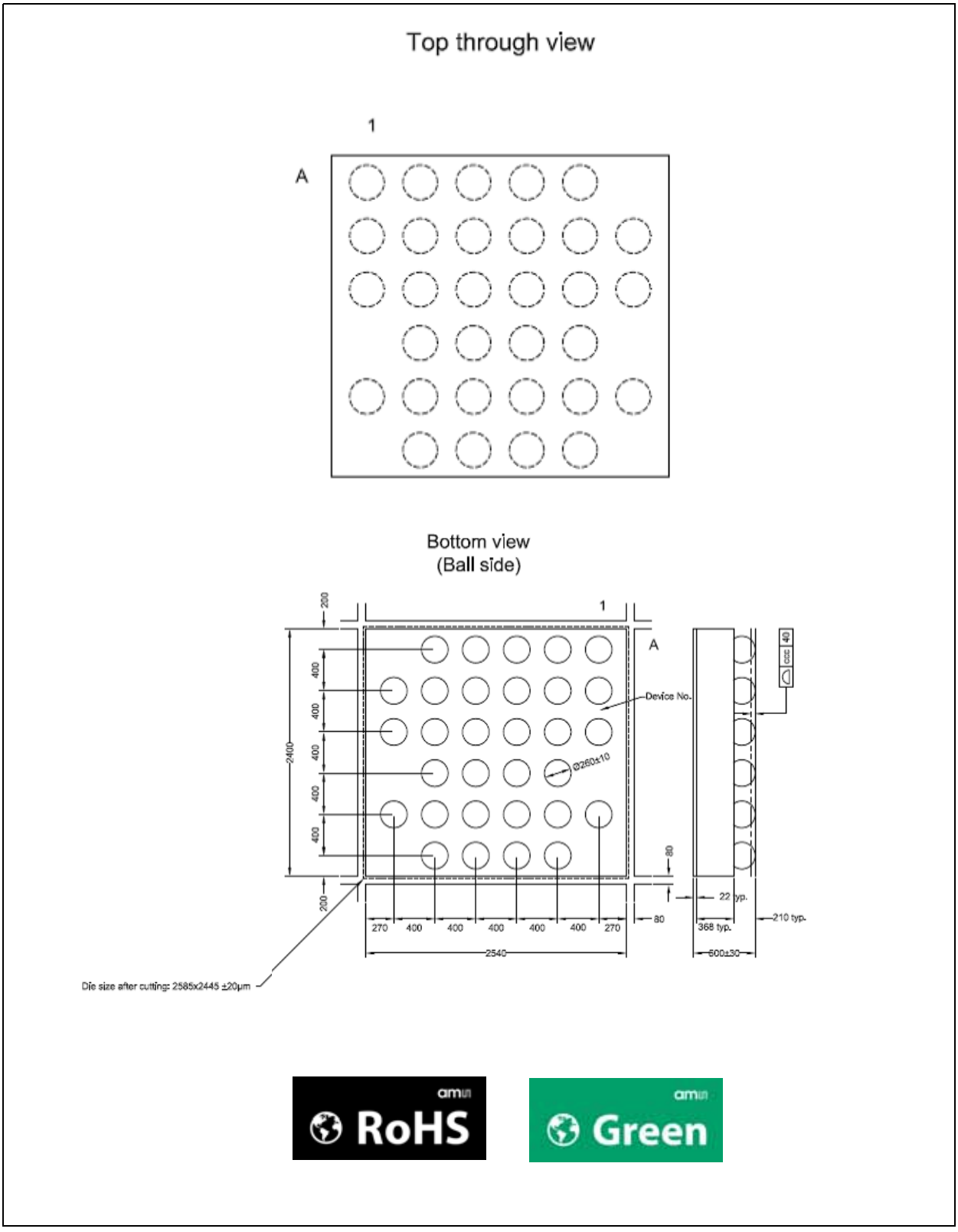


REF.	MIN	NOM	MAX
A	0.80	0.90	1.00
A1	0	0.02	0.05
A3		0.20 REF	
L	0.35	0.40	0.45
L1	0	-	0.15
b	0.15	0.20	0.25
D		4.00 BSC	
E		4.00 BSC	
e		0.40 BSC	
D2	2.60	2.70	2.80
E2	2.60	2.70	2.80
aaa	-	0.10	-
bbb	-	0.07	-
ccc	-	0.10	-
ddd	-	0.05	-
eee	-	0.08	-
fff	-	0.10	-
N		32	

Note(s) and/or Footnote(s):

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. All dimensions are in millimeters. Angles are in degrees.
3. Dimension b applies to metallized terminal and is measured between 0.25mm and 0.30mm from terminal tip. Dimension L1 represents terminal full back from package edge up to 0.15mm is acceptable.
4. Coplanarity applies to the exposed heat slug as well as the terminal.
5. Radius on terminal is optional.
6. N is the total number of terminals.

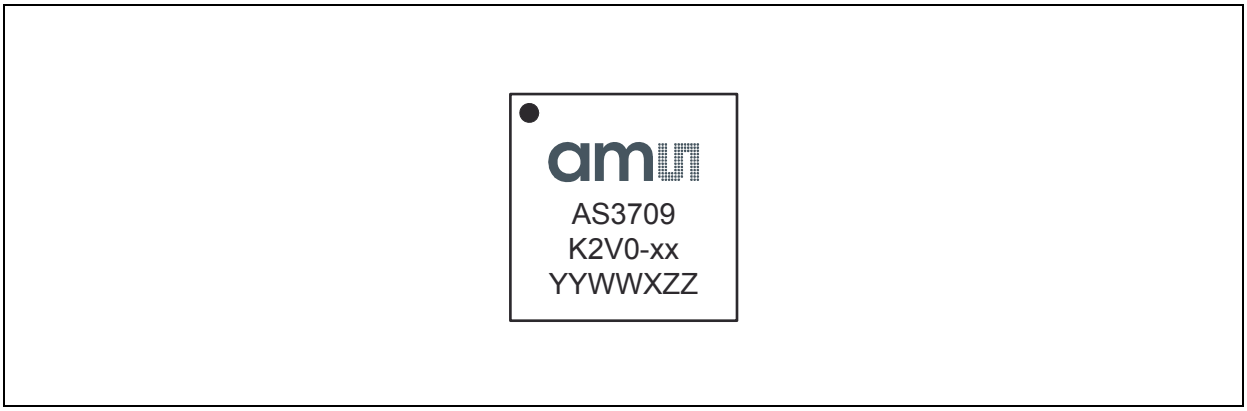
Figure 91:
WLP36 0.4mm Pitch Package Drawing



Note(s) and/or Footnote(s):

1. Pin 1 = A1
2. ccc Coplanarity
3. A1 dimensions are in µm

Figure 92:
QFN Marking



QFN Marking: Shows the package marking of the QFN product version.

Figure 93:
QFN Package Code

YY	WW	X	ZZ
Year	Manufacturing week	Plant identifier	Free choice

Figure 94:
Start-up Revision Code

Revision Code	Sequence
K2V0-ES	Engineering samples, no sequence programmed or sequence programmed on request
K2V0-00	Standard programming (no sequence programmed)
K2V0-xx	Customer specified sequence programmed during production test

Figure 95:
WL-CSP Marking

Figure 96:
WL-CSP Code

XXXX
Encoded Datecode

Figure 97:
Start-up Revision Code

Revision Code	Sequence
K2V0-ES	Engineering samples, no sequence programmed or sequence programmed on request
“empty”	Standard programming (no sequence programmed)
K2V0-00	Standard programming (no sequence programmed)
K2V0-xx	Customer specified sequence programmed during production test

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Ordering & Contact Information

Figure 98:
Ordering Information

Ordering Code	Marking	Sequence	Description	Delivery Form	Package
AS3709-BQFR-ES	K2V0-ES	Sequence programmable on request	µPMIC with 5 DCDC and 2 LDOs	Tray	32-pin QFN 4x4
AS3709-BQFM-00	K2V0-00	Default sequence	µPMIC with 5 DCDC and 2 LDOs	Tape & Reel	32-pin QFN 4x4
AS3709-BQFM-xx	K2V0-xx	Customer specified sequence	µPMIC with 5 DCDC and 2 LDOs	Tape & Reel	32-pin QFN 4x4
AS3709-BWLR-ES (Note:)	K2V0-ES	Sequence programmable on request	µPMIC with 5 DCDC and 2 LDOs	Tray	36-pin WL-CSP 0.4mm pitch
AS3709-BWLT-xx (Note:)	K2V0-xx	Customer specified sequence	µPMIC with 5 DCDC and 2 LDOs	Tape & Reel	36-pin WL-CSP 0.4mm pitch

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Reference Guide