Ethernet/IEEE 802.3 LAN Controller with Integrated MENDEC

Advance Data Sheet

FEATURES

- Integrated Ethernet Controller and Manchester Encoder/Decoder (MENDEC)
- Combines functions of the NCR92C390 and the NCR92C391
- Direct replacement of the DP83901A™
- Includes 16-byte internal FIFO with programmable threshold control
- Supports industry standard 8-, 16-, and 32-bit microprocessor interfaces
- Automatic CRC generation and checking circuit included
- Offers three loopback modes:
  - Controller only
  - Controller and MENDEC
  - Controller, MENDEC, and transceiver
- On-chip oscillator supports a crystal or TTL clock
- Supports the IEEE 802.3 standard including 10BASE2, 10BASE5 and 10BASE-T
- Decodes Manchester data with up to 20 ns of jitter
- Interface with 802.3 AUI cable, 10BASE2 or 10BASE-T transceiver
- 10 Mbps Manchester encoding/decoding with receiver clock recovery
- Externally selectable half- or full-step mode of operation at transmit output squelch circuitry to reject noise
- Low-power dissipation by using advance CMOS process

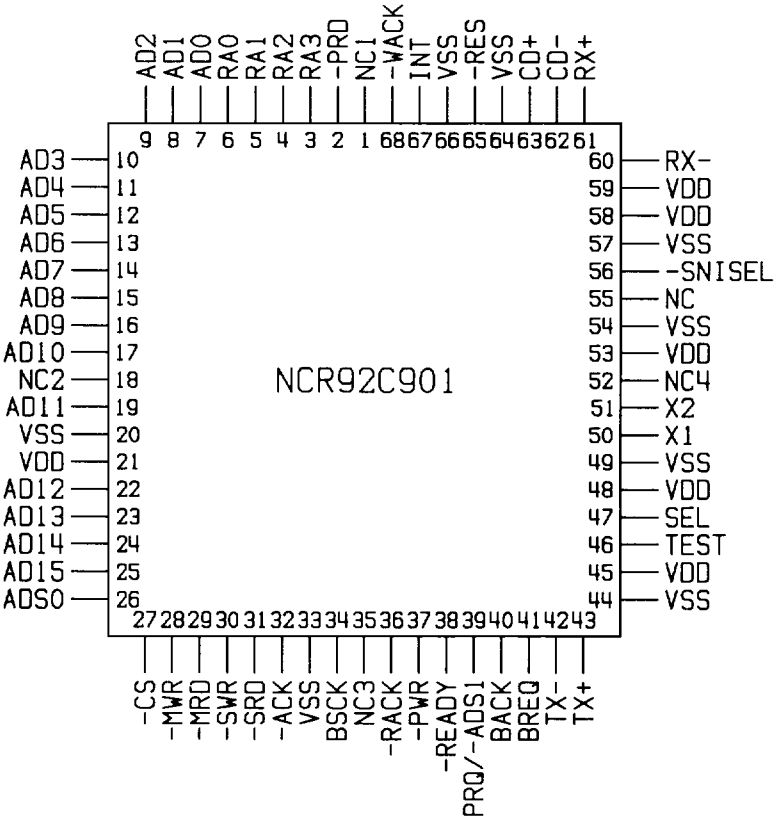


Figure 1 Pinout Diagram

Pinout Summary

Signal Name	Type	Pin No.	
NC	–	1	No Connect
–PRD	Output	2	Port Read (active low)
RA3	Input	3	Register Address
RA2	Input	4	Register Address
RA1	Input	5	Register Address
RA0	Input	6	Register Address
AD0	In/Out	7	Multiplexed Address/Data Bus
AD1	In/Out	8	Multiplexed Address/Data Bus
AD2	In/Out	9	Multiplexed Address/Data Bus
AD3	In/Out	10	Multiplexed Address/Data Bus
AD4	In/Out	11	Multiplexed Address/Data Bus
AD5	In/Out	12	Multiplexed Address/Data Bus
AD6	In/Out	13	Multiplexed Address/Data Bus
AD7	In/Out	14	Multiplexed Address/Data Bus
AD8	In/Out	15	Multiplexed Address/Data Bus
AD9	In/Out	16	Multiplexed Address/Data Bus
AD10	In/Out	17	Multiplexed Address/Data Bus
NC	–	18	No Connect
AD11	In/Out	19	Multiplexed Address/Data Bus
VSS	Ground	20	Ground
VDD	Power	21	Power
AD12	In/Out	22	Multiplexed Address/Data Bus
AD13	In/Out	23	Multiplexed Address/Data Bus
AD14	In/Out	24	Multiplexed Address/Data Bus
AD15	In/Out	25	Multiplexed Address/Data Bus
ADS0	In/Out	26	Address Strobe 0
–CS	Input	27	Chip Select (active low)
–MWR	In/Out	28	Master Write Strobe (active low)
–MRD	In/Out	29	Master Read Strobe (active low)
–SWR	Input	30	Slave Write Strobe (active low)
–SRD	Input	31	Slave Read Strobe (active low)
–ACK	Output	32	Acknowledge (active low)
VSS	Ground	33	Ground
BSCK	Input	34	Bus Clock
NC	–	35	No Connect
–RACK	Input	36	Read Acknowledge (active low)
–PWR	Output	37	Port Write (active low)
–READY	Input	38	Ready (active low)
PRQ/–ADS1	In/Out	39	Port Request/Address Strobe 1 (active high/low)
BACK	Input	40	Bus Acknowledge
BREQ	Output	41	Bus Request
TX–	Output	42	Transmit Output Minus
TX+	Output	43	Transmit Output Plus
VSS	Ground	44	Ground
VDD	Power	45	Power
TEST	Input	46	Test input (tied low during normal operation)
SEL	Input	47	Mode Select
VDD	Power	48	Power

Pinout Summary [continued]

Signal Name	Type	Pin No.	
VSS	Ground	49	Ground
X1	Input	50	Crystal or external oscillator input
X2	Output	51	Crystal feedback output
NC	–	52	No Connect
VDD	Power	53	Power
VSS	Ground	54	Ground
NC	–	55	No Connect
–SNISEL	Input	56	Test input (tied high during normal operation)
VSS	Ground	57	Ground
VDD	Power	58	Power
VDD	Power	59	Power
RX–	Input	60	Receive Input Minus
RX+	Input	61	Receive Input Plus
CD–	Input	62	Collision Input Minus
CD+	Input	63	Collision Input Plus
VSS	Ground	64	Ground
–RES	Input	65	Reset (active low)
VSS	Ground	66	Ground
INT	Output	67	Interrupt
–WACK	Input	68	Write Acknowledge (active low)

DESCRIPTION

The NCR92C901 provides the Media Access Controller (MAC) and the Manchester Encoder/Decoder (MENDEC) functions for IEEE 802.3 Local Area Networks (LANs) in one integrated circuit. The NCR92C901, in conjunction with a transceiver (10BASE5, 10BASE2, or 10BASE–T), implements the Ethernet MAC and physical solution of the IEEE 802.3 standard. The NCR92C901 converts 8– and 16–bit data from/to the parallel format used by processors to the serial format with the packet information needed for transmission on any Ethernet LAN. An internal FIFO and two DMA channels allow the NCR92C901 to efficiently manage the incoming and outgoing data. The integrated MENDEC interfaces to off–chip transceivers through six industry standard AUI signals. These may be routed off the board for connection to a 10BASE5 network, to an NCR92C392 for connection to a 10BASE2 network or to an NCR92C03–M for connection to a 10BASE–T network. Refer to Figure 2.

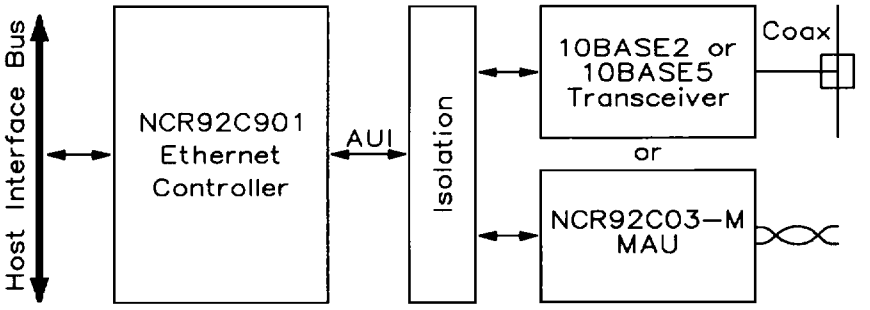


Figure 2 System Block Diagram

FUNCTIONAL DESCRIPTION

The NCR92C901 consists of two primary sections: the LAN Controller and the Manchester Encoder/ Decoder.

LAN CONTROLLER

The primary logical functions of the LAN Controller are shown on the left side of Figure 3.

- Receiver
- Transmitter
- DMA Control
- FIFO Logic
- Protocol Control
- Backoff Timers
- Bus Interface
- Multiplexer

Receiver

The receiver translates incoming NRZ serial data to standard data using the receive clock when the -CS input is asserted. The received data is byte-aligned by detecting the Start of Frame Delimiter (SFD). The data byte is placed in the internal 16-byte FIFO and the Receive Byte Count register is incremented. The first six bytes after the Start of Frame Delimiter are address fields which are checked by internal logic to validate further receptions. If the address field is not valid for receptions, the packet is discarded and the FIFO is cleared. During reception, a CRC for the incoming data packet is generated. If the CRC does not match the received CRC, an error condition is detected and the packet rejected. The first six bytes of the received packet (destination address field) is compared to the physical address registers. If they do not match, the packet is rejected. Multicast and broadcast addresses can be used also.

Transmitter

The data waiting for transmission is placed in the internal FIFO and shifted out with the most significant bit first. The Transmit Clock (TXC) is generated by the MENDEC logic. The transmitter appends 62 bits of preamble and a synchronization pattern prior to each packet transmission. The transmitted data is also routed to the internal CRC generator. After the last byte of the packet has been transmitted, the 32-bit CRC field is shifted out of the CRC logic directly. If the LAN Controller detects a collision during transmission, a 32-bit JAM pattern of all ones is generated.

DMA Control

The NCR92C901 contains two DMA channels: a local DMA channel and a remote DMA channel. During reception, the local DMA stores received packets in a receive buffer ring which is located in the local buffer memory. During transmission, the local DMA channel transfers packets from local buffer memory to an internal FIFO. The remote DMA channel is used as a slave DMA to transfer data between the local buffer memory and the host system. The local DMA channel has higher internal priority than the remote DMA channel.

FIFO and FIFO Control Logic

A 16-byte FIFO is built into the NCR92C901. During transmission, the local DMA channel writes data into the FIFO, and the transmission logic reads data from the FIFO and transmits it to the media. During reception, the receive logic writes data into the FIFO and the local DMA channel reads data from the FIFO. The FIFO control logic checks the number of bytes contained in the FIFO. If the byte count is lower (or higher) than the preset level, the local DMA begins a bus access and writes (or reads) data to (or from) the FIFO to keep the FIFO from underflowing (or overflowing).

Protocol Control

The protocol logic fully implements the IEEE 802.3 protocol. Collision recovery and random back-off logic is also implemented.

Backoff Timers

When a collision condition occurs, the NCR92C901 stops transmission, waits for a random period of time, and starts transmission again. The waiting period is determined by the back-off timers.

Bus Interface

The bus interface generates all bus interface signals necessary for DMA operations, bus request and bus acknowledge handshake protocol.

Multiplexer

The multiplexer is used to multiplex address and data bus contents at various bus cycles.

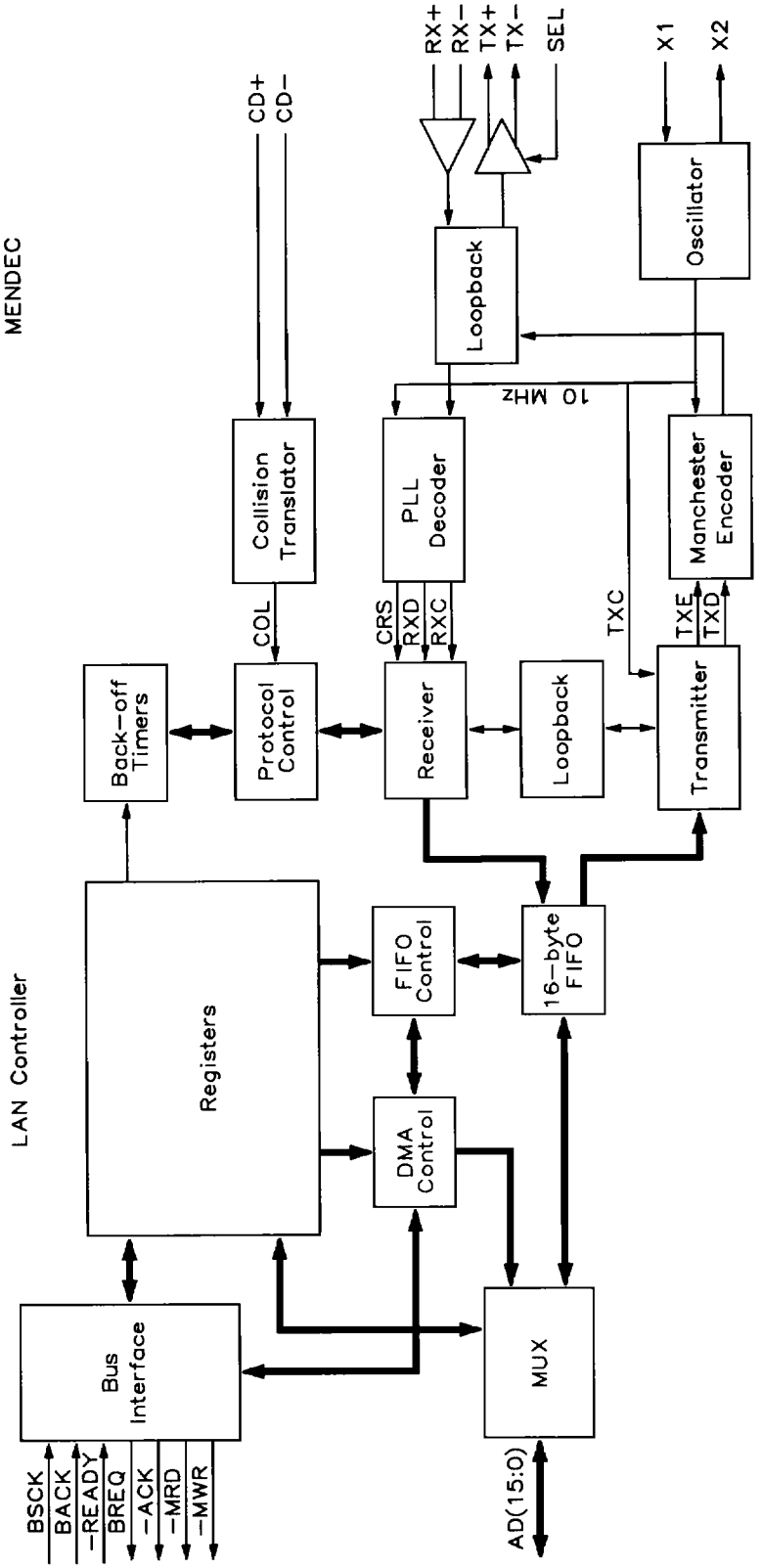


Figure 3 Chip Block Diagram

MANCHESTER ENCODER/DECODER

The primary logical functions of the MENDEC are shown on the right side of Figure 3. The Manchester Encoder/Decoder consists of the following.

- 20 MHz Crystal Oscillator
- Transmitter/Encoder
- Receiver/Decoder
- Collision Translator

Oscillator

A 20 MHz parallel resonant crystal or a 20 MHz TTL clock is used to control the oscillator that provides the 20 MHz clock signal. An internal divide-by-two counter generates the 10 MHz clock for the controller. The oscillator also provides internal clock signals to the encoding and decoding circuits.

The NCR92C901-C has an on-chip oscillator that operates with a crystal across X1 and X2, or with a TTL clock on X1 if X2 is left floating. For optimal performance, the total crystal load capacitance should not exceed 20 pF.

The NCR92C901-T requires a TTL clock to drive X1, and X2 can be left floating or grounded.

Transmitter/Encoder

When transmitting, the NCR92C901 combines clock pulses and the non-return-to-zero (NRZ) data from the controller and generates Manchester encoded data which is sent to the transceiver. The first half of the bit cell of a Manchester code contains the complement of the data and the second half contains the data, so a transition is always guaranteed in the middle of a bit cell.

The differential transmit pair (TX+/-) drives up to 50 meters of twisted pair AUI cable through an isolation transformer. These output pins are source followers which require two 270 Ω pulldown resistors to ground.

The NCR92C901 allows half-step and full-step functions to be compatible with the original Ethernet, Version 1.0, and IEEE 802.3 specifications. With the SEL signal low (for the original Ethernet), TX+ is positive with respect to TX- during the idle state. With SEL high (for the IEEE 802.3 specifications), TX+ and TX- are equal in the idle state. This provides zero differential voltage to operate with transformer coupled loads.

Receiver/Decoder

The decoder consists of a differential receiver to sense the signal of the transceiver cable and a Phase-Locked Loop (PLL) to lock onto the preamble of the incoming signal. The differential inputs (RX+/-) must be externally terminated with two 39 Ω resistors connected in series if the standard 78 Ω transceiver drop cable is used. In thin Ethernet applications, these resistors are optional.

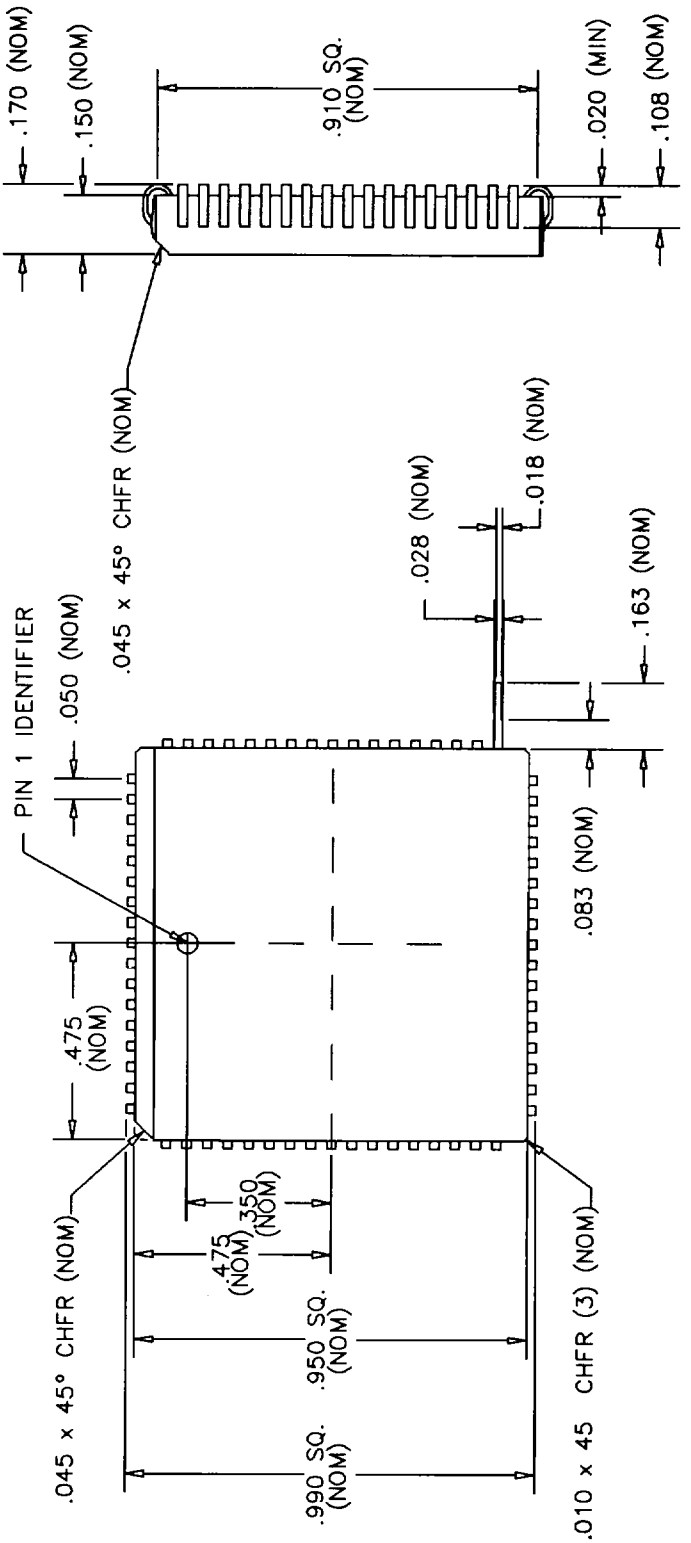
The carrier receiver detects the presence of an incoming data packet by discerning and rejecting noise from expected Manchester data. Transient noise with pulses less than 30 ns or signals with negative peaks smaller than -175 mV are rejected by the receiver. Carrier is detected for input signals with pulse widths of more than 30 ns and less than -300 mV.

The NCR92C901 tolerates jitter up to 20 ns in the receive data. The decoder detects the end of a frame when no mid-bit transitions are detected within 1.5 bit-times after the last bit. The receive clock stays active five more bit-times after the end of the receive frame to guarantee the receive timing on the controller.

Collision Translator

A transceiver detects collision on the network and generates a 10 MHz signal on the CD+/- inputs. This collision signal passes through an input stage that detects signal levels and pulse duration (the same way as the differential receive inputs). When the collision signal is detected, the NCR92C901 stops its current transmission and transmits again later.

MECHANICAL SPECIFICATIONS



NOTE : All dimensions are in inches.

ORDERING INFORMATION

The NCR92C901 is available in two versions.

1. The NCR92C901-C has an on-chip oscillator that operates with a crystal across X1 and X2, or with a TTL clock on X1 if X2 is left floating.
2. The NCR92C901-T requires a TTL clock to drive X1, and X2 can be left floating or grounded.

Each version of the NCR92C901 is available in a 68-pin Plastic Leaded Chip Carrier (PLCC). Use the following part numbers to order the part.

Package Type	Part Number
68-pin PLCC	NCR92C901-TPL
68-pin PLCC	NCR92C901-CPL

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUMS

Symbol	Parameter	Minimum	Maximum	Units
T_A	Ambient Temperature	0	70	°C
T_S	Storage Temperature	−55	125	°C
V_{DD}	Supply Voltage	−0.5	7.0	V
V_{IN}	Input Voltage	−0.5	V_{DD} + 0.5	V
V_{OUT}	Output Voltage	−0.5	V_{DD} + 0.5	V
T_L	Lead Temperature (Soldering 10 seconds maximum)		250	°C

DC CHARACTERISTICS

(V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Symbol	Parameter	Minimum	Maximum	Units
V_{OL}	Low Output Voltage (I_{OL} = 2.0 mA) (Notes 1, 4)		0.4	Volts
	Low Output Voltage (I_{OL} = 20 µA) (Notes 1, 4)		0.1	Volts
V_{OH}	High Output Voltage (I_{OH} = 2.0 mA) (Notes 1, 4)	3.5		Volts
	High Output Voltage (I_{OH} = 20 µA) (Notes 1, 4)	V_{DD} − 0.1		Volts
V_{IL}	Low Input Voltage (Note 2)		0.8	Volts
	Low Input Voltage for −RACK, −WACK (Note 2)		0.6	Volts
V_{IH}	High Input Voltage (Note 2)	2.0		Volts
	High Input Voltage for −RACK, −WACK (Note 2)	2.7		Volts
I_{IL}	Input Leakage Current (V_{IN} = V_{DD} or V_{SS})		±1.0	µA
I_{OZ}	Tristate Output Leakage (V_{OUT} = V_{DD} or V_{SS})		±10	µA
I_{DD}	Power Supply Current (V_{IN} = V_{DD} or V_{SS}) (TXC, RXC, BSCK = 10 MHz) (I_{OUT} = 0 µA) (Note 3)		40	mA

1 These levels are tested dynamically using a limited number of functional test patterns. Refer to the *AC Test Conditions* below.

2 Limited functional test patterns are performed at these input levels. For most functional tests, V_{IH} is performed at 0 V and 3 V. For −RACK and −WACK, V_{IH} is performed at 0 V and 3.2 V.

3 This is measured with a 0.1µF bypass capacitor between V_{DD} and V_{SS}.

4 The low-drive, CMOS-compatible V_{OH} and V_{OL} limits are not tested directly. Detailed device characterization guarantees this specification by testing the high-drive, TTL-compatible V_{OH} and V_{OL} specification.

AC CHARACTERISTICS

Latched Register Read Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
1	Bus clock high duration	4	22.5		ns
2	Bus clock low duration	4	22.5		ns
3	Bus clock cycle time	4	50	1000	ns
4	RA(3:0) setup to ADS0 low	4	10		ns
5	RA(3:0) hold from ADS0 low	4	13		ns
6	ADS0 pulse width	4	15		ns
7	-ACK to AD(7:0) valid	4		55	ns
8	-SRD high to data tristate	4	15	70	ns
9	-SRD low to -ACK low (Notes 1, 2, 3)	4		n*BSCK + 30	ns [4]
10	-SRD high to -ACK high	4		30	ns
11	RA(3:0) to -SRD low (Note 2)	4	10		ns

[1] -ACK is not generated until -CS and -SRD are low and the NCR92C901 has synchronized to the register access. The NCR92C901 inserts bus clock cycles until it has synchronized to the register access. In dual bus systems, additional cycles are added to complete a local or remote Direct Memory Access (DMA). Wait states must be issued to the CPU until -ACK is asserted low.

[2] -CS can be asserted before or after -SRD. If -CS is asserted after -SRD, parameter #9 is referenced from the falling edge of -CS.

[3] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

[4] This unit is based on the bus clock cycle.

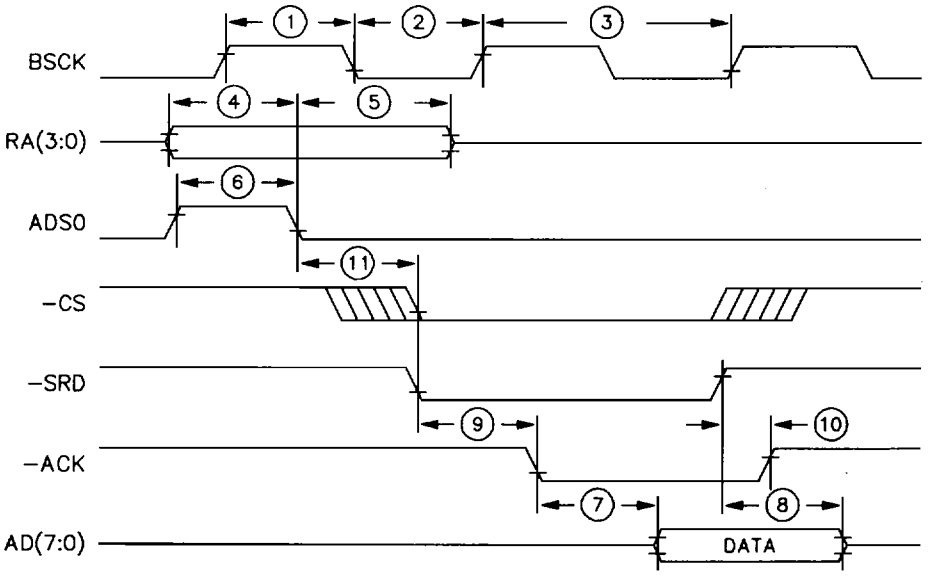


Figure 4 Latched Register Read (ADS0=0)

Unlatched Register Read Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
12	RA(3:0) setup time to -SRD (Notes 1, 2)	5	10		ns
13	RA(3:0) hold from -SRD	5	0		ns
14	-ACK low to valid data	5		55	ns
15	-SRD high to data tristate (Note 3)	5	15	70	ns
16	-SRD low to -ACK low (Note 2)	5		n*BSCK + 30	ns [4]
17	-SRD high to -ACK high	5		30	ns

[1] This specification includes flow-through time of the latch.

[2] Since address decode begins when -ACK is asserted, -CS can be asserted before or after -SRD and RA(3:0). If -CS is asserted after -SRD and RA(3:0), parameter #12 is referenced from the falling edge of -CS.

[3] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

[4] This unit is based on the bus clock cycle.

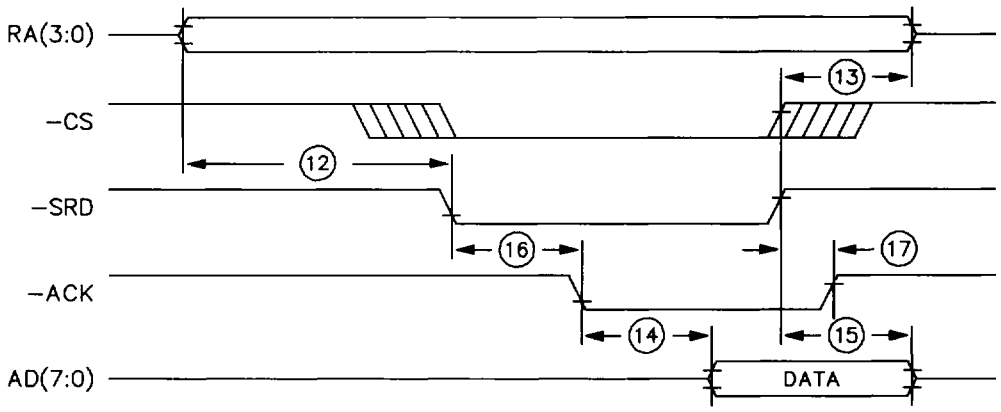


Figure 5 Unlatched Register Read (ADS0=1)

Latched Register Write Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
18	RA(3:0) setup to ADS0 low	6	10		ns
19	RA(3:0) hold from ADS0 low	6	17		ns
20	ADS0 pulse width	6	15		ns
21	AD(7:0) setup time to -SWR	6	20		ns
22	AD(7:0) hold time from -SWR	6	21		ns
23	-SWR width from -ACK low	6	50		ns
24	-SWR high to -ACK high	6		30	ns
25	-SWR low to -ACK low (Notes 1, 2)	6		n*BSCK + 30	ns [3]
26	RA(3:0) to -SWR low	6	10		ns

[1] -ACK is not generated until -CS and -SWR are low and the NCR92C901 has synchronized to the register access. In dual bus systems, additional cycles are added to complete a local or remote Direct Memory Access (DMA).

[2] -CS can be asserted before or after -SWR. If -CS is asserted after -SWR, parameter #24 is referenced from the falling edge of -CS.

[3] This unit is based on the bus clock cycle.

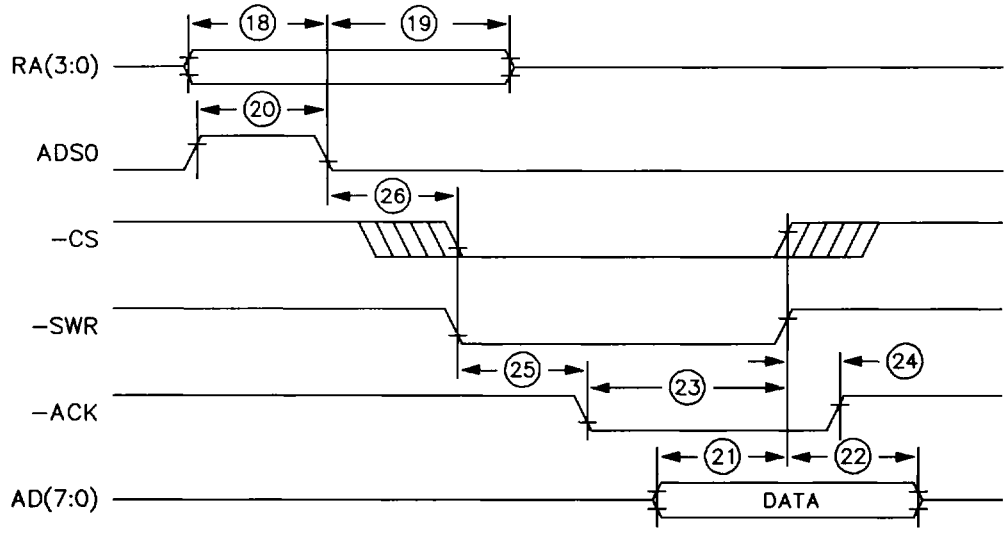


Figure 6 Latched Register Write (ADS0=0)

Unlatched Register Write Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
27	RA(3:0) setup time to -SWR (Note 1)	7	15		ns
28	RA(3:0) hold time from -SWR	7	0		ns
29	AD(7:0) setup time to -SWR	7	20		ns
30	AD(7:0) hold time from -SWR	7	21		ns
31	-SWR low to -ACK low (Note 2)	7		n*BSCK + 30	ns [3]
32	-SWR high to -ACK high	7		30	ns
33	-ACK low to -SWR high	7	50		ns

[1] This assumes that ADS0 is high when RA(3:0) is changing.

[2] -ACK is not generated until -CS and -SWR are low and the NCR92C901 has synchronized to the register access. In dual bus systems, additional cycles are added to complete a local or remote Direct Memory Access (DMA).

[3] This unit is based on the bus clock cycle.

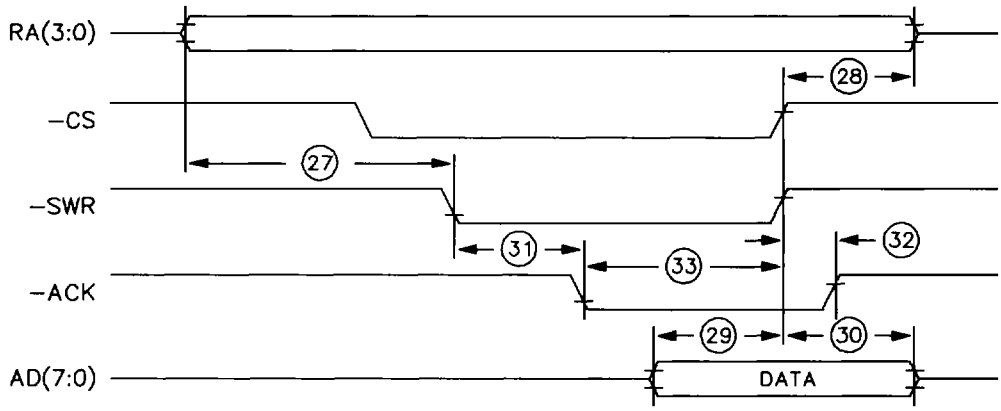


Figure 7 Unlatched Register Write (ADS0=1)

DMA Control Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
34	BSCK to BREQ high for local DMA	8		48	ns
35	BSCK to BREQ high for remote DMA	8		38	ns
36	BSCK to BREQ low	8		55	ns
37	BACK setup to BSCK (Note 1)	8	5		ns
38	BSCK to control enable	8		60	ns
39	BSCK to control release (Notes 2, 3)	8		70	ns

[1] BACK must be setup before T1 after BREQ is asserted. Missing the setup will slip the beginning of the DMA by four bus clocks. This bus latency will influence the allowable FIFO threshold and transfer mode (empty/fill vs. exact burst transfer).

[2] During remote DMA transfers only, a single bus transfer is performed. During local DMA operations, burst transfers are performed.

[3] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

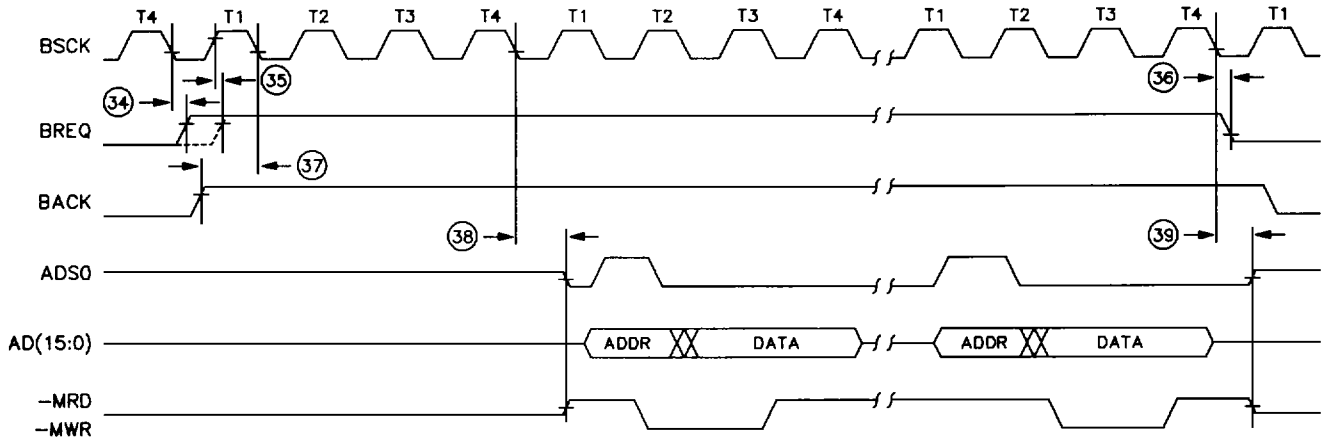


Figure 8 DMA Control – Bus Arbitration

DMA Address Generation (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
3	BSCK period (Note 1)	9	50	1000	ns
1	BSCK high duration	9	22.5		ns
2	BSCK low duration	9	22.5		ns
43	BSCK high to ADS1 high	9		34	ns
44	BSCK low to ADS1 low	9		44	ns
45	ADS1 duration	9	BSCK high duration		ns [3]
46	BSCK high to valid address	9		50	ns
47	BSCK high to address tristate (Note 2)	9	15	55	ns
48	AD(15:0) setup time to ADS0 or ADS1 low	9	BSCK high duration − 15		ns [3]
49	AD(15:0) hold time from ADS0 or ADS1 low	9	BSCK low duration − 5		ns [3]

[1] The rate of the bus clock must be high enough to support transfers to/from the FIFO at a rate greater than the serial network transfers from/to the FIFO.

[2] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

[3] This unit is based on the high/low duration of the bus clock cycle.

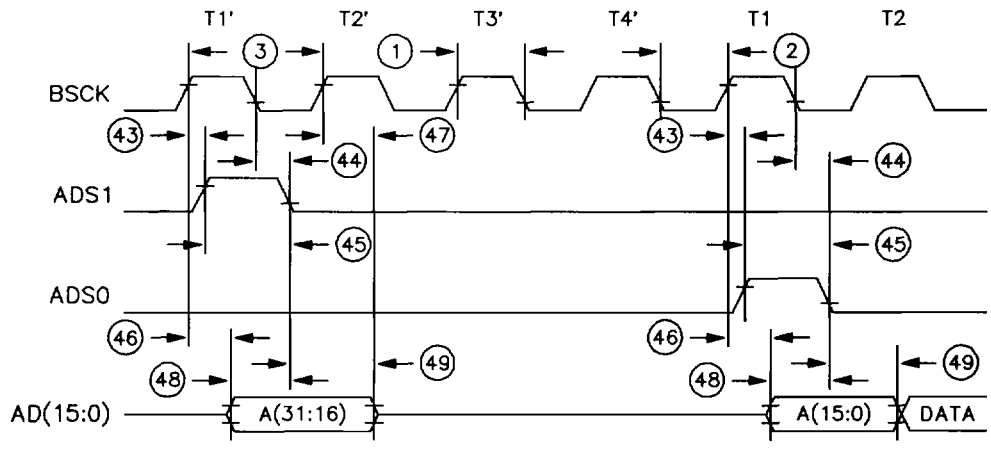


Figure 9 DMA Address Generation

Cycles T1′, T2′, T3′, and T4′ are issued only for the first transfer in a burst when 32-bit mode has been selected.

DMA Read Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
50	BSCK high to -MRD low	10		43	ns
51	BSCK high to -MRD high	10		40	ns
52	Data setup time to -MRD high	10	25		ns
53	Data hold time from -MRD high	10	0		ns
54	-MRD duration	10	2*BSCK - 15		ns [3]
55	-MRD high to address tristate (Notes 1, 2)	10		BSCK high duration + 40	ns [4]
56	ADS0 low to -MRD low	10		BSCK low duration + 10	ns [4]
57	-MRD high to address active	10	BSCK - 10		ns [3]
58	Address valid to -MRD high	10	3*BSCK - 15		ns [3]

[1] During a burst, A(15:8) are not tristate if byte wide transfers are selected. On the last transfer, A(15:8) are tristate as shown below.

[2] These limits include the RC delay inherent in our test method. These signals typically turn off within the BSCK high duration + 15 ns, enabling other devices to drive these signals without contention.

[3] This unit is based on the bus clock cycle.

[4] This unit is based on the high/low duration of the bus clock cycle.

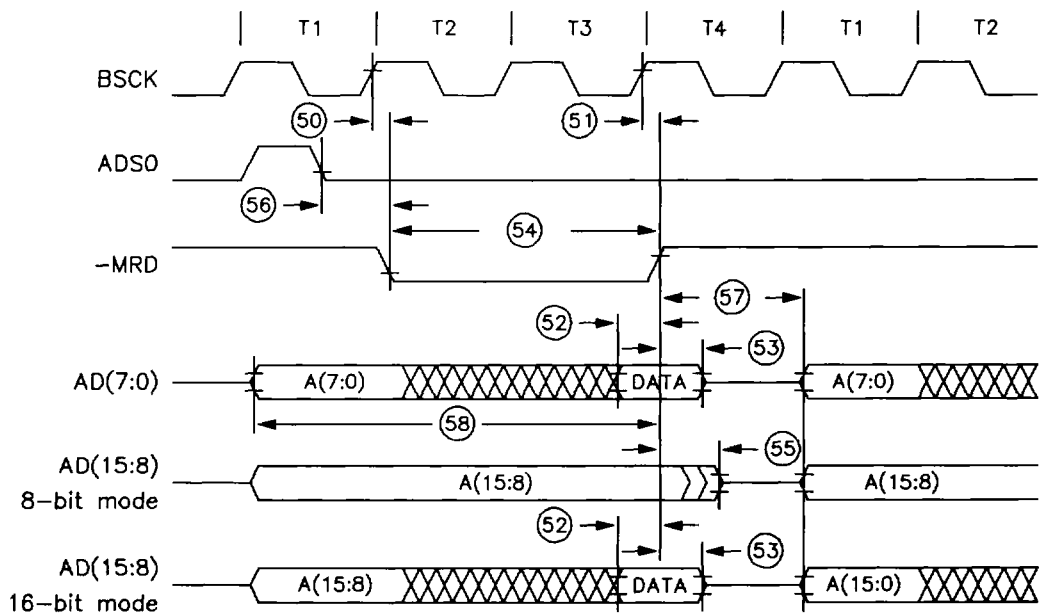


Figure 10 DMA Memory Read

DMA Write Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
59	BSCK high to -MWR low	11		40	ns
60	BSCK high to -MWR high	11		40	ns
61	Data setup time to -MWR high	11	2*BSCK - 30		ns [3]
62	Data hold time from -MWR high	11	BSCK high duration + 7		ns [4]
63	-MRW high to address tristate (Notes 1, 2)	11		BSCK high duration + 40	ns [4]
64	ADS0 low to -MWR low	11		BSCK low duration + 10	ns [4]
65	ADS0 low to valid data	11		BSCK low duration + 30	ns [4]

[1] When using byte mode transfers, A(15:8) are only tristate on the last transfer; this timing is valid only for the last transfer in a burst.

[2] These limits include the RC delay inherent in our test method. These signals typically turn off within 15 ns, enabling other devices to drive these signals without contention.

[3] This unit is based on the bus clock cycle time.

[4] This unit is based on the high/low duration of the bus clock cycle.

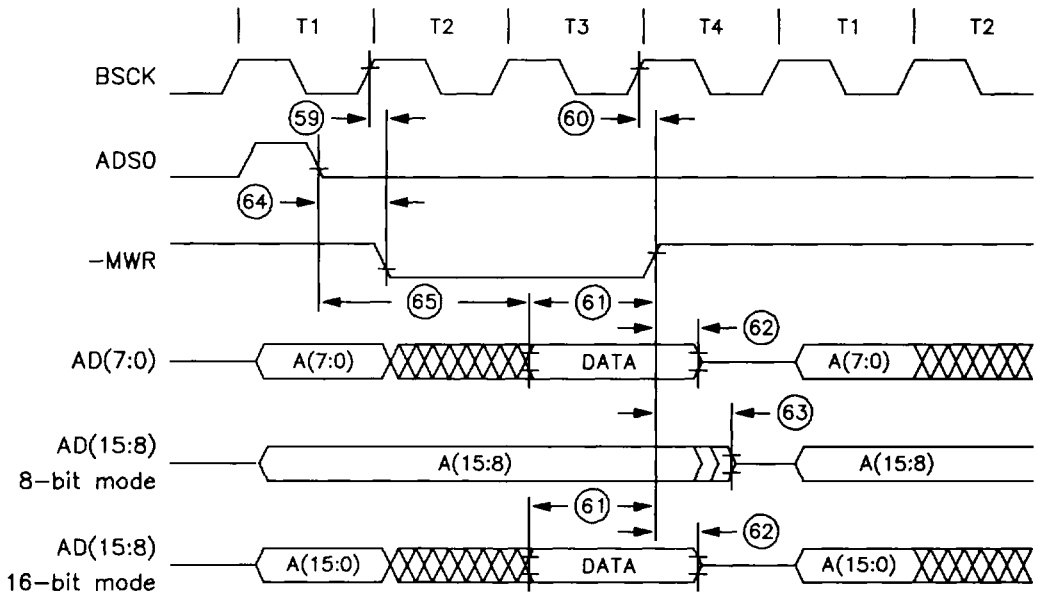


Figure 11 DMA Memory Write

Wait State Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
66	–READY setup to T3 BSCK low	12	10		ns
67	–READY low to BSCK low (release time) [1]	12	15		ns

[1] The addition of wait states affects the count of deserialized bytes and is limited to a number of bus clock cycles depending on the bus clock and network rates. The allowable wait states are shown in the table below.

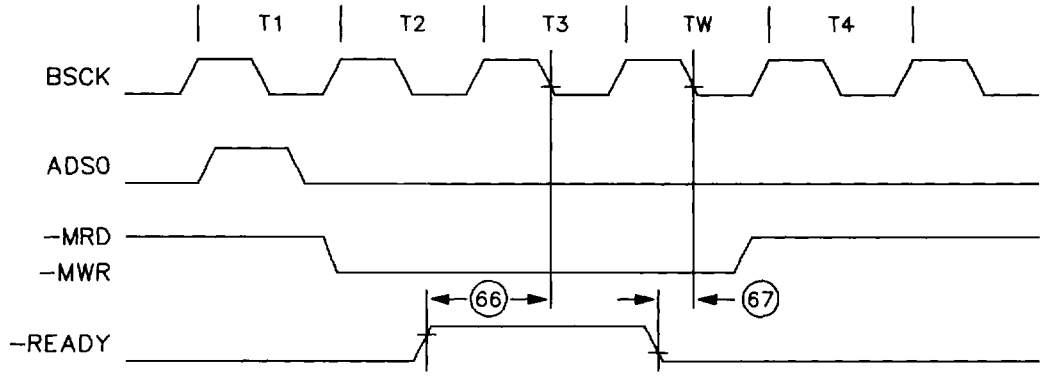


Figure 12 Wait State Insertion

TABLE 1

BSCK (MHz)	Number of Wait States	
	Byte Transfer	Word Transfer
8	0	1
10	0	1
12	1	2
14	1	2
16	1	3
18	2	3
20	2	4

Table 1 assumes a 10 MHz network clock. The number of allowable wait states in byte mode can be calculated using:

$$\#W_{(byte\ mode)} = \left(\frac{8\ tnw}{4.5\ BSCK} - 1 \right)$$

#W = the number of wait states
tnw = the network clock period
BSCK = BSCK period

The number of allowable wait states in word mode can be calculated using:

$$\#W_{(word\ mode)} = \left(\frac{5\ tnw}{2\ BSCK} - 1 \right)$$

Remote DMA Read Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
68	BSCK to -PWR low	13		43	ns
69	BSCK to -PWR high	13		40	ns
70	-PWR high to PRQ high [1]	13		30	ns
71	PRQ low from -RACK high	13		45	ns
72	-RACK read strobe pulse width	13	20		ns

[1] Start of next transfer is dependent on where -RACK is generated relative to BSCK and whether local DMA is pending.

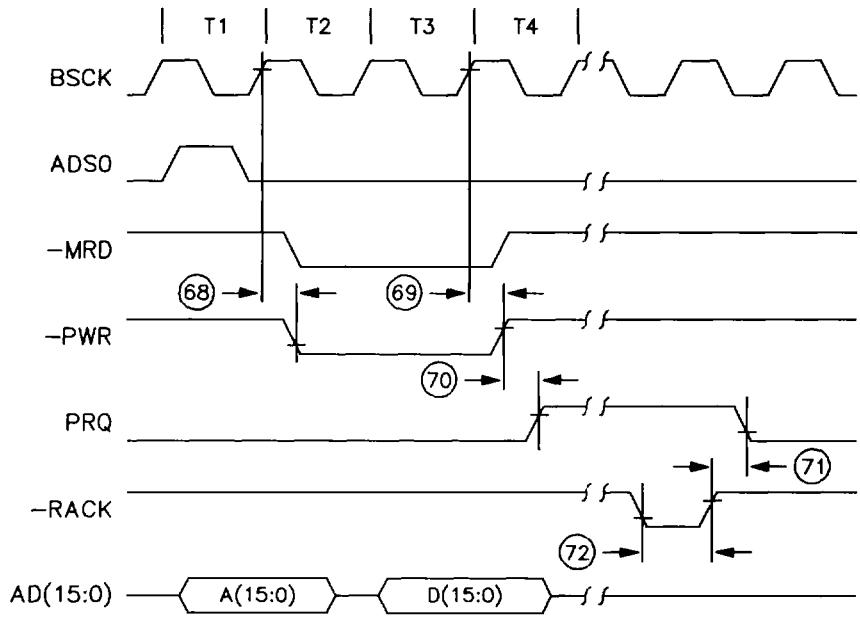


Figure 13 Remote DMA Read

Remote DMA Read Recovery Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
68	BSCK to -PWR low	14		43	ns
69	BSCK to -PWR high	14		40	ns
70	-PWR high to PRQ high (Note 1)	14		30	ns
71	PRQ low from -RACK high	14		45	ns
72	-RACK read strobe pulse width	14	20		ns
73	-RACK high to next port write cycle (Notes 2, 3, 4)	14	11		BSCK[5]

[1] Start of next transfer is dependent on where -RACK is generated relative to BSCK and whether local DMA is pending.

[2] This is not a measured value but it is guaranteed by design.

[3] -RACK must be high for a minimum of seven BSCK cycles.

[4] Assumes no local DMA interleave, no -CS input, and immediate BACK.

[5] This unit is the bus clock period.

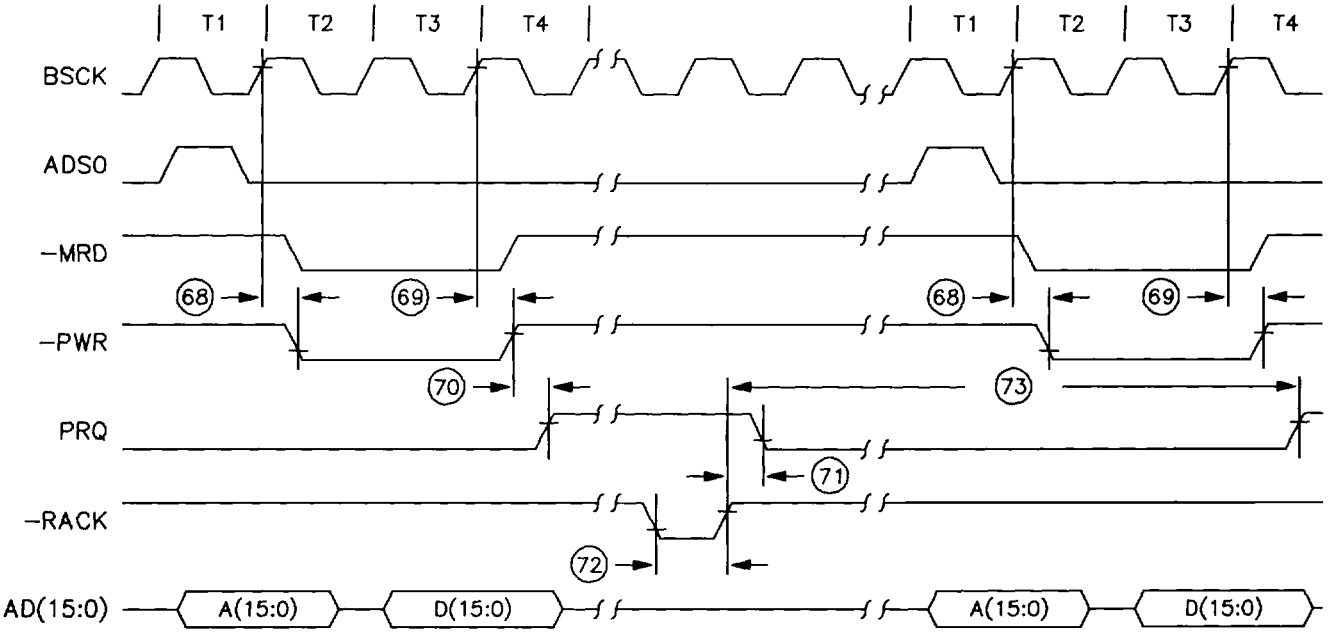


Figure 14 Remote DMA Read Recovery

Remote DMA Write Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
74	BSCK to PRQ high (Note 1)	15		40	ns
75	-WACK to PRQ low	15		55	ns
76	-WACK pulse width	15	20		ns
77	BSCK to -PRD low (Note 2)	15		40	ns
78	BSCK to -PRD high	15		40	ns

[1] The first port request is issued in response to the remote write command. It is subsequently issued on T1 clock cycles following completion of remote DMA cycles.

[2] The start of the remote DMA write following -WACK is dependent on where -WACK is issued relative to BSCK and whether a local DMA is pending.

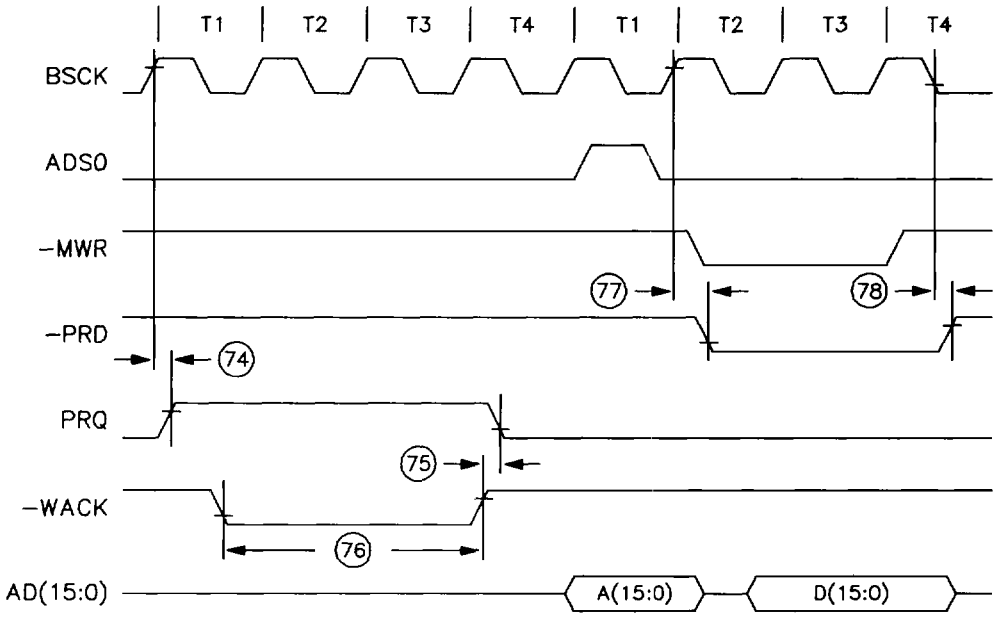


Figure 15 Remote DMA Write

Remote DMA Write Recovery Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Minimum	Maximum	Units
74	BSCK to PRQ high (Note 1)	16		42	ns
75	-WACK to PRQ low	16		55	ns
76	-WACK pulse width	16	20		ns
77	BSCK to -PRD low (Note 2)	16		40	ns
78	BSCK to -PRD high	16		40	ns
79	Remote write PRQ to PRQ high (Notes 3, 4, 5)	16	12		BSCK[6]

[1] The first port request is issued in response to the remote write command. It is subsequently issued on T1 clock cycles following completion of remote DMA cycles.

[2] The start of the remote DMA write following -WACK is dependent on where -WACK is issued relative to BSCK and whether a local DMA is pending.

[3] This assumes that parameter #76 is less than one BSCK, that there is no local DMA interleave, no -CS input, immediate -BACK, and -WACK goes high before T4.

[4] -WACK must be high for a minimum of seven BSCK cycles.

[5] This is not a measured value but it is guaranteed by design.

[6] This unit is the bus clock period.

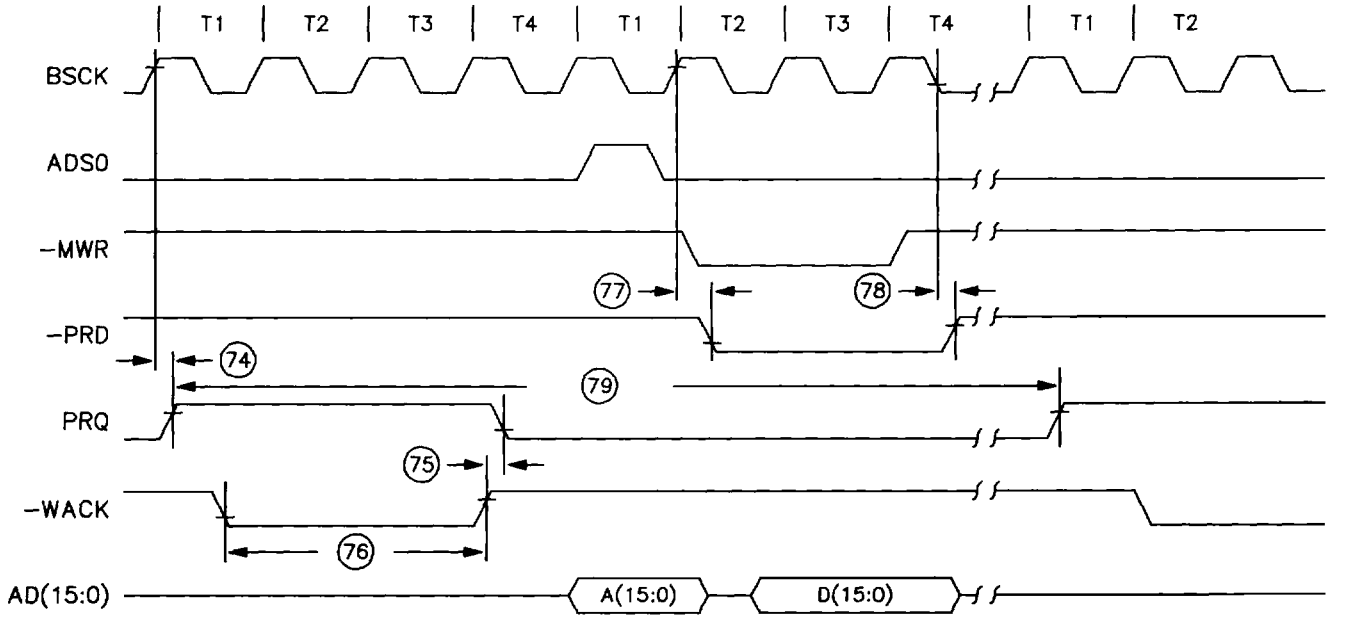


Figure 16 Remote DMA Write Recovery

Transmit Timing (V_{DD} = 4.75V to 5.25V, V_{SS} = 0V, T_A = 0°C to 70°C)

Num.	Description	Figure	Min.	Typ.	Max.	Units
80	TX+/– high before idle (half step)	17	200			ns
81	TX+/– idle time (half step)	17			8	µs

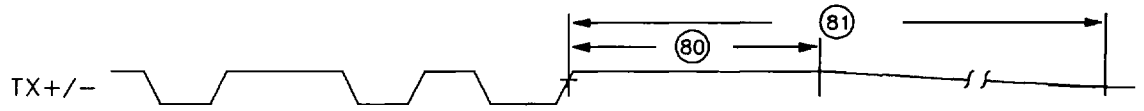
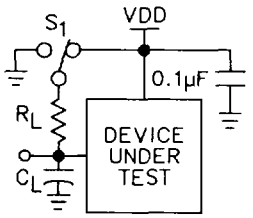


Figure 17 Transmit

AC TEST CONDITIONS

Condition	Test Value
Input Pulse Levels	VSS to 3.0 V
Input Rise/Fall Time	5 ns
Input/Output Reference	1.3 V
Tristate Reference Level	Float (ΔV) ±0.5 V



C_L = 50 pF including scope and jig capacitance.
S1 = Open for timing tests for push–pull outputs.
S1 = V_{DD} for V_{OL} test. S1 = V_{SS} for V_{OH} test.
S1 = V_{DD} for measurements from high impedance to active low, and active low to high impedance.
S1 = V_{SS} for measurements from high impedance to active high, and active high to high impedance.

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