



N-Channel Enhancement-Mode Vertical DMOS FET

Ordering Information Standard Commercial Devices

BV _{DSS} / BV _{DGS}	R _{DS(ON)} (max)	I _{D(ON)} (min)	Order Number / Package						
			TO-39	TO-52	TO-92	TO-220	Quad P-DIP	Quad C-DIP*	DICE†
40V	3Ω	2.0A	VN0104N2	VN0104N9	VN0104N3	VN0104N5	VN0104N6	VN0104N7	VN0104ND
60V	3Ω	2.0A	VN0106N2	VN0106N9	VN0106N3	VN0106N5	VN0106N6	VN0106N7	VN0106ND
90V	3Ω	2.0A	VN0109N2	VN0109N9	VN0109N3	VN0109N5	—	—	VN0109ND

* 14 pin side brazed ceramic DIP

† MIL visual screening available

High Reliability Devices

See pages 5-4 and 5-5 for MILITARY STANDARD Process Flows and Ordering Information.

Features

- Free from secondary breakdown
- Low power drive requirement
- Ease of paralleling
- Low C_{ISS} and fast switching speeds
- Excellent thermal stability
- Integral Source-Drain diode
- High input impedance and high gain
- Complementary N- and P-channel devices

Applications

- Motor control
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

Absolute Maximum Ratings

Drain-to-Source Voltage	BV _{DSS}
Drain-to-Gate Voltage	BV _{DGS}
Gate-to-Source Voltage	± 20V
Operating and Storage Temperature	-55°C to +150°C
Soldering Temperature*	300°C

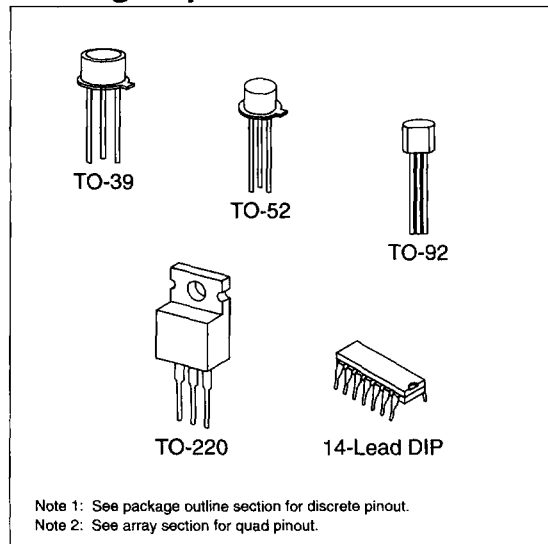
* Distance of 1.6 mm from case for 10 seconds.

Advanced DMOS Technology

These enhancement-mode (normally-off) transistors utilize a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Package Options



Note 1: See package outline section for discrete pinout.

Note 2: See array section for quad pinout.

Thermal Characteristics

Package	I_D (continuous)*	I_D (pulsed)	Power Dissipation @ $T_C = 25^\circ\text{C}$	θ_{JA} $^\circ\text{C/W}$	θ_{JC} $^\circ\text{C/W}$	I_{DR}^*	I_{DRM}
TO-39	0.8A	2.5A	3.5W	125	35	0.8A	2.5A
TO-52	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-92	0.5A	2.0A	1.0W	170	125	0.5A	2.0A
TO-220	1.5A	2.5A	15.0W	70	8	1.5A	2.5A
Plastic DIP Ceramic DIP	See DMOS Arrays & Special Functions section						

* I_D (continuous) is limited by max rated T_J .

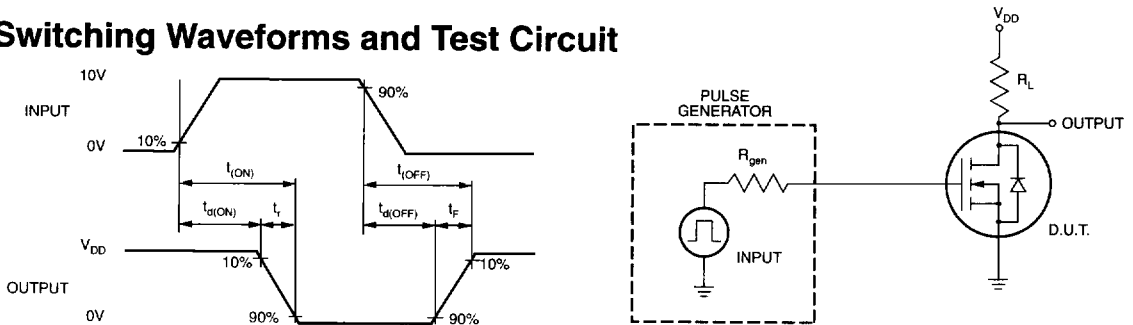
Electrical Characteristics (@ 25°C unless otherwise specified)

Symbol	Parameter	Min	Typ	Max	Unit	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	VN0109	90			V $V_{GS} = 0, I_D = 1\text{mA}$
		VN0106	60			
		VN0104	40			
$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.4	V	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with Temperature		-3.8	-5.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1\text{mA}$
I_{GSS}	Gate Body Leakage			100	nA	$V_{GS} = \pm 20\text{V}, V_{DS} = 0$
I_{DSS}	Zero Gate Voltage Drain Current			1		$V_{GS} = 0, V_{DS} = \text{Max Rating}$ $V_{GS} = 0, V_{DS} = 0.8 \text{ Max Rating}$ $T_A = 125^\circ\text{C}$
				100	μA	
$I_{D(ON)}$	ON-State Drain Current	0.5	1.0		A	$V_{GS} = 5\text{V}, V_{DS} = 25\text{V}$ $V_{GS} = 10\text{V}, V_{DS} = 25\text{V}$
		2.0	2.5			
$R_{DS(ON)}$	Static Drain-to-Source ON-State Resistance		3.0	5	Ω	$V_{GS} = 5\text{V}, I_D = 250\text{mA}$ $V_{GS} = 10\text{V}, I_D = 1\text{A}$
			2.5	3		
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with Temperature		0.70	1	%/ $^\circ\text{C}$	$V_{GS} = 10\text{V}, I_D = 1\text{A}$
G_{FS}	Forward Transconductance	300	450		m Ω	$V_{DS} = 25\text{V}, I_D = 0.5\text{A}$
C_{ISS}	Input Capacitance		45	65	pF	$V_{GS} = 0, V_{DS} = 25\text{V}$ $f = 1\text{MHz}$
C_{OSS}	Common Source Output Capacitance		20	25		
C_{RSS}	Reverse Transfer Capacitance		5	8		
$t_{d(ON)}$	Turn-ON Delay Time		3	5	ns	$V_{DD} = 25\text{V}$ $I_D = 1\text{A}$ $R_{GEN} = 25\Omega$
t_r	Rise Time		5	8		
$t_{d(OFF)}$	Turn-OFF Delay Time		6	9		
t_f	Fall Time		5	8		
V_{SD}	Diode Forward Voltage Drop		1.2	1.8		
t_{rr}	Reverse Recovery Time		400		ns	$V_{GS} = 0, I_{SD} = 1.0\text{A}$

Notes:

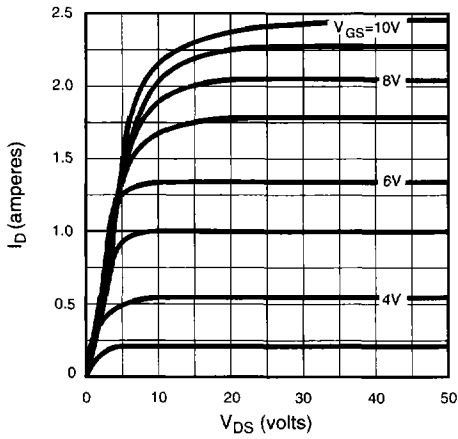
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

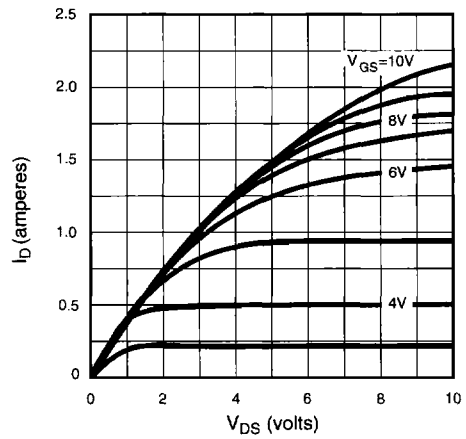


Typical Performance Curves

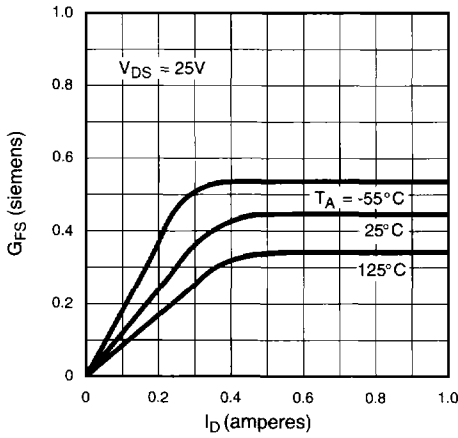
Output Characteristics



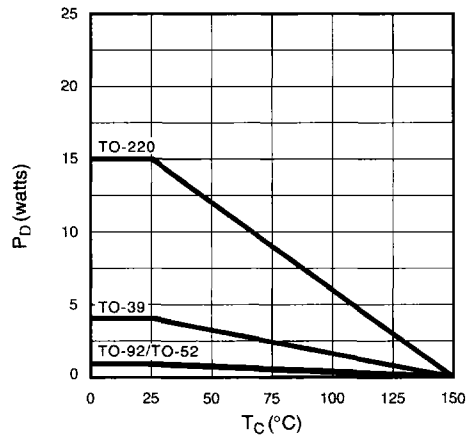
Saturation Characteristics



Transconductance vs. Drain Current

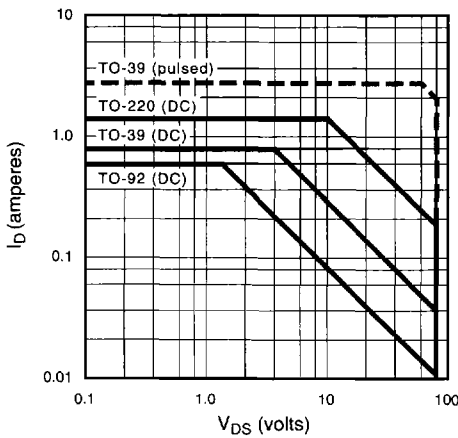


Power Dissipation vs. Case Temperature

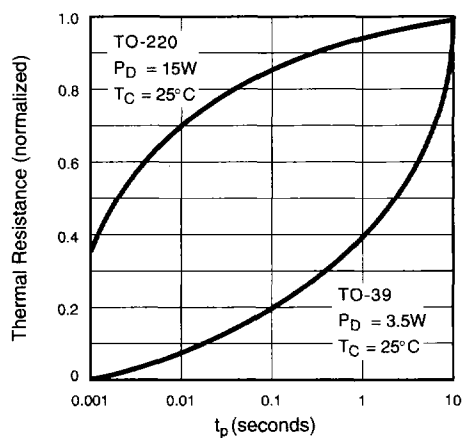


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Maximum Rated Safe Operating Area



Thermal Response Characteristics



Typical Performance Curves

