

SILICON GATE CMOS

524,288 WORD x 8 BIT CMOS PSEUDO STATIC RAM

Description

The TC518512PL is a 4M bit high speed CMOS pseudo static RAM organized as 524,288 words by 8 bits. The TC518512PL utilizes a one transistor dynamic memory cell with CMOS peripheral circuitry to provide high capacity, high speed and low power storage. The TC518512PL-LV operates from a single 3.0V ~ 5.5V power supply. Refreshing is supported by a refresh ($\overline{OE}/RFSH$) input which enables two types of refreshing - auto refresh and self refresh. The TC518512PL features a static RAM-like interface with a write cycle in which the input data is written into the memory cell at the rising edge of R/W thus simplifying the microprocessor interface.

The TC518512PL is available in a 32-pin, 0.6 inch width plastic DIP, a small outline plastic flat package, and a thin small outline package (forward type, reverse type).

Features

- Organization: 524,288 words x 8 bits
- Low voltage operation: 3.0V ~ 5.5V
- Data retention supply voltage: 3.0V ~ 5.5V
- Fast access time

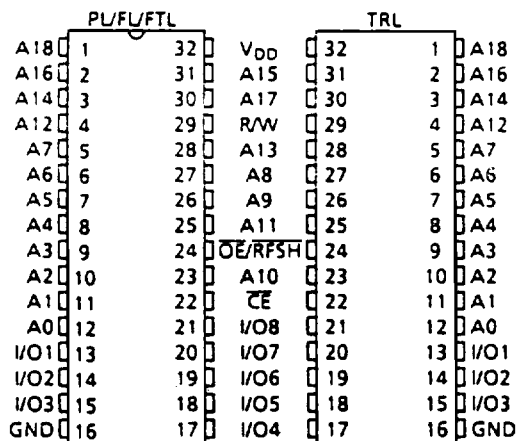
		TC518512PL-LV Family		
		-70	-80	-10
t_{CEA}	\overline{CE} Access Time	70ns	80ns	100ns
t_{OEA}	\overline{OE} Access Time	30ns	30ns	40ns
t_{RC}	Cycle Time	115ns	130ns	160ns
Power Dissipation		185mW	330mW	275mW
Self Refresh Current	5.5V	200 μ A		
Self Refresh Current	3.0V	100 μ A		

- Auto refresh is supported by an internal refresh address counter
- Self refresh is supported by an internal timer
- Inputs and outputs TTL compatible
- Refresh: 2048 refresh cycles/32ms
- Package
 - TC518512PL: DIP32-P-600
 - TC518512FL: SOP32-P-525
 - TC518512FTL: TSOP32-P-400
 - TC518512TRL: TSOP32-P-400A

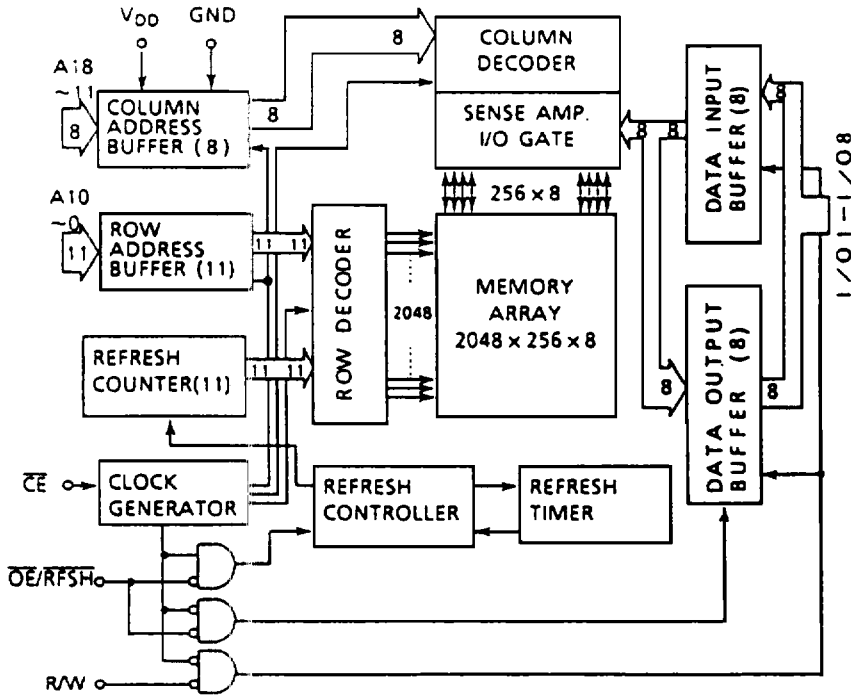
Pin Names

A0 ~ A18	Address Inputs
R/W	Read/Write Control Input
$\overline{OE}/RFSH$	Output Enable Input Refresh Input
\overline{CE}	Chip Enable Input
I/O1 ~ I/O8	Data Inputs/Outputs
V_{DD}	Power
GND	Ground

Pin Connection (Top View)



Block Diagram



Operating Mode

MODE	PIN	\overline{CE}	$\overline{OE}/RFSH$	R/W	A0 ~ A18	I/O1 ~ 8
Read		L	L	H	V*	OUT
Write		L	*	L	V*	IN
\overline{CE} only Refresh		L	H	H	V*	HZ
Auto/Self Refresh		H	L	*	*	HZ
Standby		H	H	*	*	HZ

H = High level input (V_{IH})

L = Low level input (V_{IL})

* = V_{IH} or V_{IL}

V* = At the falling edge of \overline{CE} , all address inputs are latched. At all other times, the address inputs are "**".

HZ = High impedance

Maximum Ratings

SYMBOL	ITEM	RATING	UNIT	NOTES
V_{IN}	Input Voltage	-1.0 ~ 7.0	V	1
V_{OUT}	Output Voltage	-1.0 ~ 7.0	V	
V_{DD}	Power Supply Voltage	-1.0 ~ 7.0	V	
T_{OPR}	Operating Temperature	0 ~ 70	°C	
T_{STRG}	Storage Temperature	-55 ~ 150	°C	
T_{SOLDER}	Soldering Temperature • Time	260 • 10	°C • sec	
P_D	Power Dissipation	600	mW	
I_{OUT}	Short Circuit Output Current	50	mA	

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V _{DD}	Power Supply Voltage	4.5	5.0	5.5	V	2
V _{IH}	Input High Voltage	2.4	–	V _{DD} + 1.0	V	
V _{IL}	Input Low Voltage	-1.0	–	0.8	V	

DC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 5V±10%)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES	
I _{DDO}	Operating Current (Average) CE, Address cycling t _{RC} = t _{RC} min.	70ns version	–	50	70	mA	3,4
		80ns version	–	45	60		
		100ns version	–	35	50		
I _{DDS1}	Standby Current CE = V _{IH} , OE/RFSH = V _{IH}	–	–	1	mA		
I _{DDS2}	Standby Current CE = V _{DD} - 0.2V, OE/RFSH = V _{DD} - 0.2V	–	–	200	μA		
I _{DDF1}	Self Refresh Current (Average) CE = V _{IH} , OE/RFSH = V _{IL}	–	–	1	mA		
I _{DDF2}	Self Refresh Current (Average) CE = V _{DD} - 0.2V, OE/RFSH = 0.2V	–	–	200	μA		
I _{DDF3}	Auto Refresh Current (Average) OE/RFSH cycling: t _{FC} = t _{FC} min.	70ns version	–	–	70	mA	3
		80ns version	–	–	60		
		100ns version	–	–	50		
I _{DDF4}	CE only Refresh Current (Average) CE, Address cycling t _{RC} = t _{RC} min.	70ns version	–	–	70	mA	3
		80ns version	–	–	60		
		100ns version	–	–	50		
I _{I(L)}	Input Leakage Current 0V ≤ V _{IN} ≤ V _{DD} , All other Inputs not under test = 0V	–	–	±10	μA		
I _{O(L)}	Output Leakage Current Output Disabled (CE = V _{IH} or OE/RFSH = V _{IH} or R/W = V _{IL}) 0V ≤ V _{OUT} ≤ V _{DD}	–	–	±10	μA		
V _{OH}	Output High Level I _{OH} = -1.0mA	2.4	–	–	V		
V _{OL}	Output Low Level I _{OL} = 2.1mA	–	–	0.4	V		

Capacitance* (V_{DD} = 5V, Ta = 25°C, f = 1MHz)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
C _{I1}	Input Capacitance (A0 ~ A18)	–	5	pF
C _{I2}	Input Capacitance (CE, OE/RFSH, R/W)	–	7	
C _{IO}	Input/Output Capacitance	–	7	

*This parameter is periodically sampled and is not 100% tested.

AC Characteristics (Ta = 0 ~ 70°C, VDD = 5V±10%) (Notes: 5, 6, 7, 8)

SYMBOL	PARAMETER	-70		-80		-10		UNIT	NOTES
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
t _{RC}	Random Read, Write Cycle Time	115	—	130	—	160	—	ns	
t _{RMW}	Read Modify Write Cycle Time	165	—	180	—	220	—		
t _{CE}	$\overline{\text{CE}}$ Pulse Width	70	10,000	80	10,000	100	10,000		
t _P	$\overline{\text{CE}}$ Precharge Time	35	—	40	—	50	—		
t _{CEA}	$\overline{\text{CE}}$ Access Time	—	70	—	80	—	100		
t _{OEa}	$\overline{\text{OE}}$ Access Time	—	30	—	30	—	40		
t _{CLZ}	$\overline{\text{CE}}$ to Output in Low-Z	20	—	20	—	20	—		
t _{OLZ}	$\overline{\text{OE}}$ to Output in Low-Z	0	—	0	—	0	—		
t _{WLZ}	Output Active from End of Write	0	—	0	—	0	—		
t _{CHZ}	Chip Disable to Output in High-Z	0	20	0	20	0	25		9
t _{OHZ}	$\overline{\text{OE}}$ Disable to Output in High-Z	0	20	0	20	0	25		9
t _{WHZ}	Write Enable to Output in High-Z	0	20	0	20	0	25		9
t _{OSC}	$\overline{\text{OE}}$ Setup Time Referenced to $\overline{\text{CE}}$	10	—	10	—	10	—		9
t _{OHc}	$\overline{\text{OE}}$ Hold Time Referenced to $\overline{\text{CE}}$	0	—	0	—	0	—		9
t _{RCS}	Read Command Setup Time	0	—	0	—	0	—		
t _{RCH}	Read Command Hold Time	0	—	0	—	0	—		
t _{WP}	Write Pulse Width	25	—	25	—	30	—		
t _{WCH}	Write Command Hold Time	40	—	40	—	50	—		
t _{CWL}	Write Command to $\overline{\text{CE}}$ Lead Time	25	—	25	—	30	—		
t _{DSW}	Data Setup Time from R/W	20	—	20	—	25	—		10
t _{DSC}	Data Setup Time from $\overline{\text{CE}}$	20	—	20	—	25	—		10
t _{DHW}	Data Hold Time from R/W	0	—	0	—	0	—		10
t _{DHC}	Data Hold Time from $\overline{\text{CE}}$	0	—	0	—	0	—		10
t _{ASC}	Address Setup Time	0	—	0	—	0	—		11
t _{AHC}	Address Hold Time	15	—	20	—	25	—		11
t _{FC}	Auto Refresh Cycle Time	130	—	130	—	160	—		
t _{RFD}	RFSH Delay Time from $\overline{\text{CE}}$	40	—	40	—	50	—		
t _{FAP}	RFSH Pulse Width (Auto Refresh)	30	8,000	30	8,000	30	8,000	12	
t _{FP}	RFSH Precharge Time	30	—	30	—	30	—	12	
t _{FAS}	RFSH Pulse Width (Self Refresh)	8,000	—	8,000	—	8,000	—	12	
t _{FRS}	$\overline{\text{CE}}$ Delay Time from RFSH (Self Refresh)	160	—	160	—	190	—	12	
t _{REF}	Refresh Period (2048 cycles, A0 ~ A10)	—	32	—	32	—	32	ms	
t _T	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	

3.3V Operation

DC Recommended Operating Conditions

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
V_{DD}	Power Supply Voltage	3.0	3.3	3.6	V	2
V_{IH}	Input High Voltage	$V_{DD} - 0.2V$	-	$V_{DD} + 1.0$	V	
V_{IL}	Input Low Voltage	-0.5	-	0.2	V	

DC Characteristics ($T_a = 0 \sim 70^\circ C$, $V_{DD} = 3.3V \pm 0.3V$)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT	NOTES
I_{DDO}	Operating Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	-	15	20	mA	3,4
I_{DDs2}	Standby Current	-	-	100	μA	
I_{DDF2}	Self Refresh Current (Average)	-	50	100	μA	
I_{DDF3}	Auto Refresh Current (Average) RFSH cycling: $t_{FC} = t_{FC \text{ min.}}$	-	-	20	mA	3
I_{DDF4}	\overline{CE} only Refresh Current (Average) \overline{CE} , Address cycling: $t_{RC} = t_{RC \text{ min.}}$	-	-	20	mA	3
$I_{I(L)}$	Input Leakage Current $0V \leq V_{IN} \leq V_{DD}$, All other Inputs not under test = 0V	-	-	± 10	μA	
$I_{O(L)}$	Output Leakage Current Output Disabled, $0V \leq V_{OUT} \leq V_{DD}$	-	-	± 10	μA	
V_{OH}	Output High Level, $I_{OH} = -100\mu A$	-	$V_{DD} - 0.2V$	-	V	
V_{OL}	Output Low Level, $I_{OL} = 100\mu A$	-	-	0.2	V	

AC Characteristics (Ta = 0 ~ 70°C, V_{DD} = 3.3V±0.3V) (Notes: 5, 6, 8)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTES
t _{RC}	Random Read, Write Cycle Time	230	–		
t _{RMW}	Read Modify Write Cycle Time	305	–		
t _{CE}	\overline{CE} Pulse Width	150	10,000		
t _p	\overline{CE} Precharge Time	80	–		
t _{CEA}	\overline{CE} Access Time	–	150		
t _{OEa}	\overline{OE} Access Time	–	80		
t _{CLZ}	\overline{CE} to Output in Low -Z	20	–		
t _{OLZ}	\overline{OE} to Output in Low -Z	5	–		
t _{WLZ}	Output Active from End of Write	5	–		
t _{CHZ}	Chip Disable to Output in High-Z	0	30		9
t _{OHZ}	\overline{OE} Disable to Output in High-Z	0	30		9
t _{WHZ}	Write Enable to Output in High-Z	0	30		9
t _{OSC}	\overline{OE} Setup Time Referenced to \overline{CE}	10	–		9
t _{OHC}	\overline{OE} Hold Time Referenced to \overline{CE}	15	–		9
t _{RCS}	Read Command Setup Time	0	–		
t _{RCH}	Read Command Hold Time	0	–	ns	
t _{WP}	Write Pulse Width	35	–		
t _{WCH}	Write Command Hold Time	70	–		
t _{CWL}	Write Command to \overline{CE} Lead Time	35	–		
t _{DSW}	Data Setup Time from R/W	30	–		10
t _{DSC}	Data Setup Time from \overline{CE}	30	–		10
t _{DHw}	Data Hold Time from R/W	0	–		10
t _{DHC}	Data Hold Time from \overline{CE}	0	–		10
t _{ASC}	Address Setup Time	0	–		11
t _{AHC}	Address Hold Time	30	–		11
t _{FC}	Auto Refresh Cycle Time	230	–		
t _{RFD}	\overline{RFSH} Delay Time from \overline{CE}	80	–		
t _{FAP}	\overline{RFSH} Pulse Width (Auto Refresh)	80	8,000		12
t _{FP}	\overline{RFSH} Precharge Time	50	–		12
t _{FAS}	\overline{RFSH} Pulse Width (Self Refresh)	8,000	–		12
t _{FRS}	\overline{CE} Delay Time from \overline{RFSH} (Self Refresh)	300	–		12
t _{REF}	Refresh Period (2048 cycles, A0 ~ A10)	–	32	ms	
t _T	Transition Time (Rise and Fall)	3	50	ns	

Timing Reference Levels:

Input Reference Levels: 1.5V/1.5V

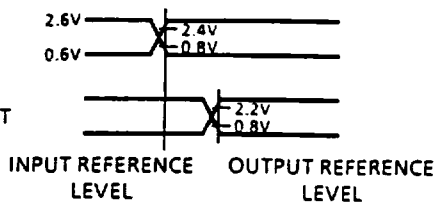
Output Reference Levels: 1.5V/1.5V

Notes:

- 1) Stress greater than those listed under "Maximum Ratings" may cause permanent damage to the device.
- 2) All voltages are referenced to GND.
- 3) I_{DD0} , I_{DD3} , and I_{DD4} depend on the cycle time.
- 4) I_{DD0} depends on the output loading. Specified values are obtained with the outputs open.
- 5) An initial pause of 100 μ s with high \overline{CE} is required after power-up before proper device operation is achieved.
- 6) AC measurements assume $t_T = 5$ ns.

7) Timing reference levels

Input Levels	:	$V_{IH} = 2.6V$ $V_{IL} = 0.6V$	INPUT
Input Reference Levels	:	$V_{IH} = 2.4V$ $V_{IL} = 0.8V$	OUTPUT
Output Reference Levels	:	$V_{OH} = 2.2V$ $V_{OL} = 0.8V$	



- 8) Measured with a load equivalent to 1 TTL load and 100pF.
- 9) t_{CHZ} , t_{OHZ} , t_{WHZ} define the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- 10) For write cycles, the input data is latched at the earlier of \overline{RW} or \overline{CE} rising edge. Therefore, the input data must be valid during the setup time (t_{DSW} or t_{DSC}) and hold time (t_{DHW} or t_{DHC}).
- 11) All address inputs are latched at the falling edge of \overline{CE} . Therefore, all the address inputs must be valid during t_{ASC} and t_{AHC} .
- 12) The two refresh operations, auto refresh and self refresh, are defined by the \overline{RFSH} pulse width under the condition $\overline{CE} = V_{IH}$.
 Auto refresh : \overline{RFSH} pulse width $\leq t_{FAP}$ (max.)
 Self refresh : \overline{RFSH} pulse width $\geq t_{FAS}$ (min.)

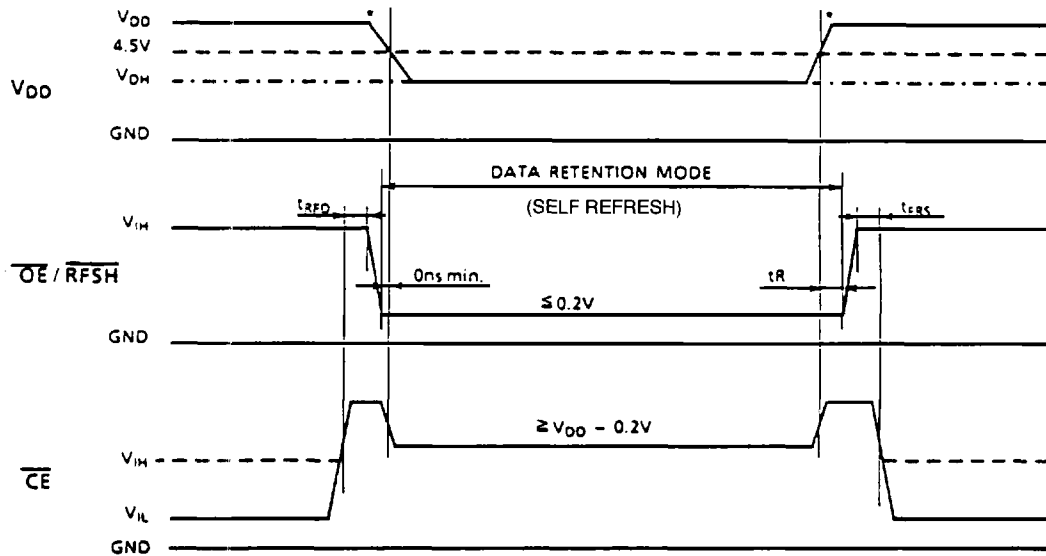
The timing parameter t_{FRS} must be met for proper device operation under the following conditions:

- after self refresh
- if $\overline{OE}/\overline{RFSH} = "L."$ after power-up

Data Retention Characteristics (Ta = 0 ~ 70°C)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
V _{DH}	Data Retention Supply Voltage	3.0	-	5.5	V
I _{DDF2}	Self Refresh Current	V _{DH} = 3.0V	-	50	μA
		V _{DH} = 5.5V	-	100	
t _R	Recovery Time	5	-	-	ms

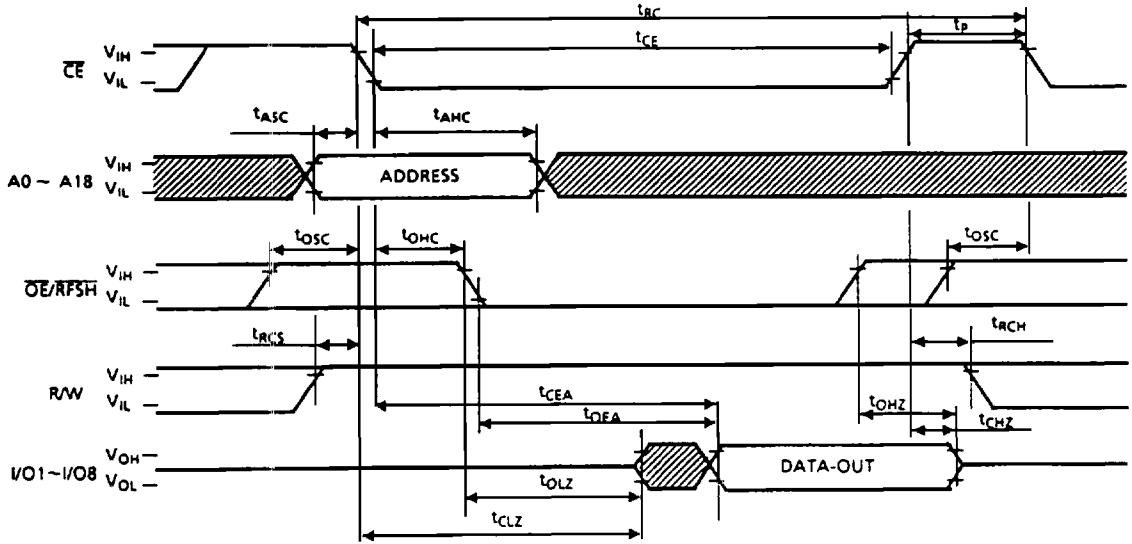
*The rising and falling slope of V_{DD} must be more than 50ms for proper device operation (20ms/V).



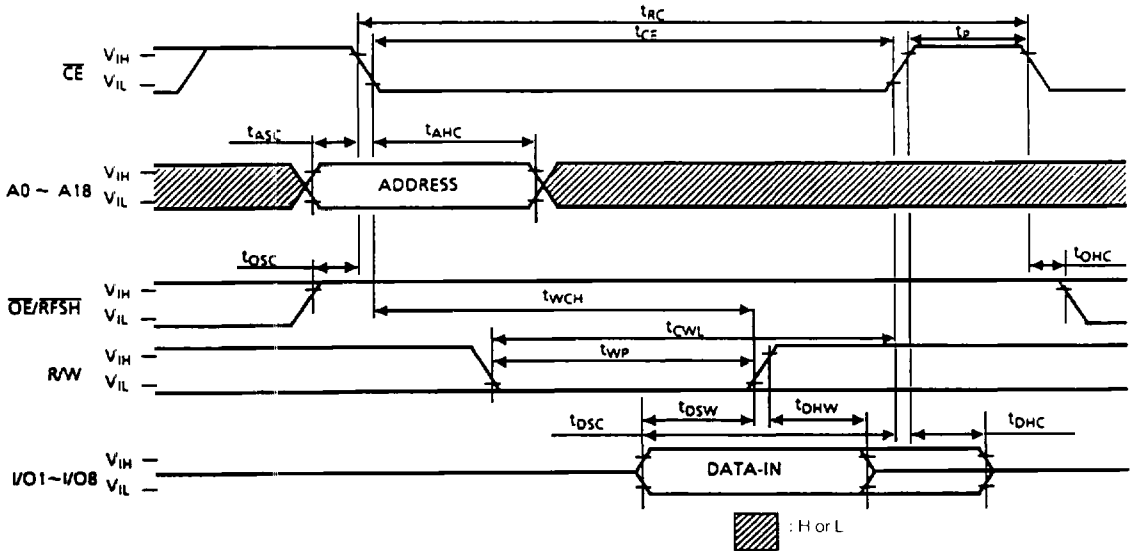
Notes: R/W, A0 ~ A18 = V_{IH} or V_{IL}
 I_{DDF1} is applicable when OE/RFSH = V_{IL} (max.), CE = V_{IH} (min.).

Timing Waveforms

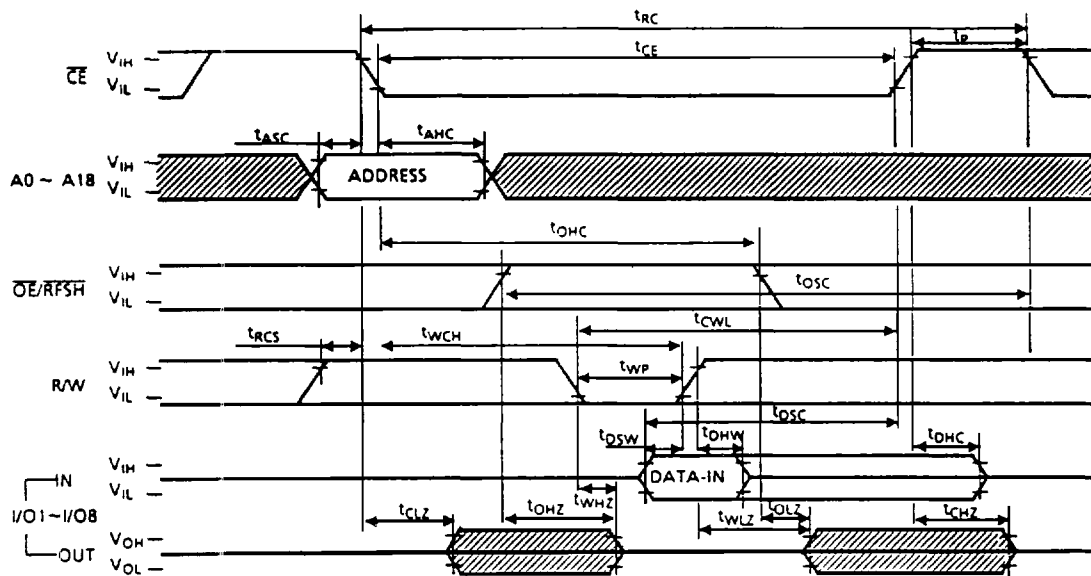
Read Cycle



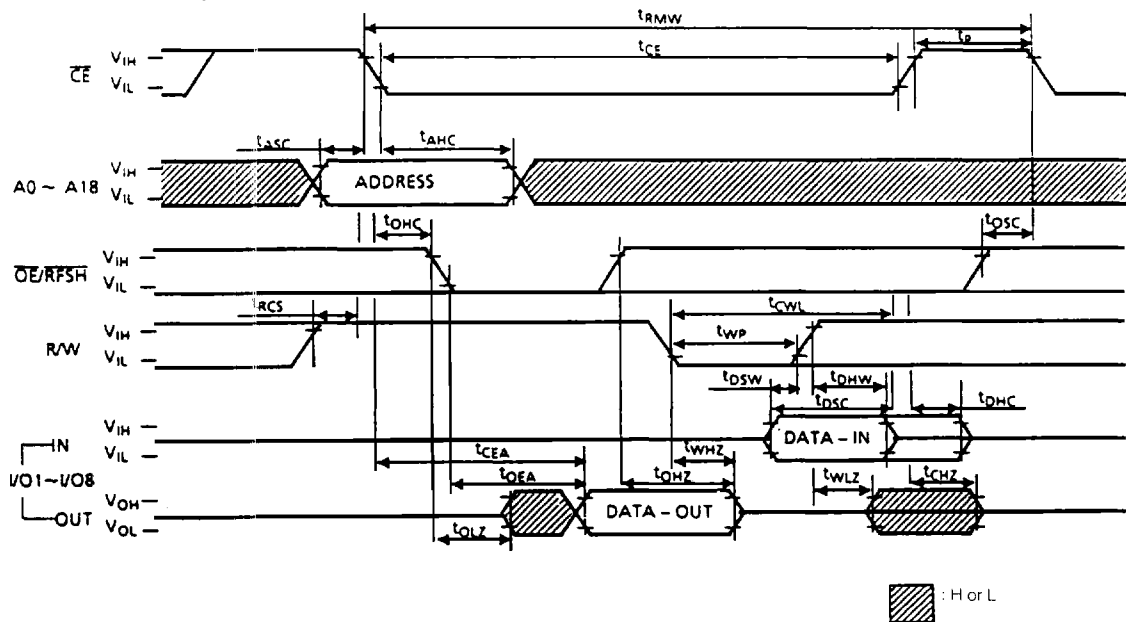
Write Cycle 1 (OE Fixed High)



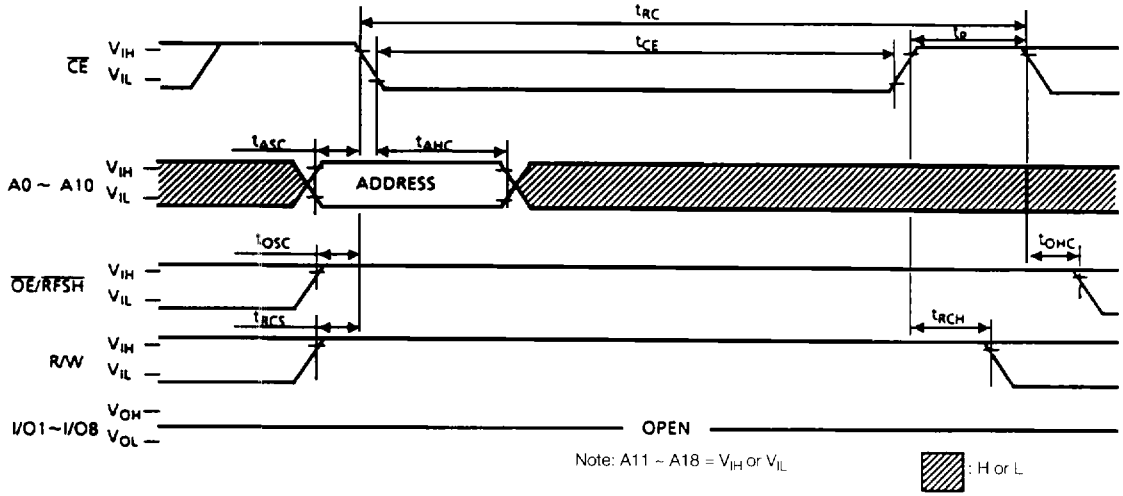
Write Cycle 2 (\overline{OE} Clocked or Fixed Low)



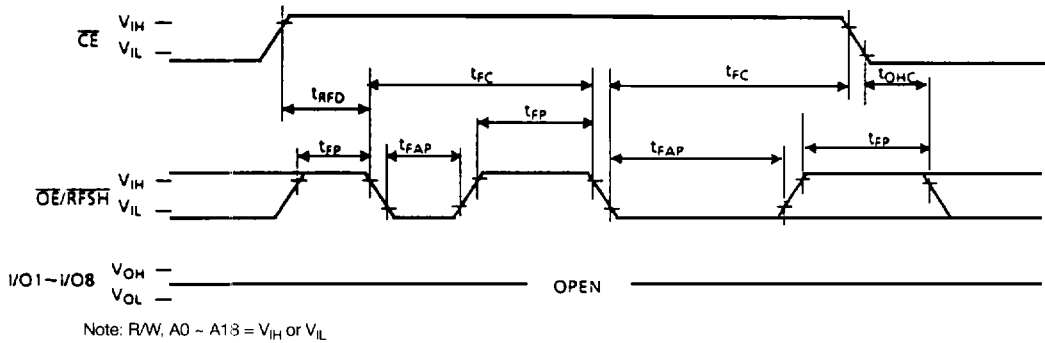
Read Modify Write Cycle



CE Only Refresh



Auto Refresh



Self Refresh

