plerow™ ALUC2535B3

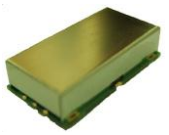
Internally Matched Balanced LNA Module Including Coupler

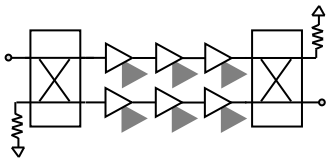
Features

- S_{21} = 34.4 dB@2500 MHz
  = 33.6 dB@2570 MHz
- NF of 0.75 dB over Frequency
- Unconditionally Stable
- Single 5 V Supply
- High OIP3@Low Current
- 3-stage Balanced Type

Description

RoHS-compliant





3-stage Balanced Type

Specifications (in Production)

Typ.@T = 25 °C, V_s = 5 V, Freq. = 2535 MHz, $Z_{o.sys}$ = 50 ohms

Parameter	Unit	Specifications		
		Min	Typ	Max
Frequency Range	MHz	2500		2570
Gain	dB	33	34	
Gain Flatness	dB		±0.4	±0.5
Noise Figure	dB		0.75	0.80
Output IP3 (1)	dBm	39	40	
S11/S22 (2)	dB			-20/-20
Output P1dB	dBm	23	24	
Switching Time (3)	μsec		-	
Supply Current	mA		340	380
Supply Voltage	V		5	
Impedance	Ω		50	
Max. RF Input Power	dBm		C.W 29~31(before fail)	
Package Type & Size	mm		Surface Mount Type, 22Wx12Lx5H	

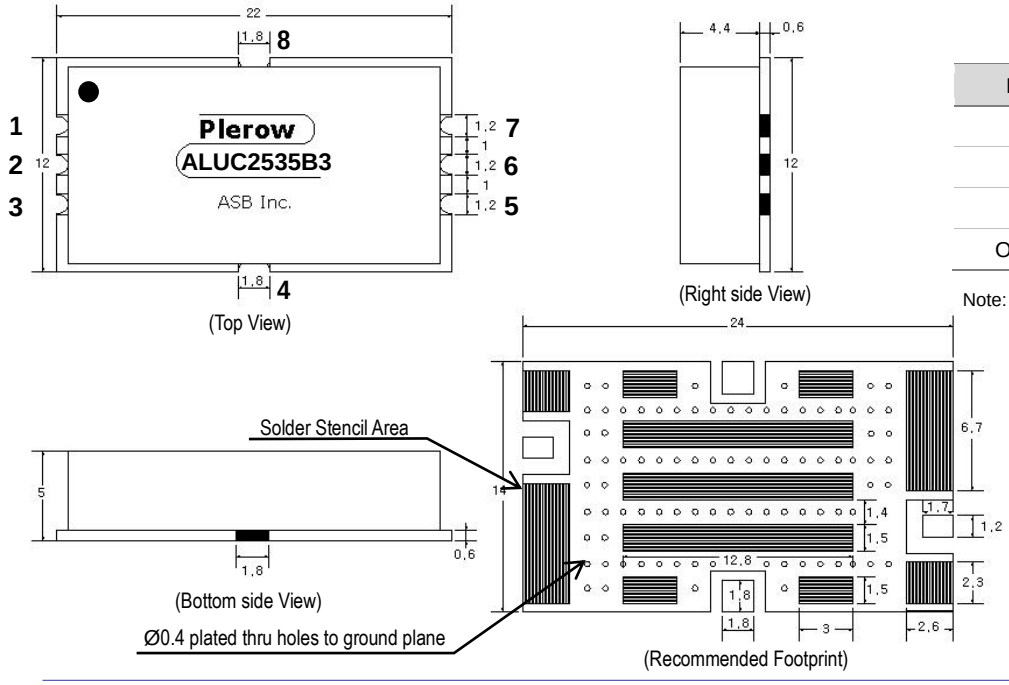
Operating temperature is –40 °C to +85 °C.
1) OIP3 is measured with two tones at an output power of +7 dBm/tone separated by 1 MHz.
2) S11, S22(max) is the worst value within the frequency band.
3) Switching time means the time that takes for output power to get stabilized to its final level after switching DC voltage from 0 V to V_S.

More Information

Website: www.asb.co.kr
E-mail: sales@asb.co.kr

Tel: (82) 42-528-7223
Fax: (82) 42-528-7222

Outline Drawing (Unit: mm)



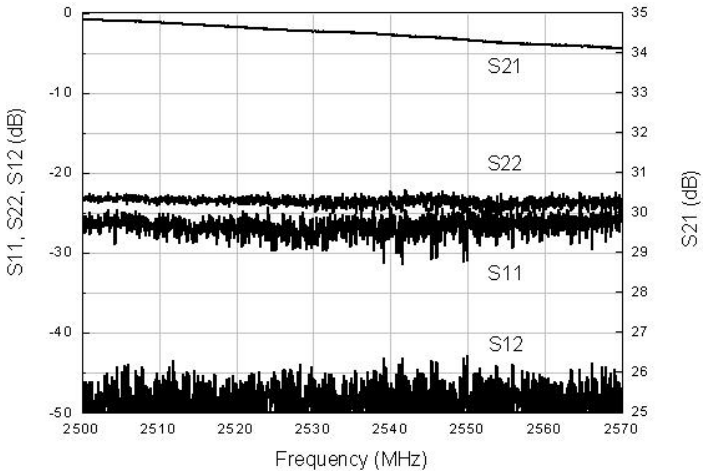
Port Number	Function
1	RF In
5	RF Out
4, 8	Vs
Others, Bottom	GND

Note: 1. The number and size of ground via holes in a circuit board is critical for thermal RF grounding considerations.
2. We recommend that the ground via holes be placed on the bottom of all ground pins for better RF and thermal performance, as shown in the drawing at the left side.

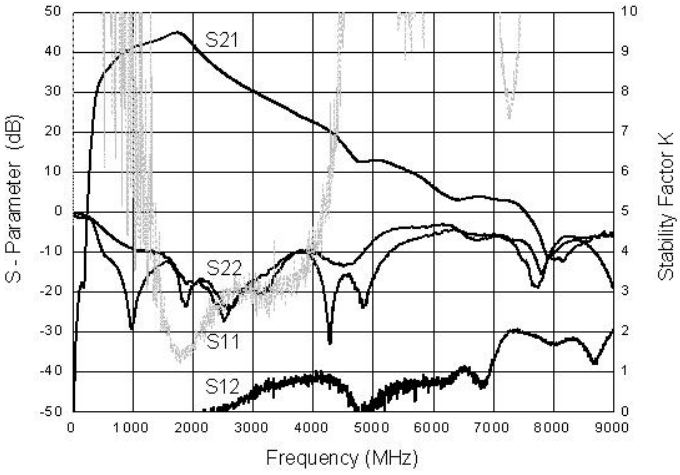
Typical Performance (Measured)

2500~2570 MHz
+5 V

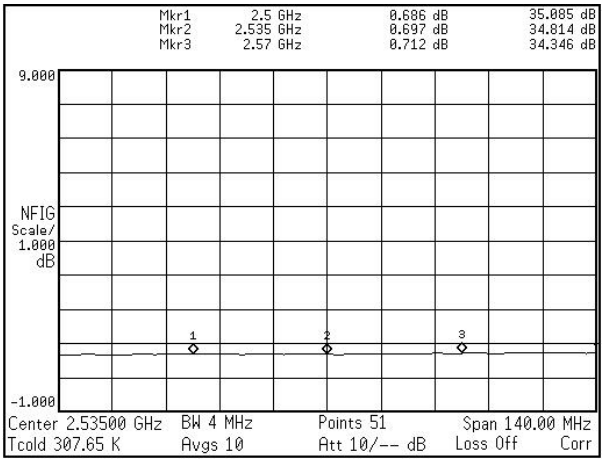
S-parameters



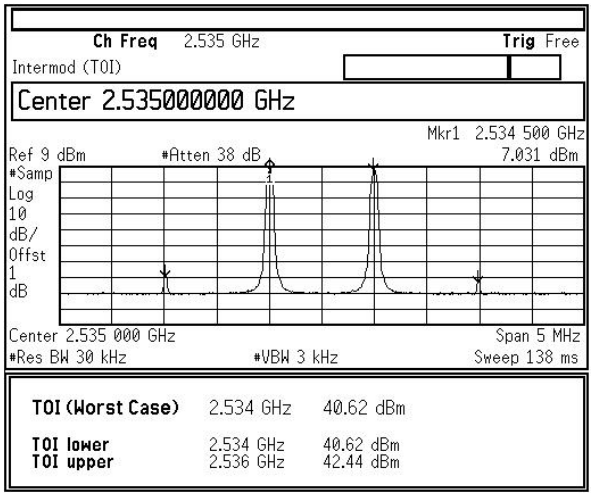
S-parameters & K Factor



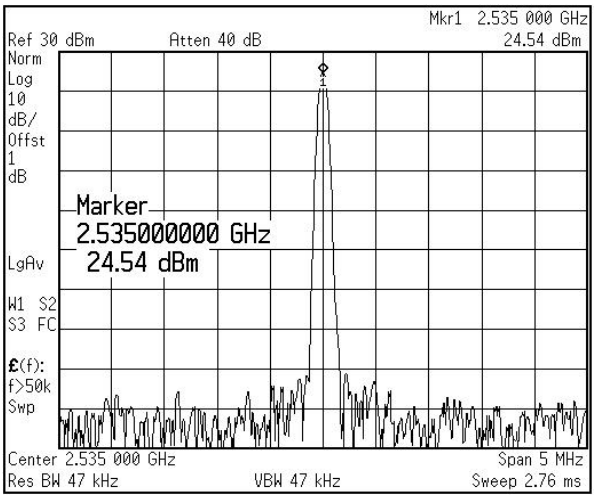
Noise Figure



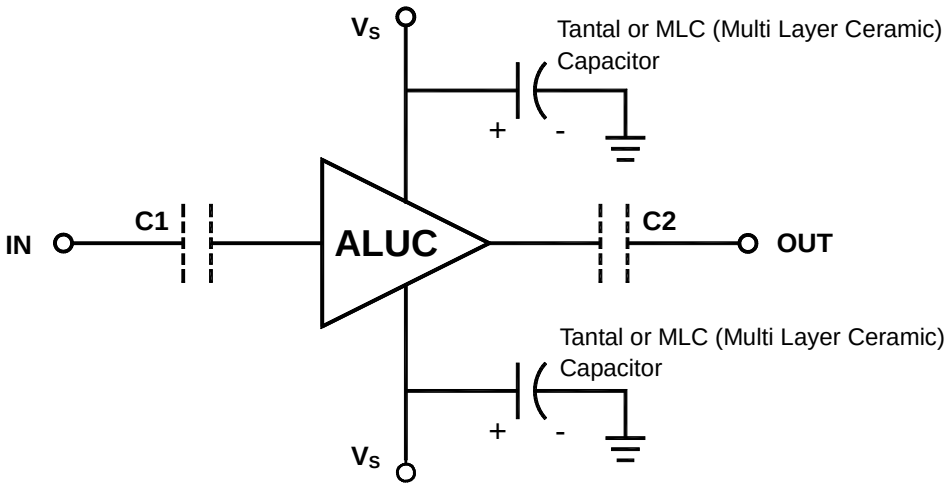
OIP3



P1dB



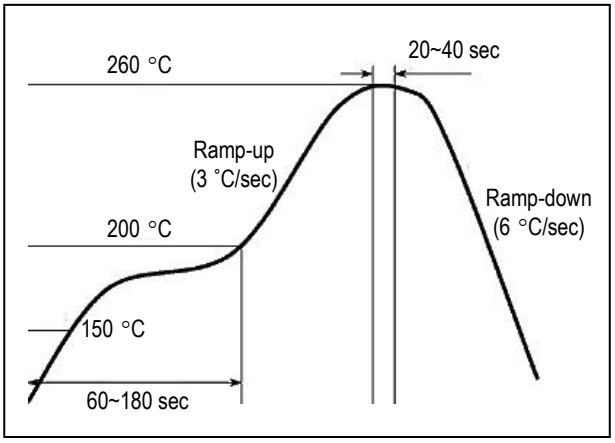
Application Circuit



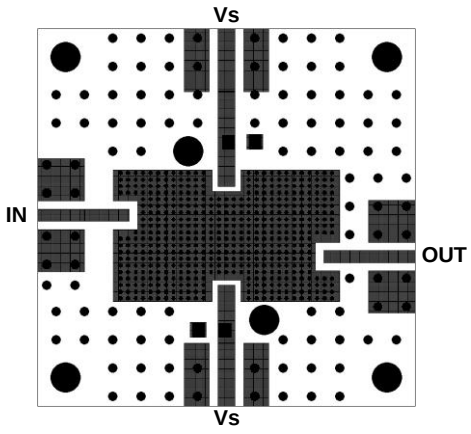
1) The tantal or MLC (Multi Layer Ceramic) capacitor is optional and for bypassing the AC noise introduced from the DC supply. The capacitance value may be determined by customer's DC supply status. The capacitor should be placed as close as possible to V_s pin and be connected directly to the ground plane for the best electrical performance.

2) DC blocking capacitors are always necessarily placed at the input and output port for allowing only the RF signal to pass and blocking the DC component in the signal. The DC blocking capacitors are included inside the ALN module. Therefore, C1 & C2 capacitors may not be necessary, but can be added just in case that the customer wants. The value of C1 & C2 is determined by considering the application frequency.

Recommended Soldering Reflow Process



Evaluation Board Layout



Size 40x40 mm
(for ALUC Series – 22x12 mm)