HD64180S (NPU)

Network Processing Unit (NPU)
CMOS 8-bit Microprocessor for Communications Applications

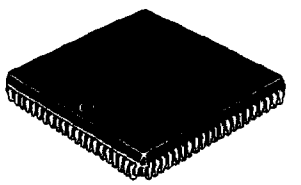
Description

The HD64180S Network Processing Unit (NPU) provides multi-purpose high-speed communication control functions on a single LSI chip. The HD64180S allows efficient, high-performance communication protocol and user application processing at a low cost.

Built-in features of the HD64180S include an 8-bit CPU, a 2-channel serial interface (MSCI, ASCI/CSIO), a DMAC with 2-channel chained block transfer capabilities, and a timer. The MSCI provides asynchronous, byte synchronous, and bit synchronous communication modes, and enables serial communications using protocols such as HDLC. The built-in features of the HD64180S allow it to control communication using various protocols as well as application processing. In distributed environments, communication throughput can be increased by eliminating the need for the main processor to do communication processing.

The built-in features of the HD64180S also make it flexible. Applications range from a communication subsystem processor for inter-computer links or an ISDN protocol processor to a controller in a distributed control system for industrial robots.

In addition, the HD64180S is designed to interface with conventional communication LSIs and to be compatible with existing communication software. It can be used with almost any type of communication system.

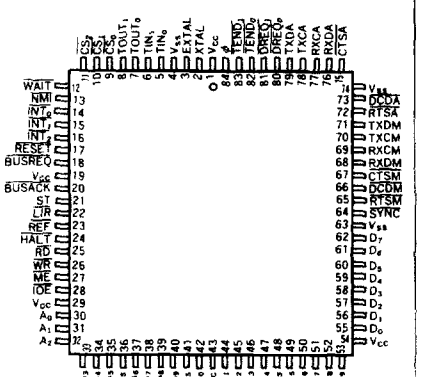


(CP-84)

*For details about HD64180S specifications, please refer to "HD64180S NPU Hardware Manual" (Order Number M21T022).

The absolute maximum ratings are limiting values, to be applied individually, beyond which the device may be permanently damaged. Functional operation under any of these conditions is *not guaranteed*. Exposing a circuit to its absolute maximum rating for extended periods of time may affect the device's reliability.

Pin Arrangement



(Top View)

Characteristics

Item	Specifications
CPU	• Software compatible with HD64180Z • 80 type bus interface • On-chip MMU (1 Mbyte physical address space)
DMAC	• 2 channels • DMA transfer between memory and memory, memory and I/O (memory-mapped I/O), and memory and MSCI • Chained-block transfer between memory and MSCI • Internal interrupt requests av ailable
Multiprotocol serial communications interface (MSCI)	• Full duplex channel • Asynchronous, byte synchronous (mono-, Bi-, or external synchronous), or bit synchronous (HDLC or loop) selectable • Transmit/receive control using modem control signals ($\overline{\text{RTSM}}$, $\overline{\text{CTSM}}$, and $\overline{\text{DCDM}}$) • Internal Advanced Digital PLL (ADPLL) clock extraction receive data and/or receive clock noise suppression • On-chip baud rate generator • Internal interrupt requests available • Maximum transfer rate 7.1 Mbps (with 10 MHz clock)
Asynchronous serial communications interface/clocked serial I/O port (ASCI/CSIO)	• Full duplex channel • Asynchronous or clocked serial mode (selectable) • Transmit/receive control using modem control signals ($\overline{\text{RTSA}}$, $\overline{\text{CTSA}}$, and $\overline{\text{DCDA}}$) • On-chip baud rate generator • Internal interrupt requests available
Timers	• 2 channels • 8-bit reloadable up-counter • Output waveform generator and external event count functions • Internal interrupt requests available
Interrupt controller	• Four external interrupt lines ($\overline{\text{NMI}}$, $\overline{\text{INT}_0}$, $\overline{\text{INT}_1}$, and $\overline{\text{INT}_2}$) • Fifteen internal interrupt sources
Memory access support function	• Internal refresh controller • Internal wait state controller • Internal chip-select controller
Other functions	• On-chip clock oscillator circuit • Low power dissipation modes (sleep and system stop)

Ordering Information

Product Name	Max Operating Frequency	Package
HD64180SCP6	6 MHz	CP-84 (84-pin PLCC)
HD64180SCP8	8 MHz	
HD64180SCP10	10 MHz	

Signal Functions

Type	Mnemonic	I/O	Function
Power Supply	Vcc	I	Power supply
	Vss	I	Ground
Clock	XTAL	I	Crystal
	EXTAL	I	External clock
	ø	O	System clock
Reset	$\overline{\text{RESET}}$	I	Reset
Address Bus	$A_0 - A_{19}$	O	Address bus
Data Bus	$D_0 - D_7$	I/O	Data bus
Memory I/O	$\overline{\text{RD}}$	O	Read
Interface	$\overline{\text{WR}}$	O	Write
	$\overline{\text{ME}}$	O	Memory enable
	$\overline{\text{IOE}}$	O	I/O enable
	$\overline{\text{WAIT}}$	I	Wait request
	$\overline{\text{CS}}_0 - \overline{\text{CS}}_2$	O	Programmable chip-select
System Control	$\overline{\text{BUSREQ}}$	I	Bus request
	$\overline{\text{BUSACK}}$	O	Bus request acknowledge
	$\overline{\text{HALT}}$	O	Halt
	$\overline{\text{LIR}}$	O	Opcode fetch
	ST	O	Status
	$\overline{\text{REF}}$	O	Refresh
Interrupt Control	$\overline{\text{NMI}}$	I	Non-maskable interrupt
	$\overline{\text{INT}}_0 - \overline{\text{INT}}_2$	I	Interrupt request
DMAC	$\overline{\text{DREQ}}_0$, $\overline{\text{DREQ}}_1$	I	DMA request (channel 0, 1)
	$\overline{\text{TEND}}_0$, $\overline{\text{TEND}}_1$	O	DMA end (channel 0, 1)
MSCI	TXDM	O	Transmit data
	RXDM	I	Receive data
	TXCM	I/O	Transmit clock
	RXCM	I/O	Receive clock
	$\overline{\text{RTSM}}$	O	Modem control
	$\overline{\text{DCDM}}$	I	
	$\overline{\text{CTSM}}$	I	
	$\overline{\text{SYNC}}$	I/O	Synchronization
ASCI/CSIO	TXDA	O	Transmit data
	RXDA	I	Receive data
	TXCA	I/O	Transmit clock
	RXCA	I/O	Receive clock
	$\overline{\text{RTSA}}$	O	Modem control
	$\overline{\text{DCDA}}$	I	
	$\overline{\text{CTSA}}$	I	
Timer	TIN_0, TIN_1	I	Event input (channel 0, 1)
	TOUT_0, TOUT_1	O	Timer output (channel 0, 1)

Block Diagram