



## P-Channel Enhancement-Mode Vertical DMOS FETs

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{ISS}$  and fast switching speeds
- ▶ High input impedance and high gain
- ▶ Excellent thermal stability
- ▶ Integral source-to-drain diode

### Applications

- ▶ Motor controls
- ▶ Converters
- ▶ Amplifiers
- ▶ Switches
- ▶ Power supply circuits
- ▶ Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

### General Description

The Supertex VP0808 is an enhancement-mode (normally-off) transistor that utilizes a vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors, and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Ordering Information

| Device | Package   | $BV_{DSS}/BV_{DGS}$<br>(V) | $R_{DS(ON)}$<br>(max)<br>( $\Omega$ ) | $I_{D(ON)}$<br>(min)<br>(A) |
|--------|-----------|----------------------------|---------------------------------------|-----------------------------|
|        | TO-92     |                            |                                       |                             |
| VP0808 | VP0808L-G | -80                        | 5.0                                   | -1.1                        |

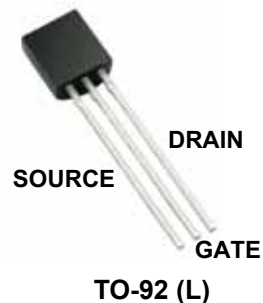
*For packaged products, -G indicates package is RoHS compliant ("Green").  
Consult factory for die / wafer form part numbers.  
Refer to Die Specification VF25 for layout and dimensions.*

### Absolute Maximum Ratings

| Parameter                         | Value                             |
|-----------------------------------|-----------------------------------|
| Drain-to-source voltage           | $BV_{DSS}$                        |
| Drain-to-gate voltage             | $BV_{DGS}$                        |
| Gate-to-source voltage            | $\pm 30V$                         |
| Operating and storage temperature | $-55^{\circ}C$ to $+150^{\circ}C$ |

*Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.*

### Pin Configuration



### Product Marking



YY = Year Sealed  
 WW = Week Sealed  
 \_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or TO-92 (L)

### Thermal Characteristics

| Package | $I_D$<br>(continuous) <sup>†</sup><br>(mA) | $I_D$<br>(pulsed)<br>(A) | Power Dissipation<br>@ $T_c = 25^\circ\text{C}$<br>(W) | $\theta_{jc}$<br>( $^\circ\text{C}/\text{W}$ ) | $\theta_{ja}$<br>( $^\circ\text{C}/\text{W}$ ) | $I_{DR}^\dagger$<br>(mA) | $I_{DRM}$<br>(mA) |
|---------|--|--------------------------|--|--|--|--------------------------|-------------------|
| TO-92   | -280                                       | -3.0                     | 1.0  | 125  | 170  | -280                     | -3.0              |

**Notes:**

<sup>†</sup>  $I_D$  (continuous) is limited by max rated  $T_j$ .

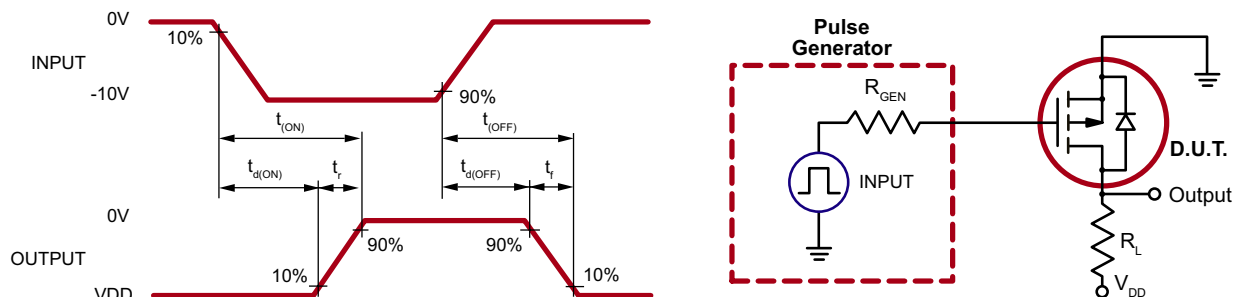
### Electrical Characteristics ( $T_A = 25^\circ\text{C}$ unless otherwise specified)

| Sym          | Parameter                                  | Min  | Typ  | Max  | Units         | Conditions  |
|--------------|--|------|------|------|---------------|---|
| $BV_{DSS}$   | Drain-to-source breakdown voltage          | -80  | -    | -    | V             | $V_{GS} = 0V, I_D = -10\mu\text{A}$                                     |
| $V_{GS(th)}$ | Gate threshold voltage                     | -1.0 | -    | -4.5 | V             | $V_{GS} = V_{DS}, I_D = -1.0\text{mA}$                                  |
| $I_{GSS}$    | Gate body leakage current                  | -    | -    | -100 | nA            | $V_{GS} = \pm 20V, V_{DS} = 0V$   |
| $I_{DSS}$    | Zero gate voltage drain current            | -    | -    | -10  | $\mu\text{A}$ | $V_{GS} = 0V, V_{DS} = \text{Max Rating}$                               |
|              |  | -    | -    | -500 |               | $V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$ |
| $I_{D(ON)}$  | On-state drain current                     | -1.1 | -    | -    | A             | $V_{GS} = -10V, V_{DS} = -15V$  |
| $R_{DS(ON)}$ | Static drain-to-source on-state resistance | -    | -    | 5.0  | $\Omega$      | $V_{GS} = -10V, I_D = -1.0A$  |
| $G_{FS}$     | Forward transconductance                   | 200  | -    | -    | mmho          | $V_{DS} = -10V, I_D = -500\text{mA}$                                    |
| $C_{ISS}$    | Input capacitance                          | -    | -    | 150  | pF            | $V_{GS} = 0V,$<br>$V_{DS} = -25V,$<br>$f = 1.0\text{MHz}$               |
| $C_{OSS}$    | Common source output capacitance           | -    | -    | 60   |               |   |
| $C_{RSS}$    | Reverse transfer capacitance               | -    | -    | 25   |               |   |
| $t_{d(ON)}$  | Turn-on time                               | -    | -    | 15   | ns            | $V_{DD} = -25V,$<br>$I_D = -500\text{mA},$<br>$R_{GEN} = 25\Omega$      |
| $t_r$        | Rise time                                  | -    | -    | 40   |               |   |
| $t_{d(OFF)}$ | Turn-off time                              | -    | -    | 30   |               |   |
| $t_f$        | Fall time                                  | -    | -    | 30   |               |   |
| $V_{SD}$     | Diode forward voltage drop                 | -    | -1.2 | -    | V             | $V_{GS} = 0V, I_{SD} = -900\text{mA}$                                   |

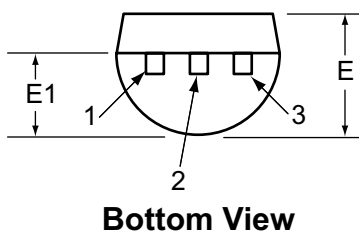
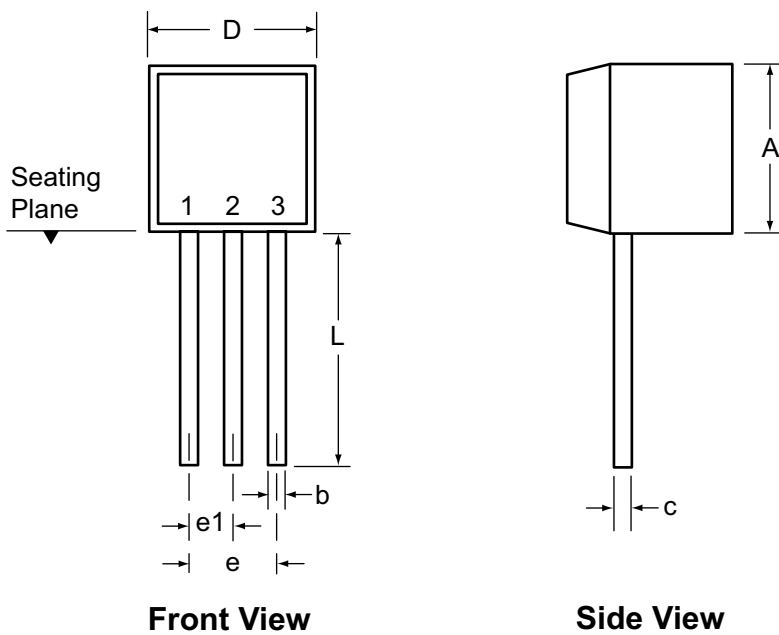
**Notes:**

1. All D.C. parameters 100% tested at  $25^\circ\text{C}$  unless otherwise stated. (Pulse test:  $300\mu\text{s}$  pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

### Switching Waveforms and Test Circuit



### 3-Lead TO-92 Package Outline (L)



| Symbol              | A   | b    | c     | D     | E    | E1   | e    | e1   | L    |       |
|---------------------|-----|------|-------|-------|------|------|------|------|------|-------|
| Dimensions (inches) | MIN | .170 | .014† | .014† | .175 | .125 | .080 | .095 | .045 | .500  |
|                     | NOM | -    | -     | -     | -    | -    | -    | -    | -    | -     |
|                     | MAX | .210 | .022† | .022† | .205 | .165 | .105 | .105 | .055 | .610* |

JEDEC Registration TO-92.

\* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

**Supertex inc.** does not recommend the use of its products in life support applications, and will not knowingly sell them for use in such applications unless it receives an adequate "product liability indemnification insurance agreement." **Supertex inc.** does not assume responsibility for use of devices described, and limits its liability to the replacement of the devices determined defective due to workmanship. No responsibility is assumed for possible omissions and inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications refer to the **Supertex inc.** (website: <http://www.supertex.com>)