Operational Amplifier / Comparator Series

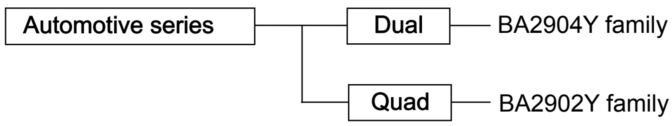
Automotive Operational Amplifiers: Ground Sense

BA2904YF-C,BA2904YFVM-C,BA2902YF-C,BA2902YFV-C

No.11049EAT23

●Description

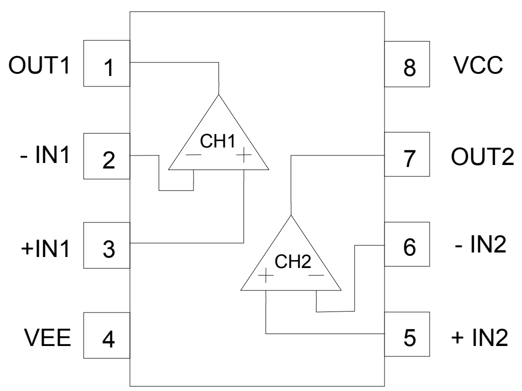
Automotive series BA2904Y family and BA2902Y family integrate two or four independent Op-Amps and phase compensation capacitors on a single chip and have some features of high-gain, low power consumption, and operating voltage range of 3[V] to 32[V] (single power supply).

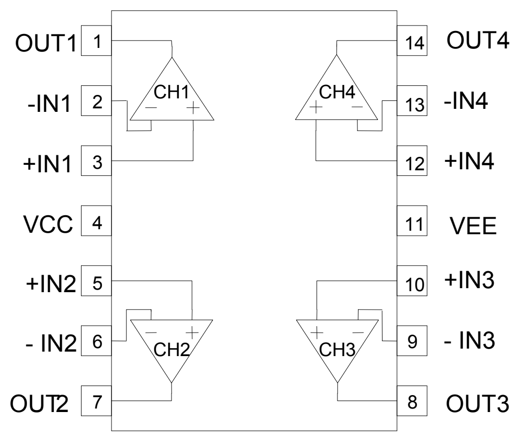


●Features

1) Operable with a single power supply
2) Wide operating supply voltage
   +3.0[V]～+32.0[V](single supply)
3) Standard Op-Amp Pin-assignments
4) Input and output are operable GND sense
5) Internal phase compensation type
6) Low supply current
7) High open loop voltage gain
8) Internal ESD protection
   Human body model (HBM) ±5000[V](Typ.)
9) Wide temperature range
   -40[℃]～+125[℃]

●Pin Assignment





SOP8	MSOP8	SOP14	SSOP-B14
BA2904YF-C	BA2904YFVM-C	BA2902YF-C	BA2902YFV-C

●**Absolute Maximum Ratings** (Ta=25[℃])

○BA2904Y family , BA2902Y family

Parameter	Symbol	Ratings	Unit
		BA2904Y, BA2902Y	
Supply Voltage	VCC-VEE	+36	V
Differential Input Voltage (*1)	Vid	36	V
Input Common-mode Voltage Range	Vicm	(VEE-0.3)～(VEE+36)	V
Operating Temperature Range	Topr	-40～+125	℃
Storage Temperature Range	Tstg	-55～+150	℃
Maximum Junction Temperature	Tjmax	+150	℃

Note: Absolute maximum rating item indicates the condition which must not be exceeded.
Application if voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

(*1) The voltage difference between inverting input and non-inverting input is the differential input voltage.
Then input terminal voltage is set to more than VEE.

●Electric Characteristics

○BA2904Y family (Unless otherwise specified VCC=+5[V], VEE=0[V])

Parameter	Symbol	Temperature Range	Limits Min.	Limits Typ.	Limits Max.	Unit	Conditions
Input Offset Voltage (*2)	Vio	25℃	-	2	7	mV	VOUT=1.4[V]
		Full range	-	-	7		VCC=5～30[V], VOUT=1.4[V]
Input Offset Current (*2)	Iio	25℃	-	2	50	nA	VOUT=1.4[V]
		Full range	-	-	100		
Input Bias Current (*2)	Ib	25℃	-	20	60	nA	VOUT=1.4[V]
		Full range	-	-	100		
Supply Current	ICC	25℃	-	0.7	1.2	mA	RL=∞All Op-Amps
		Full range	-	-	1.2		
High Level Output Voltage	VOH	25℃	3.5	-	-	V	RL=2[kΩ]
		Full range	3.2	-	-		
			27	28	-		VCC=30[V],RL=10[kΩ]
Low Level Output Voltage	VOL	Full range	-	5	20	mV	RL=∞All Op-Amps
Large Signal Voltage Gain	AV	25℃	25	100	-	V/mV	RL≧2[kΩ],VCC=15[V] VOUT=1.4～11.4[V]
		Full range	25	-	-		
Input Common-mode Voltage range	Vicm	25℃	0	-	VCC-1.5	V	(VCC-VEE)=5V, VOUT=VEE+1.4[V]
		Full range	0	-	VCC-2.0		
Common-mode Rejection Ratio	CMRR	25℃	65	80	-	dB	VOUT=1.4[V]
Power Supply Rejection Ratio	PSRR	25℃	65	100	-	dB	VCC=5~30[V]
Output Source Current (*3)	IOH	25℃	20	30	-	mV	VIN+=1[V],VIN-=0[V] VOUT=0[V] 1CH is short circuit
		Full range	10	-	-		
Output Source Current (*3)	IOL	25℃	10	20	-	mA	VIN+=0[V],VIN-=1[V] VOUT=5[V] 1CH is short circuit
		Full range	2	-	-		
	Isink	25℃	12	40	-	μA	VIN+=0[V],VIN-=1[V] VOUT=200[mV]

(*2) Absolute value

(*3) Under high temperatures, please consider the power dissipation when selecting the output current.
When the output terminal is continuously shorted the output current reduces the internal temperature by flushing.

○BA2902Y family (Unless otherwise specified VCC=+5[V], VEE=0[V])

Parameter	Symbol	Temperature Range	Limits			Unit	Conditions
			Min.	Typ.	Max.		
Input Offset Voltage (*4)	Vio	25℃	-	2	7	mV	VOUT=1.4[V]
		Full range	-	-	7		VCC=5～30[V], VOUT=1.4[V]
Input Offset Current (*4)	Iio	25℃	-	2	50	nA	VOUT=1.4[V]
		Full range	-	-	100		
Input Bias Current (*4)	Ib	25℃	-	20	60	nA	VOUT=1.4[V]
		Full range	-	-	100		
Supply Current	ICC	25℃	-	0.7	2	mA	RL=∞ All Op-Amps
		Full range	-	-	3		
High Level Output Voltage	VOH	25℃	3.5	-	-	V	RL=2[kΩ]
		Full range	3.2	-	-		
			27	28	-		VCC=30[V],RL=10[kΩ]
Low Level Output Voltage	VOL	Full range	-	5	20	mV	RL=∞All Op-Amps
Large Signal Voltage Gain	AV	25℃	25	100	-	V/mV	RL≧2[kΩ],VCC=15[V] VOUT=1.4～11.4[V]
		Full range	25	-	-		
Input Common-mode Voltage range	Vicm	25℃	0	-	VCC-1.5	V	(VCC-VEE)=5V, VOUT=VEE+1.4[V]
		Full range	0	-	VCC-2.0		
Common-mode Rejection Ratio	CMRR	25℃	65	80	-	dB	VOUT=1.4[V]
Power Supply Rejection Ratio	PSRR	25℃	65	100	-	dB	VCC=5~30[V]
Output Source Current (*5)	IOH	25℃	20	30	-	mV	VIN+=1[V],VIN-=0[V] VOUT=0[V] 1CH is short circuit
		Full range	10	-	-		
Output Source Current (*5)	IOL	25℃	10	20	-	mA	VIN+=0[V],VIN-=1[V] VOUT=5[V] 1CH is short circuit
		Full range	2	-	-		
	Isink	25℃	12	40	-	μA	VIN+=0[V],VIN-=1[V] VOUT=200[mV]

(*4) Absolute value
(*5) Under high temperatures, please consider the power dissipation when selecting the output current.
When the output terminal is continuously shorted the output current reduces the internal temperature by flushing.

●Reference Data BA2904Y family

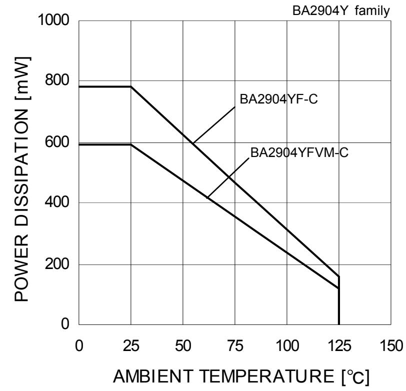


Fig. 1
Derating Curve

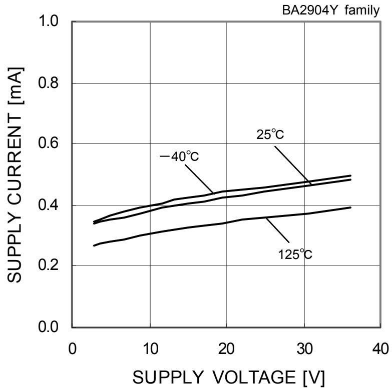


Fig. 2
Supply Current – Supply Voltage

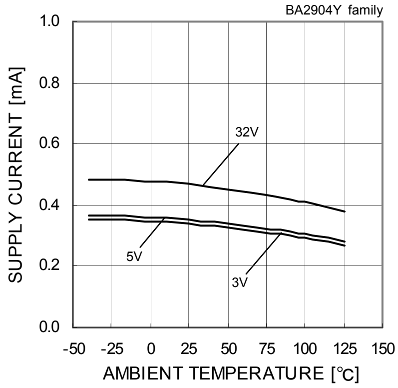


Fig. 3
Supply Current – Ambient Temperature

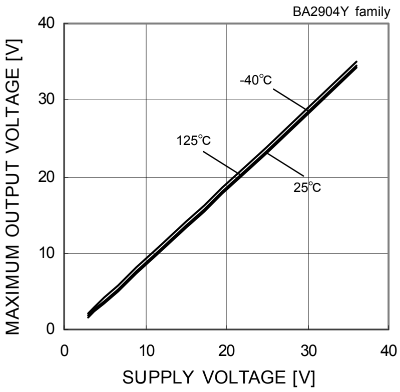


Fig. 4
Maximum Output Voltage – Supply Voltage
(RL=10[kΩ])

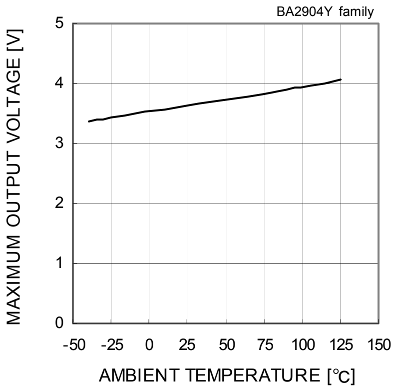


Fig. 5
Maximum Output Voltage – Ambient Temperature
(VCC=5[V],RL=2[kΩ])

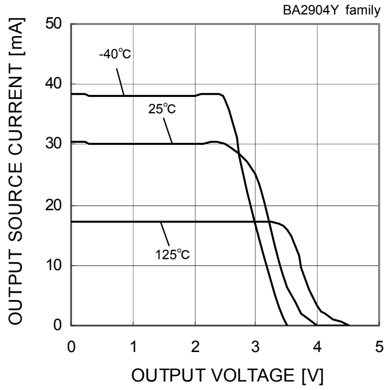


Fig. 6
Output Source Current – Output Voltage
(VCC=5[V])

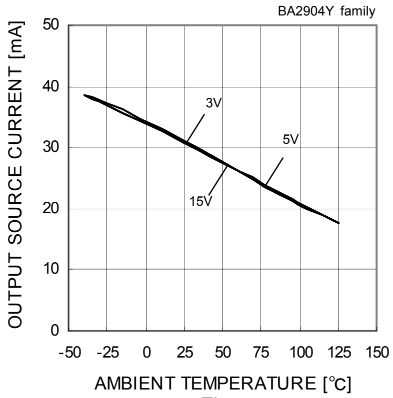


Fig. 7
Output Source Current – Ambient Temperature
(VOUT=0[V])

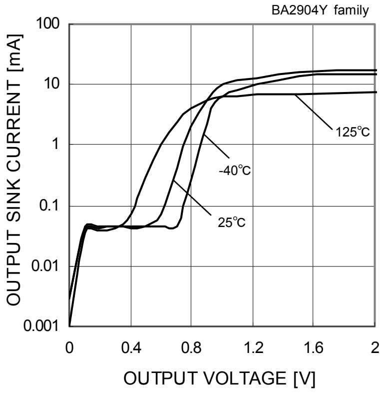


Fig. 8
Output Sink Current – Output Voltage
(VCC=5[V])

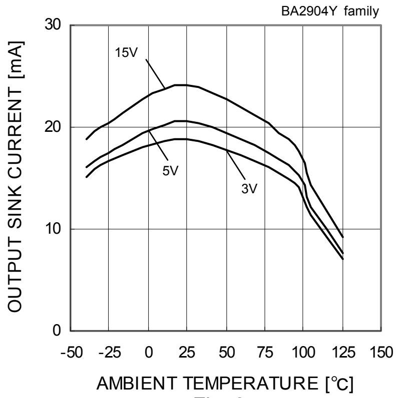


Fig. 9
Output Sink Current – Ambient Temperature
(VOUT=VCC)

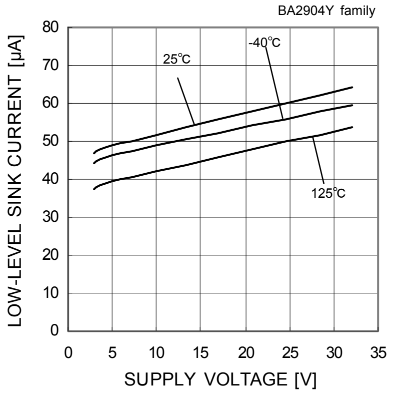


Fig. 10
Low Level Sink Current – Supply Voltage
(VOUT=0.2[V])

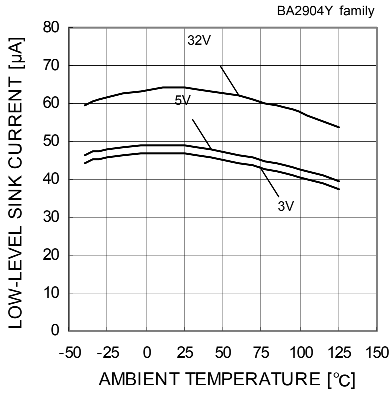


Fig. 11
Low Level Sink Current – Ambient Temperature
(VOUT=0.2[V])

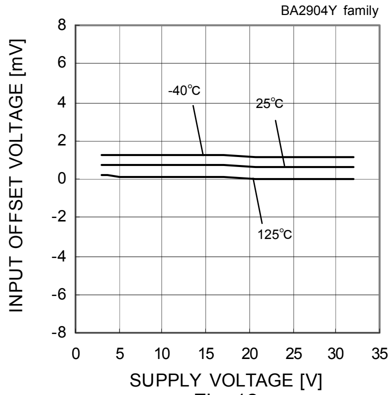


Fig. 12
Input Offset Voltage – Supply Voltage
(Vicm=0[V], VOUT=1.4[V])

(*)The data above is ability value of sample, it is not guaranteed.

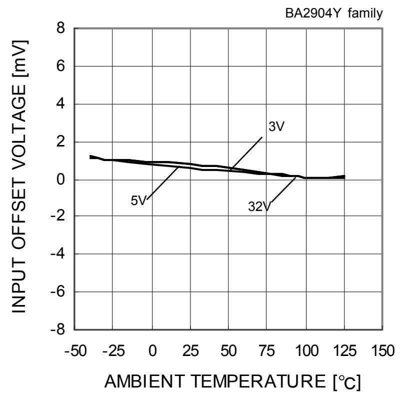


Fig. 13

Input Offset Voltage – Ambient Temperature
(Vicm=0[V], VOUT=1.4[V])

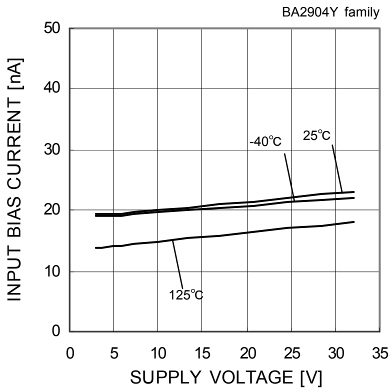


Fig. 14

Input Bias Current – Supply Voltage
(Vicm=0[V], VOUT=1.4[V])

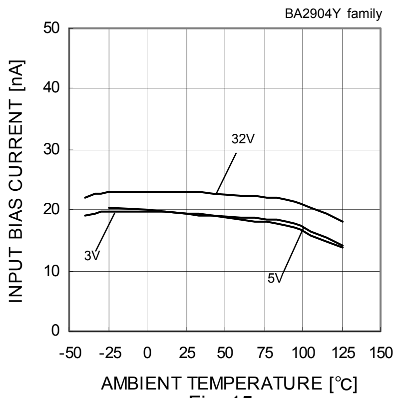


Fig. 15

Input Bias Current – Ambient Temperature
(Vicm=0[V],VOUT=1.4[V])

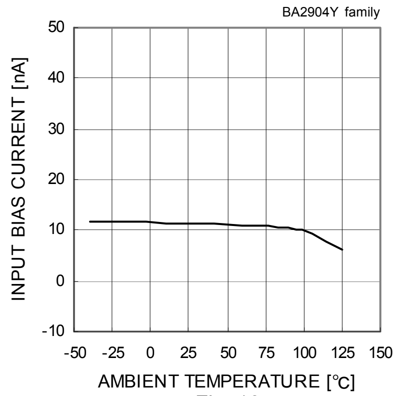


Fig. 16

Input Bias Current – Ambient Temperature
(VCC=30[V],Vicm=28[V],VOUT=1.4[V])

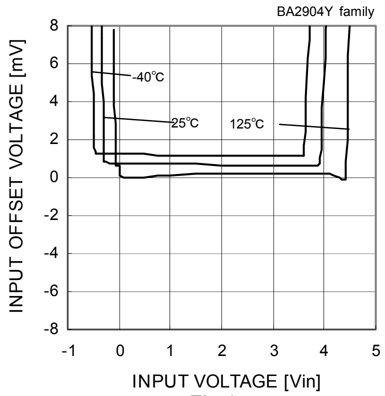


Fig.17

Input Offset Voltage – Input Voltage
(VCC=5[V])

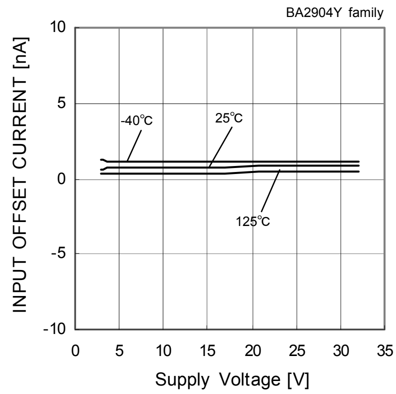


Fig. 18

Input Offset Current – Supply Voltage
(Vicm=0[V],VOUT=1.4[V])

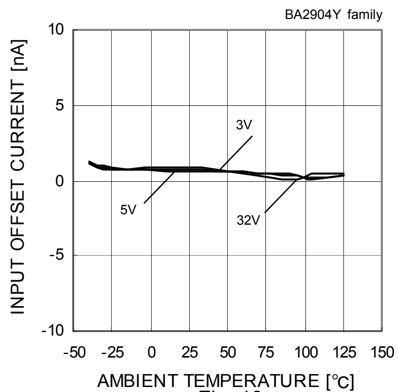


Fig. 19

Input Offset Current – Ambient Temperature
(Vicm=0[V],VOUT=1.4[V])

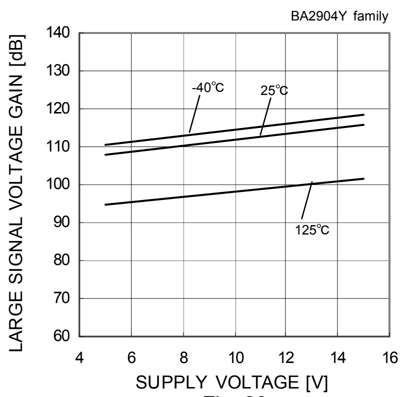


Fig. 20

Large Signal Voltage Gain – Supply Voltage(RL=2[kΩ])

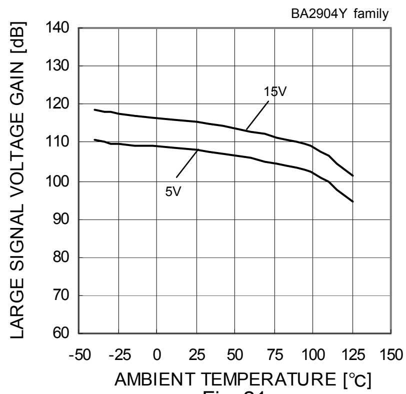


Fig. 21

Large Signal Voltage Gain – Ambient Temperature
(RL=2[kΩ])

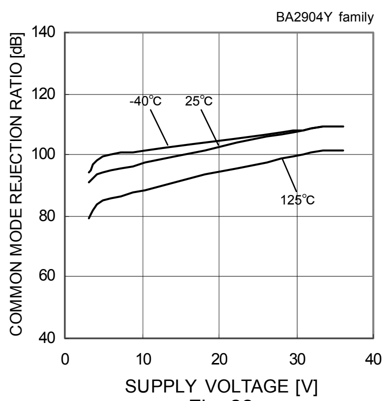


Fig. 22

Common Mode Rejection Ratio
– Supply Voltage

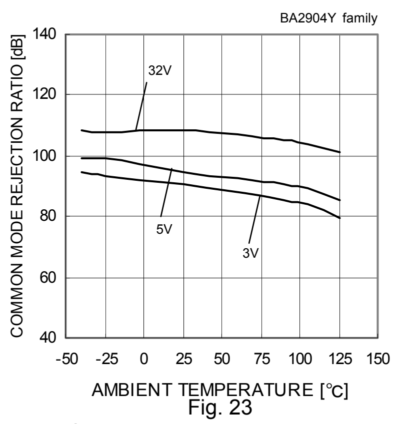


Fig. 23

Common Mode Rejection Ratio
– Ambient Temperature

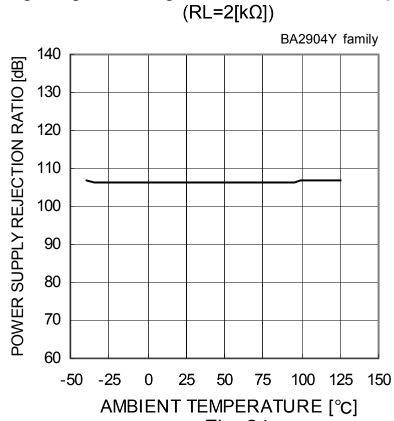


Fig. 24

Power Supply Rejection Ratio
– Ambient Temperature

(*)The data above is ability value of sample, it is not guaranteed.

● Reference Data BA2902Y family

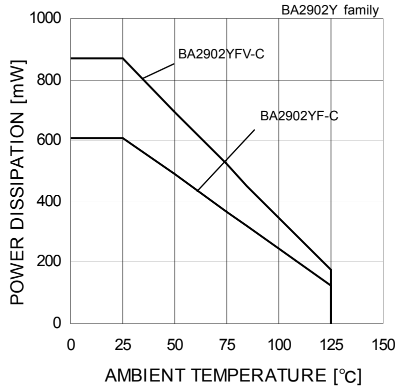


Fig. 25
Derating Curve

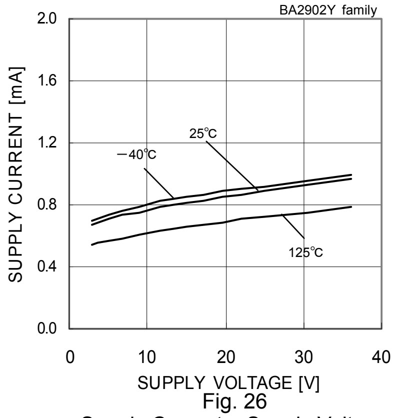


Fig. 26
Supply Current – Supply Voltage

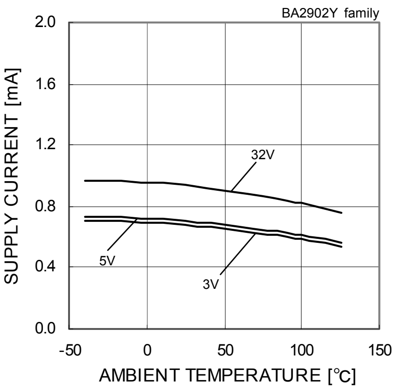


Fig. 27
Supply Current – Ambient Temperature

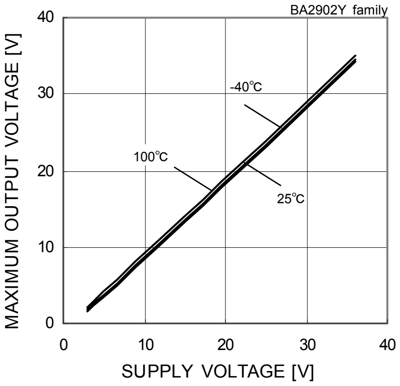


Fig. 28
Maximum Output Voltage – Supply Voltage
(RL=10[kΩ])

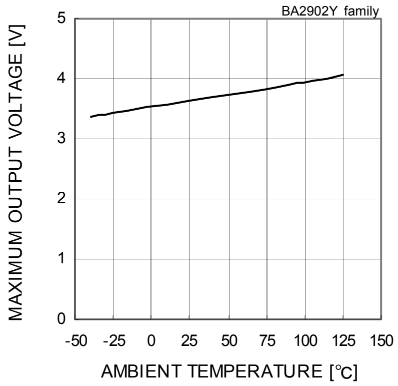


Fig. 29
Maximum Output Voltage – Ambient Temperature
(VCC=5[V],RL=2[kΩ])

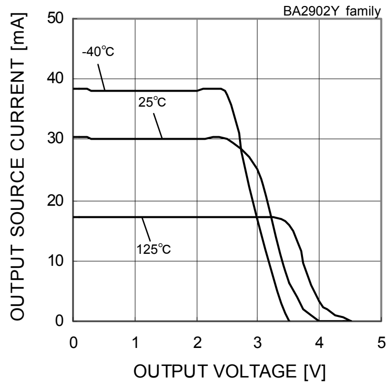


Fig. 30
Output Source Current – Output Voltage
(VCC=5[V])

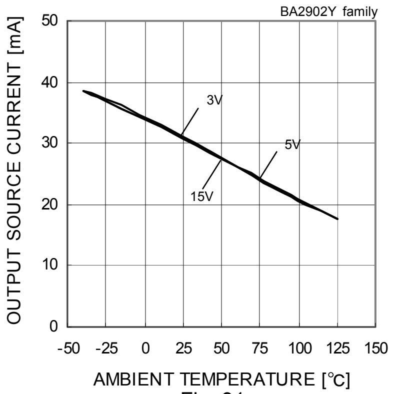


Fig. 31
Output Source Current – Ambient Temperature
(VOUT=0[V])

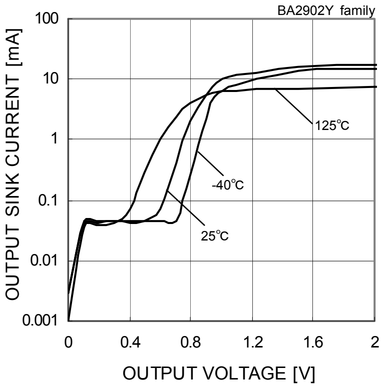


Fig. 32
Output Sink Current – Output Voltage
(VCC=5[V])

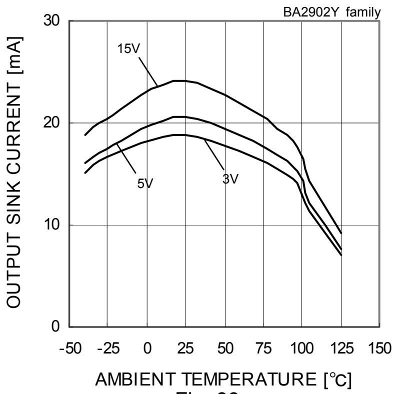


Fig. 33
Output Sink Current – Ambient Temperature
(VOUT=VCC)

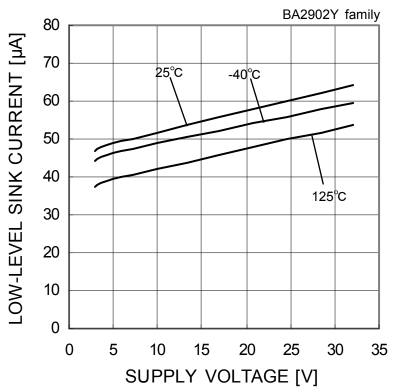


Fig. 34
Low Level Sink Current – Supply Voltage
(VOUT=0.2[V])

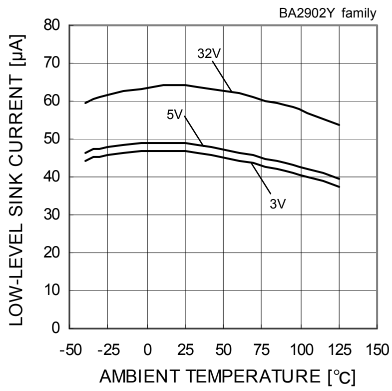


Fig. 35
Low Level Sink Current – Ambient Temperature
(VOUT=0.2[V])

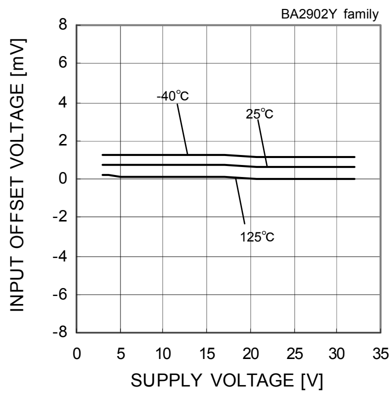


Fig. 36
Input Offset Voltage – Supply Voltage
(Vicm=0[V], VOUT=1.4[V])

(*)The data above is ability value of sample, it is not guaranteed.

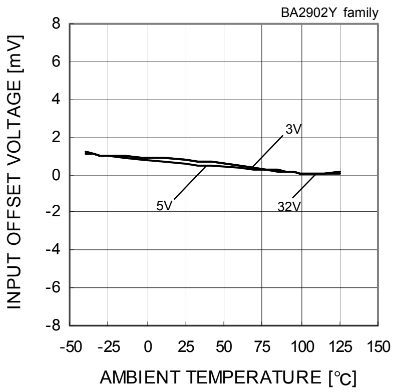


Fig. 37
Input Offset Voltage – Ambient Temperature
(Vicm=0[V], VOUT=1.4[V])

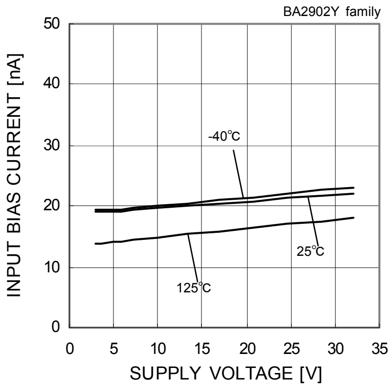


Fig. 38
Input Bias Current – Supply Voltage
(Vicm=0[V], VOUT=1.4[V])

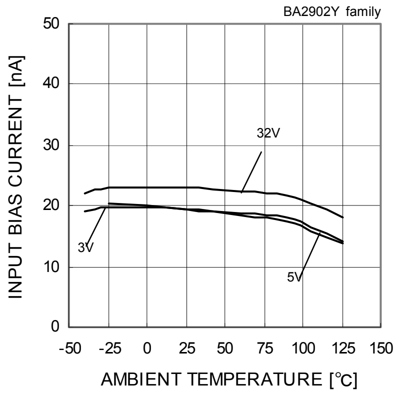


Fig. 39
Input Bias Current – Ambient Temperature
(Vicm=0[V],VOUT=1.4[V])

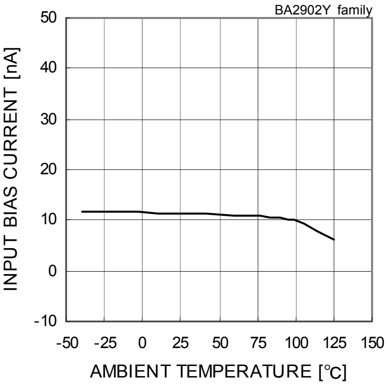


Fig. 40
Input Bias Current – Ambient Temperature
(VCC=30[V],Vicm=28[V],VOUT=1.4[V])

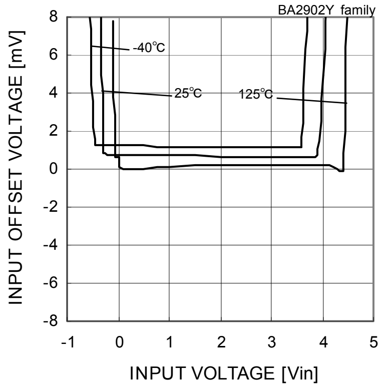


Fig. 41
Input Offset Voltage – Input Voltage
(VCC=5[V])

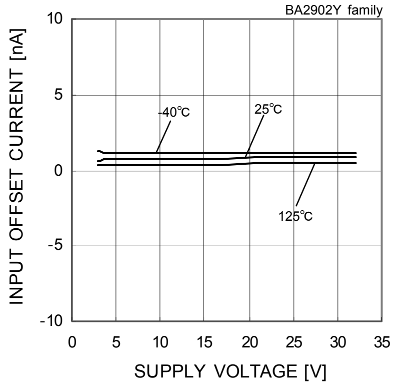


Fig. 42
Input Offset Current – Supply Voltage
(Vicm=0[V],VOUT=1.4[V])

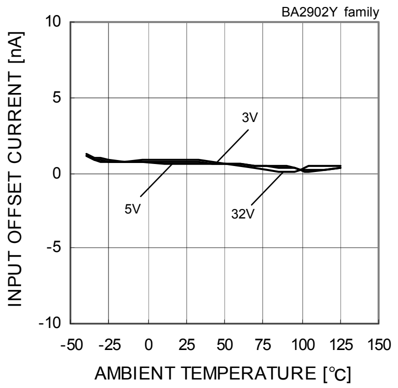


Fig. 43
Input Offset Current – Ambient Temperature
(Vicm=0[V],VOUT=1.4[V])

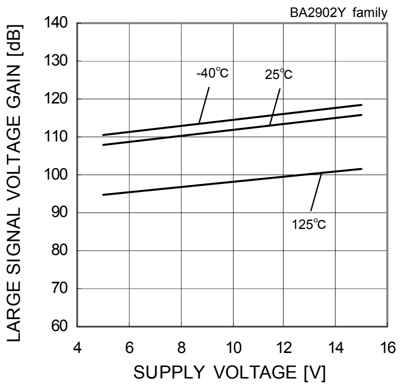


Fig. 44
Large Signal Voltage Gain – Supply Voltage
(RL=2[kΩ])

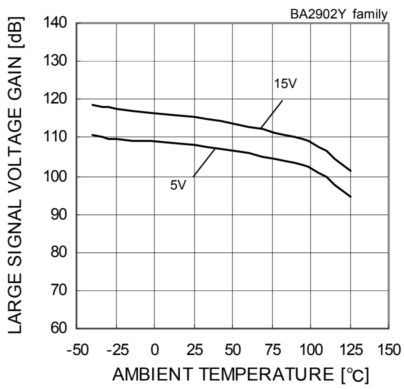


Fig. 45
Large Signal Voltage Gain – Ambient Temperature
(RL=2[kΩ])

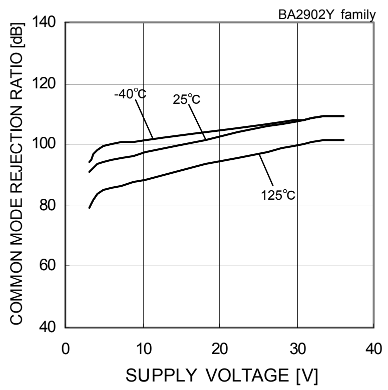


Fig. 46
Common Mode Rejection Ratio
– Supply Voltage

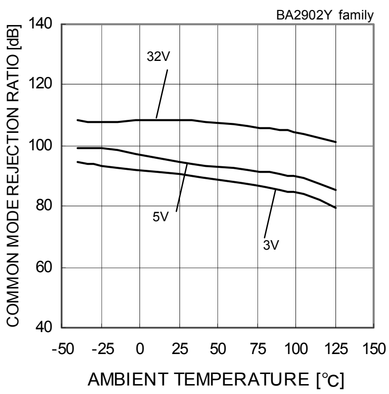


Fig. 47
Common Mode Rejection Ratio
– Ambient Temperature

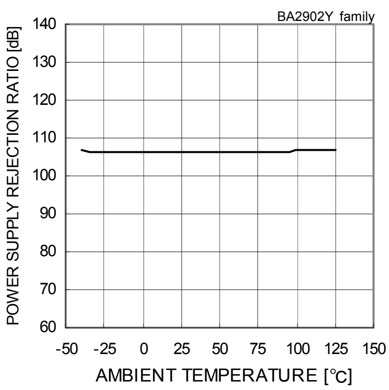
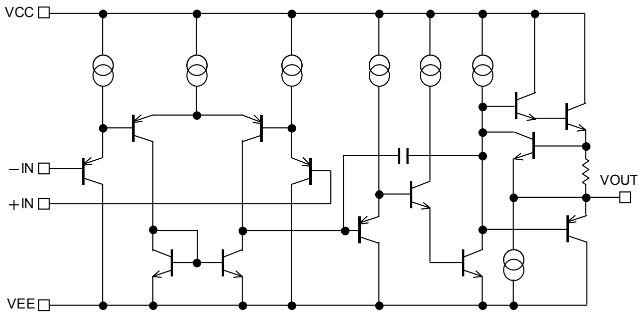


Fig. 48
Power Supply Rejection Ratio
– Ambient Temperature

(*)The data above is ability value of sample, it is not guaranteed.

●Circuit Diagram



BA2904Y / BA2902Y Schematic Diagram
Fig. 49 Schematic Diagram (one channel only)

●Test circuit1 NULL method

VCC,VEE,EK,Vicm Unit : [V]

Parameter	VF	S1	S2	S3	BA2904Y family BA2902Y family				calculation
					Vcc	VEE	EK	Vicm	
Input Offset Voltage	VF1	ON	ON	OFF	5～30	0	-1.4	0	1
Input Offset Current	VF2	OFF	OFF	OFF	5	0	-1.4	0	2
Input Bias Current	VF3	OFF	ON	OFF	5	0	-1.4	0	3
	VF4	ON	OFF						
Large Signal Voltage Gain	VF5	ON	ON	ON	15	0	-1.4	0	4
	VF6				15	0	-11.4	0	
Common-mode Rejection Ratio (Input common-mode Voltage Range)	VF7	ON	ON	OFF	5	0	-1.4	0	5
	VF8				5	0	-1.4	3.5	
Power Supply Rejection Ratio	VF9	ON	ON	OFF	5	0	-1.4	0	6
	VF10				30	0	-1.4	0	

- Calculation -

1. Input Offset Voltage (Vio)

$$\text{Vio} = \frac{|\,\text{VF1}\,|}{1 + \text{Rf} \,/\, \text{Rs}} \quad [\text{V}]$$

2. Input Offset Current (Iio)

$$\text{Iio} = \frac{|\,\text{VF2} - \text{VF1}\,|}{\text{Ri} \times (1 + \text{Rf} \,/\, \text{Rs})} \quad [\text{A}]$$

3. Input Bias Current (Ib)

$$\text{Ib} = \frac{|\,\text{VF4} - \text{VF3}\,|}{2 \times \text{Ri} \times (1 + \text{Rf} \,/\, \text{Rs})} \quad [\text{A}]$$

4. Large Signal Voltage Gain (Av)

$$\text{Av} = 20 \times \text{Log} \frac{\Delta \text{EK} \times (1 + \text{Rf}/\text{Rs})}{|\text{VF5-VF6}|} \quad [\text{dB}]$$

5. Common-mode Rejection Ration (CMRR)

$$\text{CMRR} = 20 \times \text{Log} \frac{\Delta \text{Vicm} \times (1 + \text{Rf}/\text{Rs})}{|\text{VF8-VF7}|} \quad [\text{dB}]$$

6. Power supply rejection ratio (PSRR)

$$\text{PSRR} = 20 \times \text{Log} \frac{\Delta \text{Vcc} \times (1 + \text{Rf}/\text{Rs})}{|\text{VF10-VF9}|} \quad [\text{dB}]$$

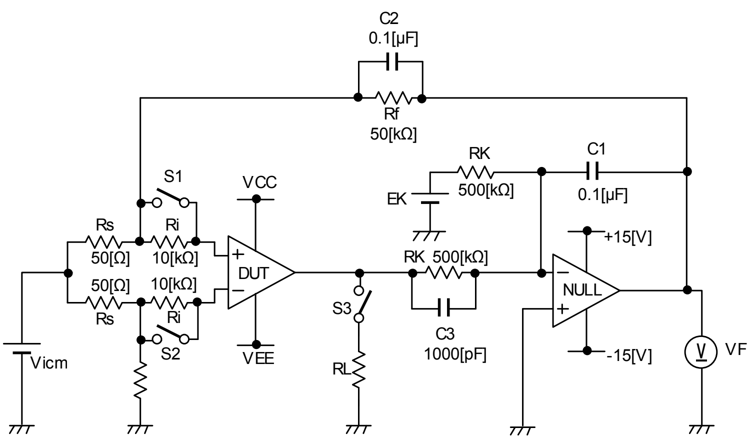


Fig. 50 Test circuit1 (one channel only)

●Test Circuit 2 Switch Condition

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12	SW 13	SW 14
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
High Level Output Voltage	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
Low Level Output Voltage	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
Output Source Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Output Sink Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
Gain Bandwidth Product	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Equivalent Input Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF

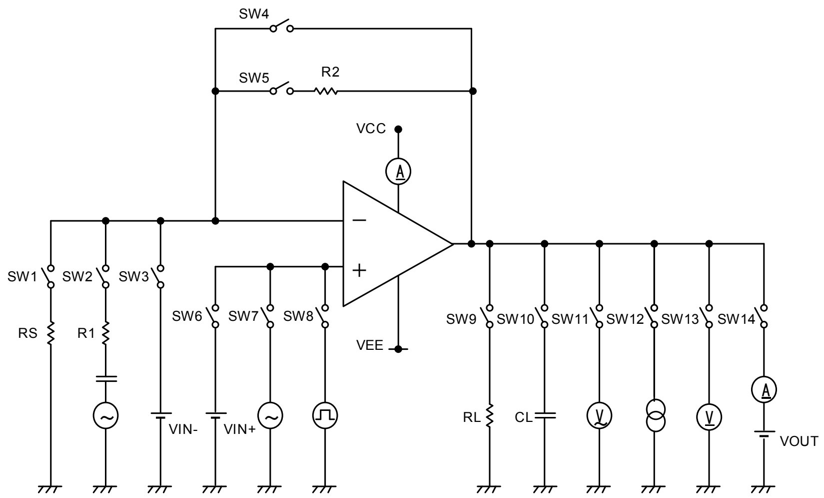


Fig. 51 Test Circuit 2 (each Op-Amp)

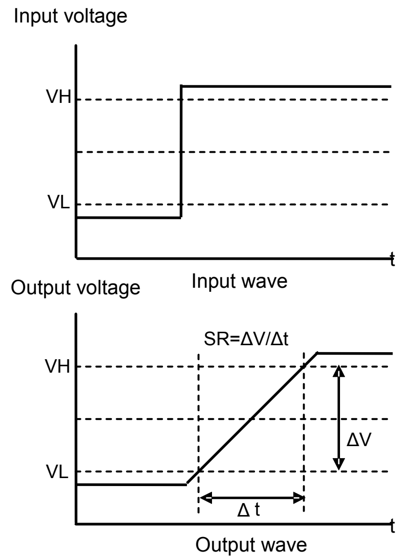
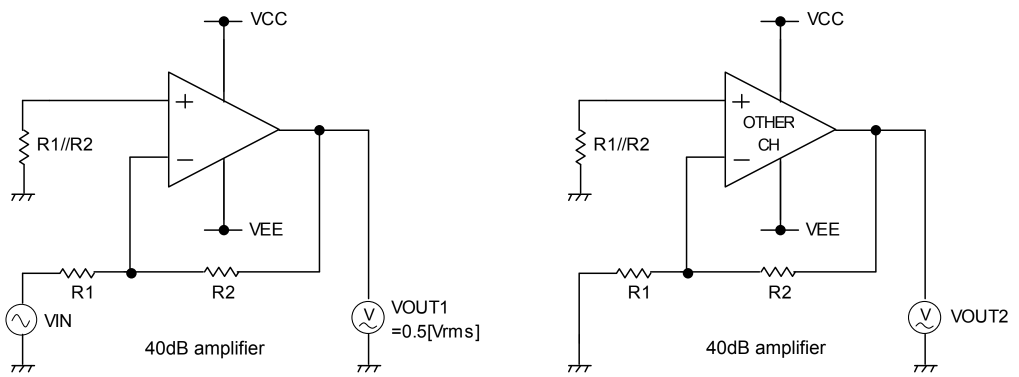


Fig. 52 Slew Rate Input Waveform

●Measurement Circuit 3 Amplifier To Amplifier Coupling



$$CS = 20 \times \log \frac{100 \times VOUT1}{VOUT2}$$

Fig. 53 Test Circuit 3

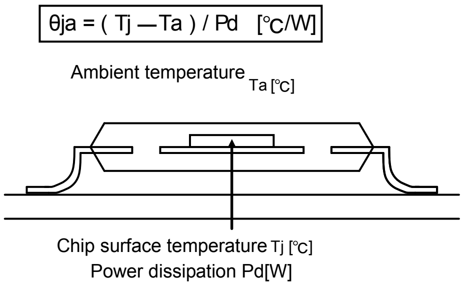
●Derating curves

Power dissipation(total loss) indicates the power that can be consumed by IC at Ta=25℃(normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip(maximum junction temperature) and thermal resistance of package(heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicatesthis heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol θja[℃/W].The temperature of IC inside the package can be estimated by this thermal resistance. Fig.54(a) shows the model of thermal resistance of the package. Thermal resistance θja, ambient temperature Ta, junction temperature Tj, and power dissipation Pd can be calculated by the equation below:

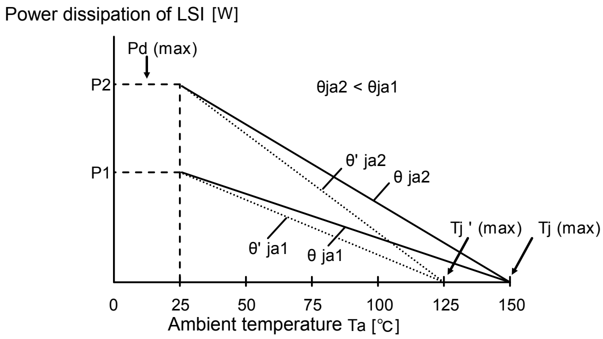
$$\theta ja = (Tj - Ta) / Pd \quad [℃/W] \quad \cdots\cdots \quad (\text{I})$$

Derating curve in Fig.54(b) indicates power that can be consumed by IC with reference to ambient temperature.Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient iis determined by thermal resistance θja. Thermal resistance θja depends on chip size, power consumption, package,ambient temperature, package condition, wind velocity, etc even when the same of package is used.

Thermal reduction curve indicates a reference value measured at a specified condition. Fig.55(c),(d) show a derating curve for an example of BA2904Y, BA2902Y.

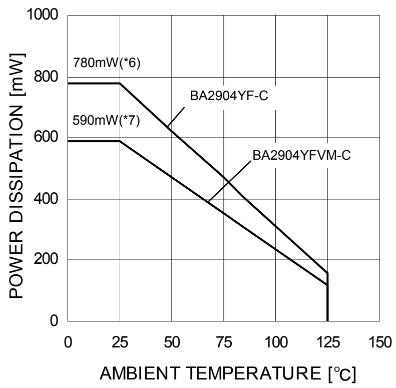


(a) Thermal resistance

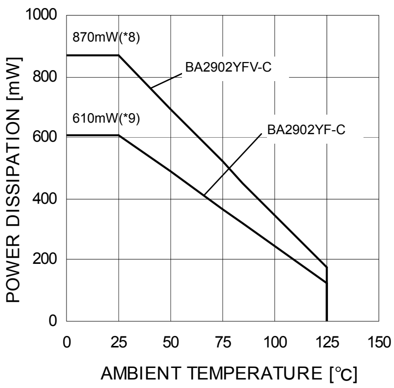


(b) Derating curve

Fig. 54 Thermal resistance and derating



(c) BA2904Y family



(d) BA2902Y family

(*6)	(*7)	(*8)	(*9)	Unit
6.2	4.8	7.0	4.9	[mW/℃]

When using the unit above Ta=25[℃], subtract the value above per degree [℃].
Permissible dissipation is the value when FR4 glass epoxy board 70[mm]×70[mm]×1.6[mm](cooper foil area below 3[%]) is mounted.

Fig. 55 Derating curve

●Description of Electrical Characteristics

Described below are descriptions of the relevant electrical terms
Please note that item names, symbols and their meanings may differ from those on another manufacturer's documents.

1.Absolute maximum ratings

The absolute maximum ratings are values that should never be exceeded, since doing so may result in deterioration of electrical characteristics or damage to the part itself as well as peripheral components.

1.1 Power supply voltage (VCC-VEE)
Expresses the maximum voltage that can be supplied between the positive and negative supply terminals without causing deterioration of the electrical characteristics or destruction of the internal circuitry.

1.2 Differential input voltage (Vid)
Indicates the maximum voltage that can be supplied between the non-inverting and inverting terminals without damaging the IC.

1.3 Input common-mode voltage range (Vicm)
Signifies the maximum voltage that can be supplied to non-inverting and inverting terminals without causing deterioration of the characteristics or damage to the IC itself. Normal operation is not guaranteed within the common-mode voltage range of the maximum ratings – use within the input common-mode voltage range of the electric characteristics instead.

1.4 Operating and storage temperature ranges (Topr,Tstg)
The operating temperature range indicates the temperature range within which the IC can operate. The higher the ambient temperature, the lower the power consumption of the IC. The storage temperature range denotes the range of temperatures the IC can be stored under without causing excessive deterioration of the electrical characteristics.

1.5 Power dissipation (Pd)
Indicates the power that can be consumed by a particular mounted board at ambient temperature (25℃). For packaged products, Pd is determined by the maximum junction temperature and the thermal resistance.

2.Electrical characteristics

2.1 Input offset voltage (Vio)
Signifies the voltage difference between the non-inverting and inverting terminals. It can be thought of as the input voltage difference required for setting the output voltage to 0 V.

2.2 Input offset voltage drift (△Vio/△T)
Denotes the ratio of the input offset voltage fluctuation to the ambient temperature fluctuation.

2.3 Input offset current (Iio)
Indicates the difference of input bias current between the non-inverting and inverting terminals.

2.4 Input offset current drift (△Iio/△T)
Signifies the ratio of the input offset current fluctuation to the ambient temperature fluctuation.

2.5 Input bias current (Ib)
Denotes the current that flows into or out of the input terminal, it is defined by the average of the input bias current at the non-inverting terminal and the input bias current at the inverting terminal.

2.6 Circuit current (ICC)
Indicates the current of the IC itself that flows under specified conditions and during no-load steady state.

2.7 High level output voltage/low level output voltage (VOH/VOL)
Signifying the voltage range that can be output under specified load conditions, it is in general divided into high level output voltage and low level output voltage. High level output voltage indicates the upper limit of the output voltage, while low level output voltage the lower limit.

2.8 Large signal voltage gain (AV)
The amplifying rate (gain) of the output voltage against the voltage difference between non-inverting and inverting terminals, it is (normally) the amplifying rate (gain) with respect to DC voltage.
AV = (output voltage fluctuation) / (input offset fluctuation)

2.9 Input common-mode voltage range (Vicm)
Indicates the input voltage range under which the IC operates normally.

2.10 Common-mode rejection ratio (CMRR)
Signifies the ratio of fluctuation of the input offset voltage when the in-phase input voltage is changed (DC fluctuation).
CMRR = (change in input common-mode voltage) / (input offset fluctuation)

2.11 Power supply rejection ratio (PSRR)
Denotes the ratio of fluctuation of the input offset voltage when supply voltage is changed (DC fluctuation).
SVR = (change in power supply voltage) / (input offset fluctuation)

2.12 Output source current/ output sink current (IOH/IOL)
The maximum current that can be output under specific output conditions, it is divided into output source current and output sink current. The output source current indicates the current flowing out of the IC, and the output sink current the current flowing into the IC.

2.13 Channel separation (CS)
Expresses the amount of fluctuation of the input offset voltage or output voltage with respect to the change in the output voltage of a driven channel.

2.14 Slew rate (SR)
Indicates the time fluctuation ratio of the output voltage when an input step signal is supplied.

2.15 Gain bandwidth product (GBW)
The product of the specified signal frequency and the gain of the op-amp at such frequency, it gives the approximate value of the frequency where the gain of the op-amp is 1 (maximum frequency, and unity gain frequency)

●Notes for use

1) Unused circuits
When there are unused circuits, it is recommended that they be connected as in Fig.56, setting the non-inverting input terminal to a potential within the in-phase input voltage range (Vicm).

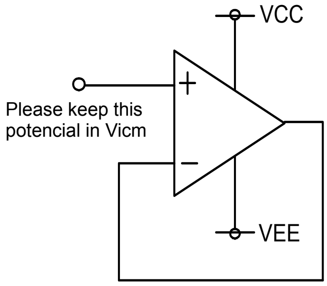


Fig. 56 Example of processing unused circuit

2) Input voltage
Applying VEE+36[V] to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, irrespective of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

3) Power supply (single / dual)
The op-amp operates when the voltage supplied is between VCC and VEE Therefore, the single supply op-mp can be used as a dual supply op-amp as well.

4) Power dissipation (Pd)
Using the unit in excess of the rated power dissipation may cause deterioration in electrical characteristics due to the rise in chip temperature, including reduced current capability. Therefore, please take into consideration the power dissipation (Pd) under actual operating conditions and apply a sufficient margin in thermal design. Refer to the thermal derating curves for more information.

5) Short-circuit between pins and erroneous mounting
Incorrect mounting may damage the IC. In addition, the presence of foreign substances between the outputs, the output and the power supply, or the output and GND may result in IC destruction.

6) Operation in a strong electromagnetic field
Operation in a strong electromagnetic field may cause malfunctions.

7) Radiation
This IC is not designed to withstand radiation.

8) IC handing
Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuation of the electrical characteristics due to piezoelectric (piezo) effects.

9) IC operation
The output stage of the IC is configured using Class C push-pull circuits. Therefore, when the load resistor is connected to the middle potential of VCC and VEE, crossover distortion occurs at the changeover between discharging and charging of the output current. Connecting a resistor between the output terminal and GND, and increasing the bias current for Class A operation will suppress crossover distortion.

10) Board inspection
Connecting a capacitor to a pin with low impedance may stress the IC. Therefore, discharging the capacitor after every process is recommended. In addition, when attaching and detaching the jig during the inspection phase, ensure that the power is turned OFF before inspection and removal. Furthermore, please take measures against ESD in the assembly process as well as during transportation and storage.

11) Output capacitor
Discharge of the external output capacitor to VCC is possible via internal parasitic elements when VCC is shorted to VEE, causing damage to the internal circuitry due to thermal stress. Therefore, when using this IC in circuits where oscillation due to output capacitive load does not occur, such as in voltage comparators, use an output capacitor with a capacitance less than 0.1μF.

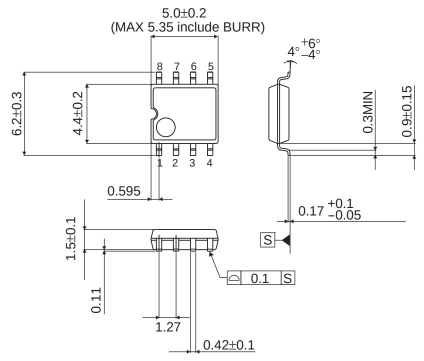
12) Oscillation by output capacitor
Please pay attention to oscillation by output capacitor, designing application of negative feed back loop circuit with these ICs.

● Ordering part number

B	A	2	9	0	2	Y	F	V	-	C	E	2

Part No.	Part No.	Package	Automotive series	Packaging and forming specification
	2904Y 2902Y	F : SOP8 SOP14 FV : SSOP-B14 FVM : MSOP8		E2: Embossed tape and reel (SOP8/SOP14/ SSOP-B14) TR: Embossed tape and reel (MSOP8)

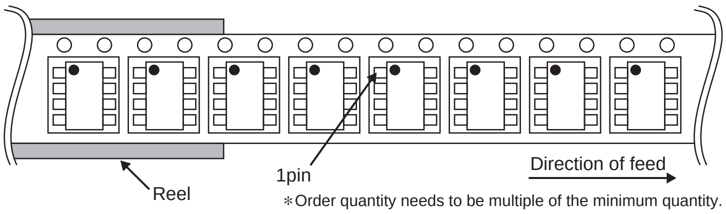
SOP8



(Unit : mm)

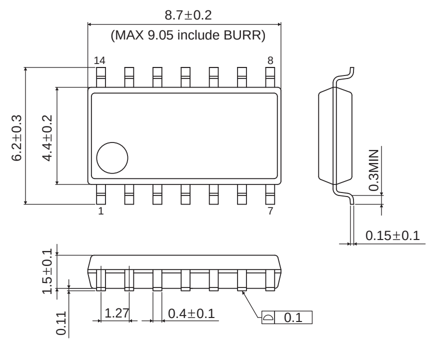
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

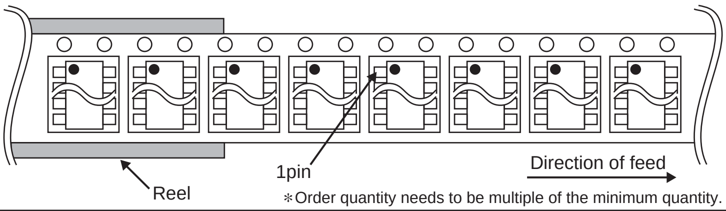
SOP14



(Unit : mm)

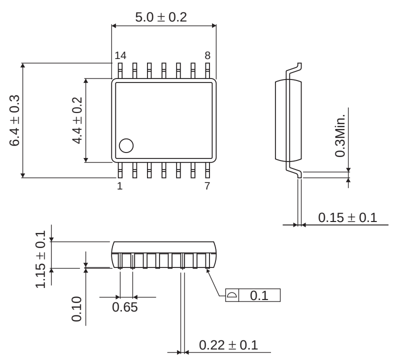
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

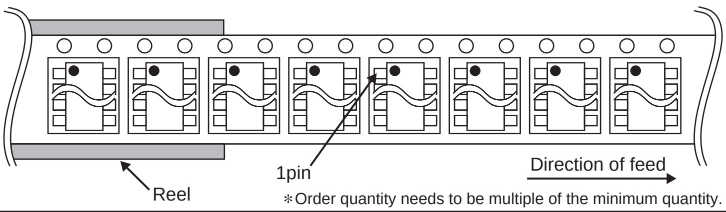
SSOP-B14



(Unit : mm)

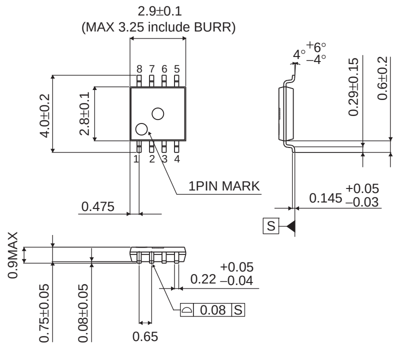
<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

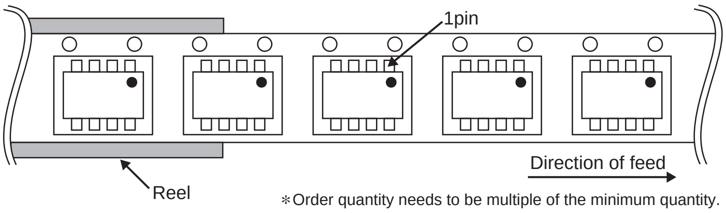
MSOP8



(Unit : mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

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