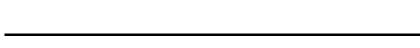
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April 1st, 2010 Renesas Electronics Corporation

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DATA SHEET



MOS FIELD EFFECT TRANSISTOR NP36P04SDG

SWITCHING P-CHANNEL POWER MOSFET

DESCRIPTION

The NP36P04SDG is P-channel MOS Field Effect Transistor designed for high current switching applications.

ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
NP36P04SDG-E1-AY Note	D O. (Tin)	T 0500 -/	TO 050 (MD 0714)
NP36P04SDG-E2-AY Note	Pure Sn (Tin)	Tape 2500 p/reel	TO-252 (MP-3ZK)

Note Pb-free (This product does not contain Pb in external electrode.)

FEATURES

• Super low on-state resistance

 $R_{DS(on)1} = 17.0 \text{ m}\Omega \text{ MAX}. \text{ (Vgs} = -10 \text{ V, I}_D = -18 \text{ A})$

 $R_{DS(on)2} = 23.5 \text{ m}\Omega \text{ MAX.} \text{ (Vgs} = -4.5 \text{ V, Ip} = -18 \text{ A)}$

Low input capacitance

Ciss = 2800 pF TYP.

ABSOLUTE MAXIMUM RATINGS (TA = 25°C)

	(/		
Drain to Source Voltage (V _{GS} = 0 V)	VDSS	-40	V
Gate to Source Voltage (VDS = 0 V)	Vgss	∓20	V
Drain Current (DC) (Tc = 25°C)	I _{D(DC)}	∓36	Α
Drain Current (pulse) Note1	D(pulse)	∓108	Α
Total Power Dissipation (Tc = 25°C)	P _{T1}	56	W
Total Power Dissipation (T _A = 25°C)	P _{T2}	1.2	W
Channel Temperature	Tch	175	°C
Storage Temperature	Tstg	-55 to +175	°C
Single Avalanche Current Note2	las	26	Α
Single Avalanche Energy Note2	Eas	67	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Starting T_{ch} = 25°C, V_{DD} = -20 V, R_G = 25 Ω , V_{GS} = -20 \rightarrow 0 V

THERMAL RESISTANCE

<R>

Channel to Case Thermal Resistance	Rth(ch-C)	2.68	°C/W
Channel to Ambient Thermal Resistance	Rth(ch-A)	125	°C/W

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(TO-252)

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ELECTRICAL CHARACTERISTICS (TA = 25°C)

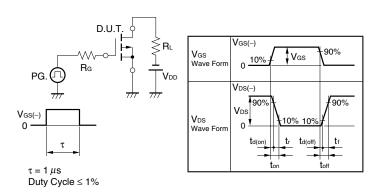
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	IDSS	V _{DS} = -40 V, V _{GS} = 0 V			-10	μΑ
Gate Leakage Current	Igss	V _{GS} = ∓20 V, V _{DS} = 0 V			∓100	nA
Gate to Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_{D} = -250 \mu\text{A}$	-1.0	-1.6	-2.5	V
Forward Transfer Admittance Note	y _{fs}	V _{DS} = -10 V, I _D = -18 A	12	23		S
Drain to Source On-state Resistance Note	R _{DS(on)1}	V _{GS} = -10 V, I _D = -18 A		12.5	17.0	mΩ
	R _{DS(on)2}	V _{GS} = -4.5 V, I _D = -18 A		15.4	23.5	mΩ
Input Capacitance	Ciss	V _{DS} = -10 V,		2800		pF
Output Capacitance	Coss	V _{GS} = 0 V,		450		pF
Reverse Transfer Capacitance	Crss	f = 1 MHz		280		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = -20 V, I _D = -18 A,		8		ns
Rise Time	tr	V _{GS} = -10 V,		10		ns
Turn-off Delay Time	t _{d(off)}	R _G = 0 Ω		250		ns
Fall Time	tr			140		ns
Total Gate Charge	Q _G	V _{DD} = -32 V,		55		nC
Gate to Source Charge	Q _{GS}	V _{GS} = -10 V,		7		nC
Gate to Drain Charge	Q _{GD}	I _D = -36 A		15		nC
Body Diode Forward Voltage Note	V _{F(S-D)}	I _F = -36 A, V _{GS} = 0 V		0.95	1.5	V
Reverse Recovery Time	trr	I _F = -36 A, V _{GS} = 0 V,		44		ns
Reverse Recovery Charge	Qrr	di/dt = -100 A/μs		51		nC

Note Pulsed test PW \leq 350 μ s, Duty Cycle \leq 2%

TEST CIRCUIT 1 AVALANCHE CAPABILITY

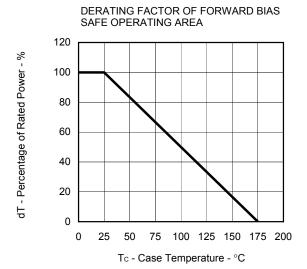
$V_{GS} = -20 \rightarrow 0 \text{ V}$ V_{DD} V_{DD}

TEST CIRCUIT 2 SWITCHING TIME

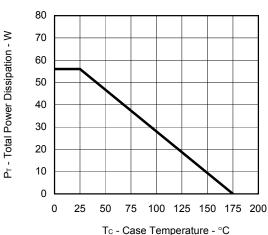


TEST CIRCUIT 3 GATE CHARGE

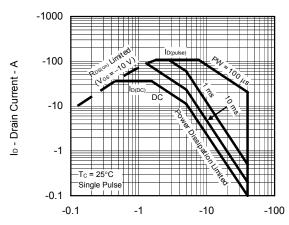
TYPICAL CHARACTERISTICS (TA = 25°C)



TOTAL POWER DISSIPATION vs. CASE TEMPERATURE

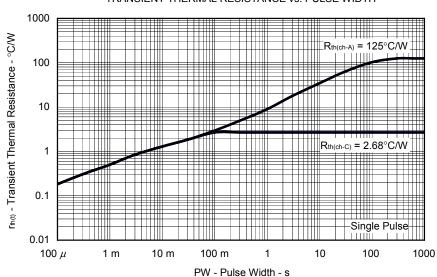


FORWARD BIAS SAFE OPERATING AREA

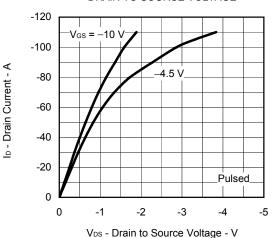


V_{DS} - Drain to Source Voltage - V

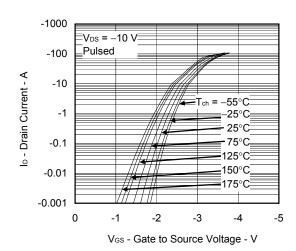
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



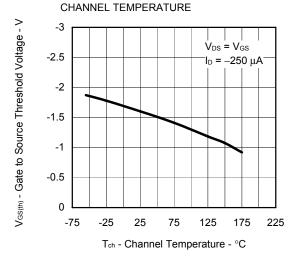
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



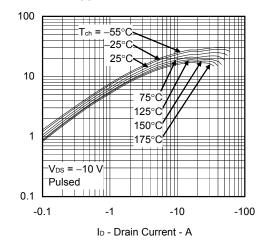
FORWARD TRANSFER CHARACTERISTICS



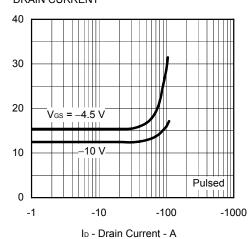
GATE TO SOURCE THRESHOLD VOLTAGE vs.



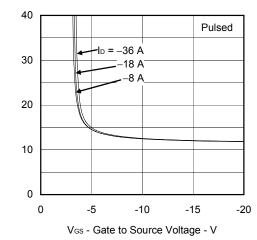
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



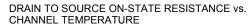
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE

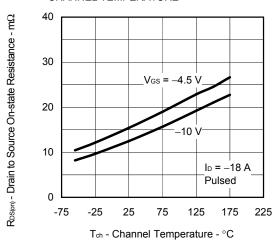


R_{DS(on)} - Drain to Source On-state Resistance - mΩ

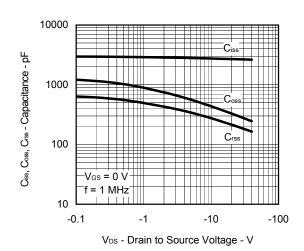
ys | - Forward Transfer Admittance - S

RDS(on) - Drain to Source On-state Resistance - mΩ

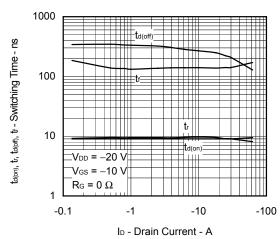




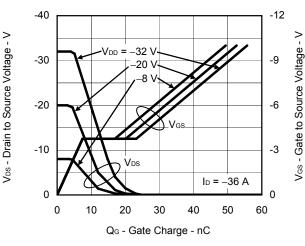
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



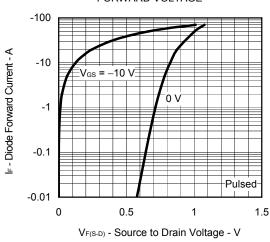
SWITCHING CHARACTERISTICS



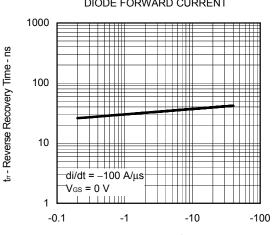
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

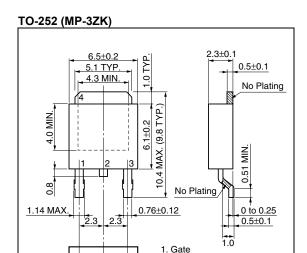


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



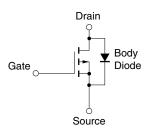
IF - Diode Forward Current - A

PACKAGE DRAWING (Unit: mm)



Drain
 Source
 Fin (Drain)

EQUIVALENT CIRCUIT



Remark Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

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