

## N-channel 650 V, 0.6 $\Omega$ typ., 7 A MDmesh II Plus™ low $Q_g$ Power MOSFETs in TO-220FP and I<sup>2</sup>PAKFP packages

Datasheet - preliminary data

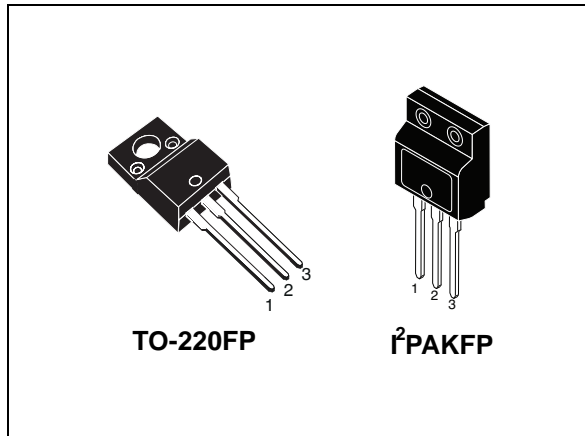
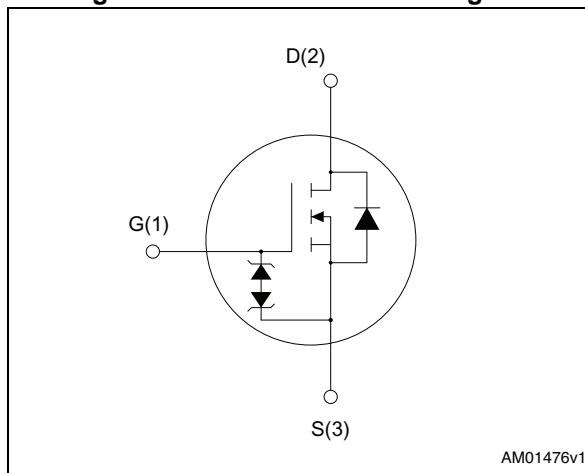


Figure 1. Internal schematic diagram



### Features

Order codes	$V_{DS}$	$R_{DS(on) \max}$	$I_D$
STF11N65M2	650 V	0.67 $\Omega$	7 A
STFI11N65M2			

- Extremely low gate charge
- Lower  $R_{DS(on)}$  x area vs previous generation
- Low gate input resistance
- 100% avalanche tested
- Zener-protected

### Applications

- Switching applications

### Description

These devices are N-channel Power MOSFETs developed using a new generation of MDmesh™ technology: MDmesh II Plus™ low  $Q_g$ . These revolutionary Power MOSFETs associate a vertical structure to the company's strip layout to yield one of the world's lowest on-resistance and gate charge. They are therefore suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order codes	Marking	Package	Packaging
STF11N65M2	11N65M2	TO-220FP	Tube
STFI11N65M2		I <sup>2</sup> PAKFP	

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Revision history</b> .....	<b>13</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ °C}$	7	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ °C}$	4.4	A
$I_{DM}^{(2)}$	Drain current (pulsed)	28	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ °C}$	25	W
$dv/dt^{(3)}$	Peak diode recovery voltage slope (starting $T_j = 25\text{ °C}$ , $I_D = I_{AS}$ , $V_{DD} = 50\text{ V}$ )	15	V/ns
$dv/dt^{(4)}$	MOSFET $dv/dt$ ruggedness	50	V/ns
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat sink ( $t = 1\text{ s}$ ; $T_C = 25\text{ °C}$ )	2500	V
$T_{stg}$	Storage temperature	- 55 to 150	°C
$T_j$	Max. operating junction temperature	150	

1. The value is rated according to Rthj-case and limited by package.
2. Pulse width limited by  $T_{jmax}$
3.  $I_{SD} \leq 7\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ;  $V_{DS\text{ peak}} < V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .
4.  $V_{DS} \leq 520\text{ V}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj\text{-case}}$	Thermal resistance junction-case max	5	°C/W
$R_{thj\text{-amb}}$	Thermal resistance junction-amb max	62.5	°C/W

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not repetitive (pulse width limited by $T_{jmax}$ )	1.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ °C}$ , $I_D = I_{AR}$ ; $V_{DD} = 50$ )	110	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	650			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 650\text{ V}$			1	$\mu\text{A}$
		$V_{DS} = 650\text{ V}, T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 3.5\text{ A}$		0.6	0.67	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 100\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	410	-	pF
$C_{oss}$	Output capacitance		-	20	-	pF
$C_{rss}$	Reverse transfer capacitance		-	0.95	-	pF
$C_{oss\text{ eq.}}^{(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }520\text{ V}, V_{GS} = 0$	-	83	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	6.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 520\text{ V}, I_D = 7\text{ A}, V_{GS} = 10\text{ V}$ (see <a href="#">Figure 15</a> )	-	12.5	-	nC
$Q_{gs}$	Gate-source charge		-	3.2	-	nC
$Q_{gd}$	Gate-drain charge		-	5.8	-	nC

1.  $C_{oss\text{ eq.}}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 325 \text{ V}$ , $I_D = 3.5 \text{ A}$ , $R_G = 4.7 \Omega$ , $V_{GS} = 10 \text{ V}$ (see <a href="#">Figure 14</a> and <a href="#">19</a> )	-	9.5	-	ns
$t_r$	Rise time		-	7.5	-	ns
$t_{d(off)}$	Turn-off delay time		-	26	-	ns
$t_f$	Fall time		-	15	-	ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		7	A
$I_{SDM}^{(1)(2)}$	Source-drain current (pulsed)		-		28	A
$V_{SD}^{(3)}$	Forward on voltage	$I_{SD} = 7 \text{ A}$ , $V_{GS} = 0$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 7 \text{ A}^{(2)}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see <a href="#">Figure 16</a> )	-	318		ns
$Q_{rr}$	Reverse recovery charge		-	2.5		nC
$I_{RRM}$	Reverse recovery current		-	15.5		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 7 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see <a href="#">Figure 16</a> )	-	437		ns
$Q_{rr}$	Reverse recovery charge		-	3.2		nC
$I_{RRM}$	Reverse recovery current		-	15		A

1. Pulse width limited by safe operating area
2. Test condition is referred to through-hole package
3. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

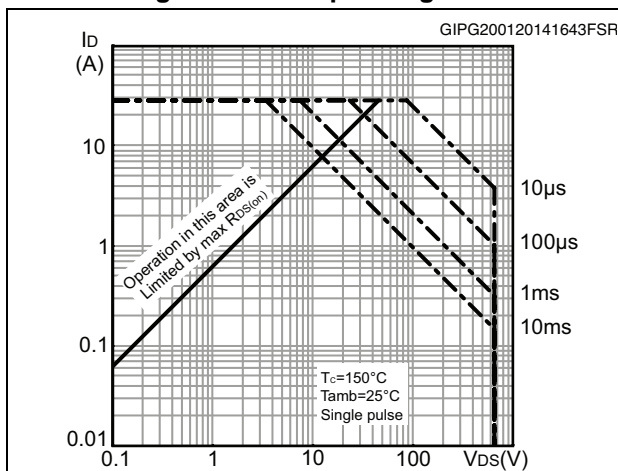


Figure 3. Thermal impedance

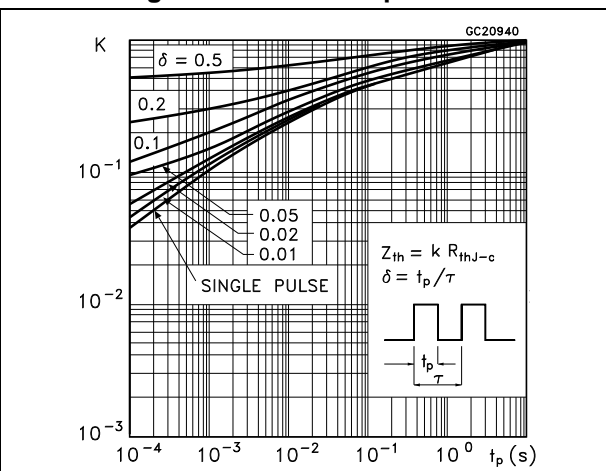


Figure 4. Output characteristics

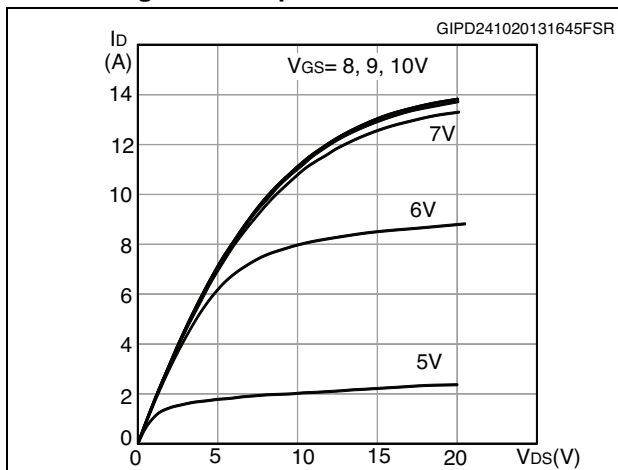


Figure 5. Transfer characteristics

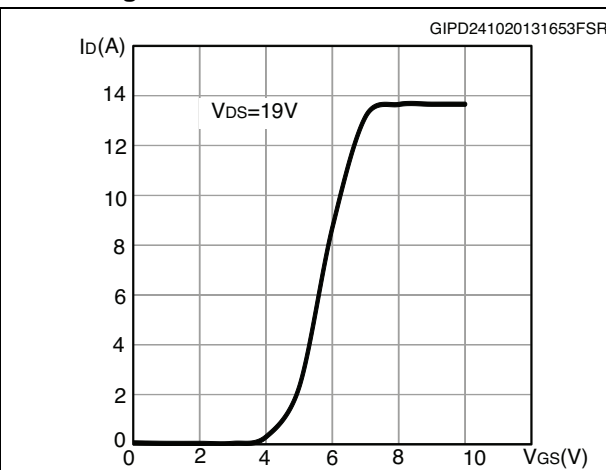


Figure 6. Normalized  $V_{(BR)DSS}$  vs temperature

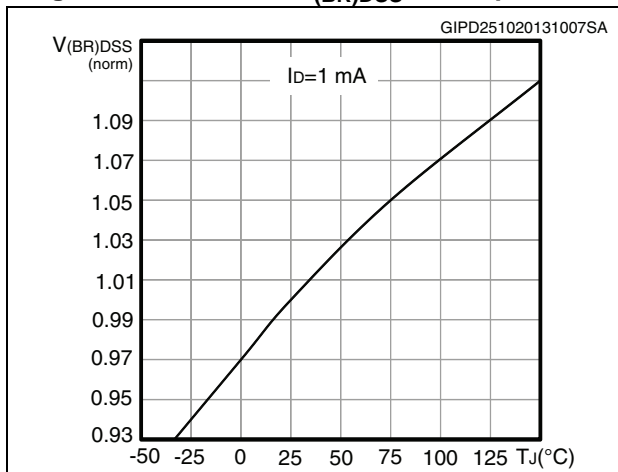


Figure 7. Static drain-source on-resistance

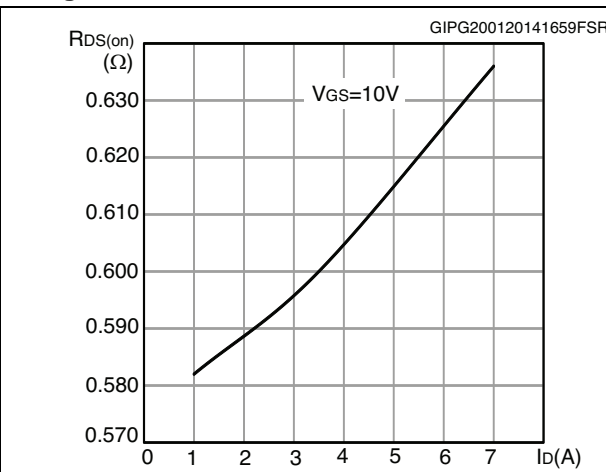


Figure 8. Gate charge vs gate-source voltage

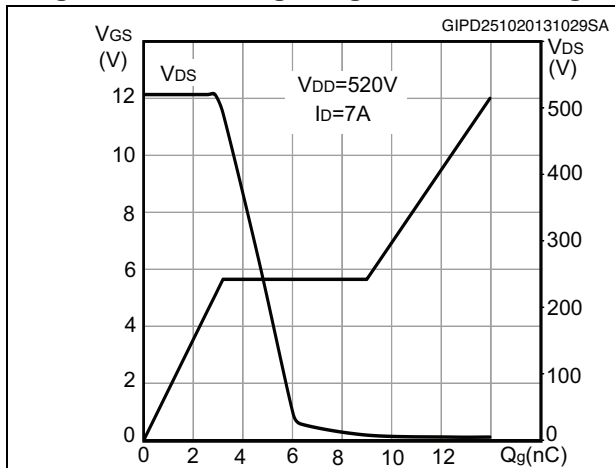


Figure 9. Capacitance variations

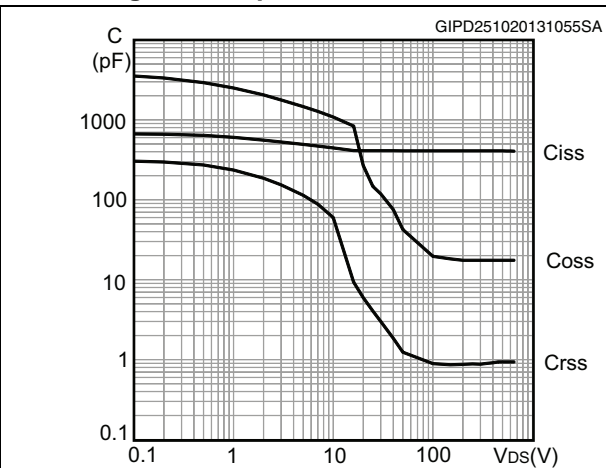


Figure 10. Normalized gate threshold voltage vs temperature

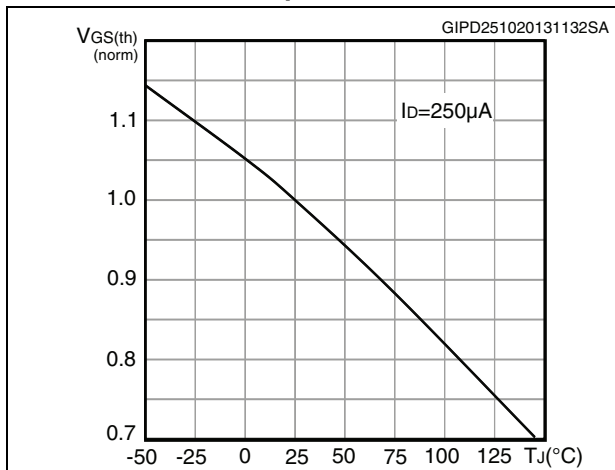


Figure 11. Normalized on-resistance vs temperature

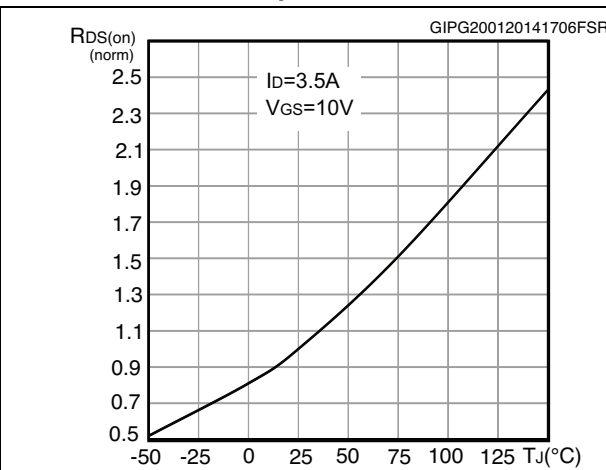


Figure 12. Source-drain diode forward characteristics

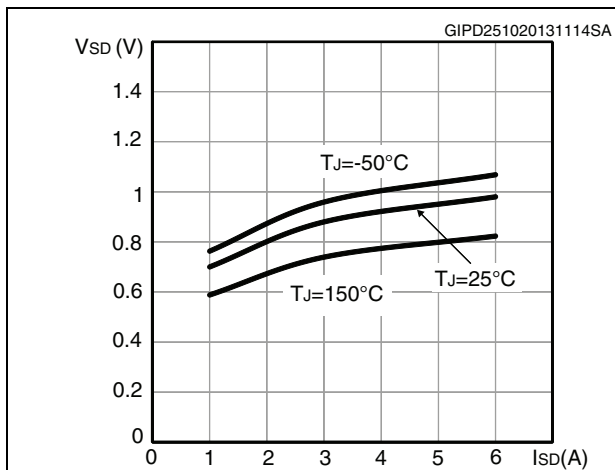
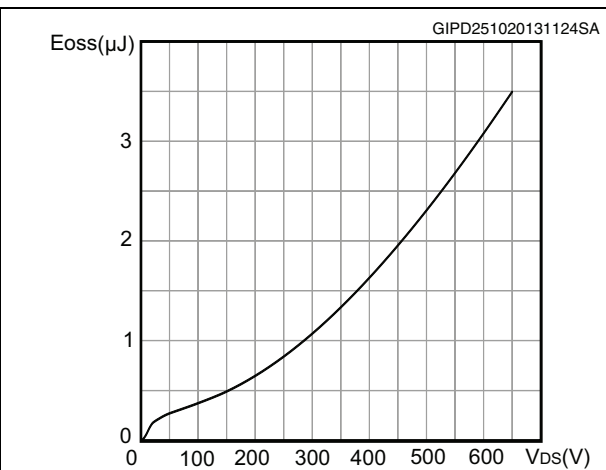


Figure 13. Output capacitance stored energy



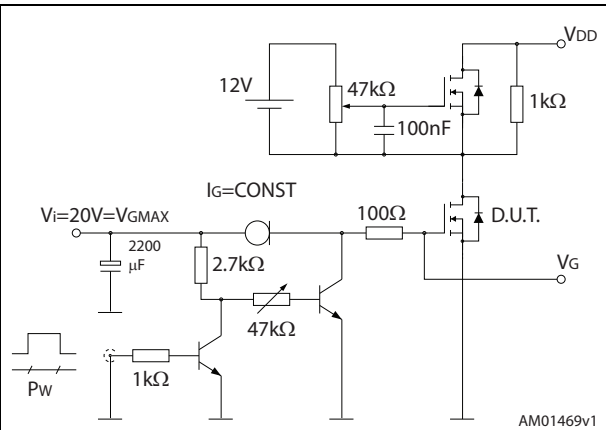
### 3 Test circuits

Figure 14. Switching times test circuit for resistive load



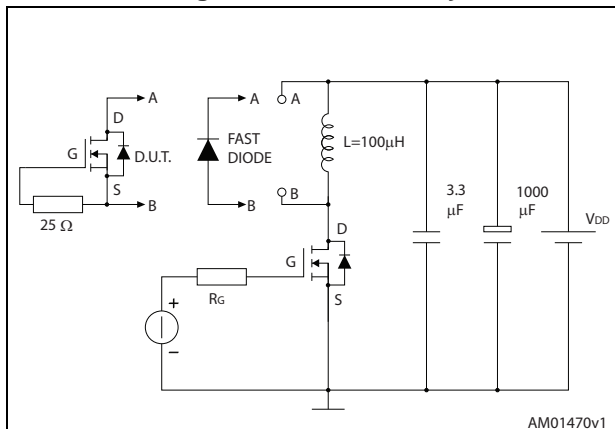
AM01468v1

Figure 15. Gate charge test circuit



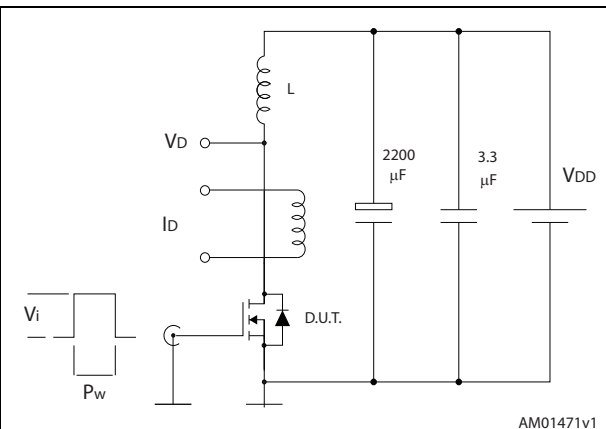
AM01469v1

Figure 16. Test circuit for inductive load switching and diode recovery times



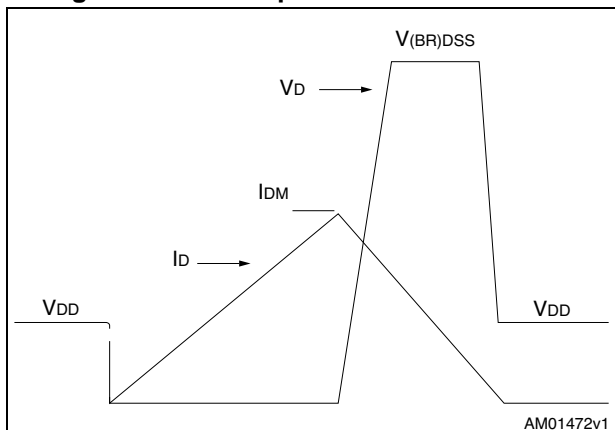
AM01470v1

Figure 17. Unclamped inductive load test circuit



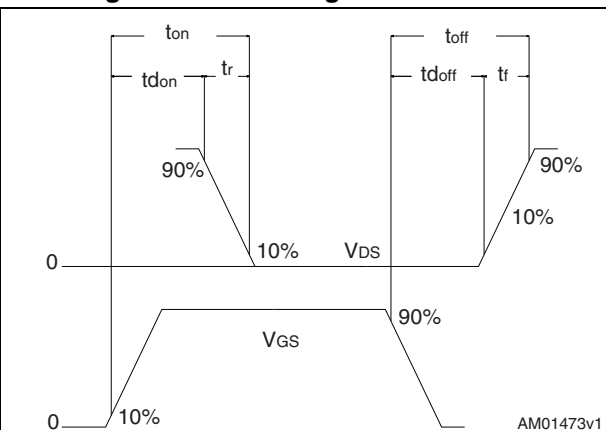
AM01471v1

Figure 18. Unclamped inductive waveform



AM01472v1

Figure 19. Switching time waveform



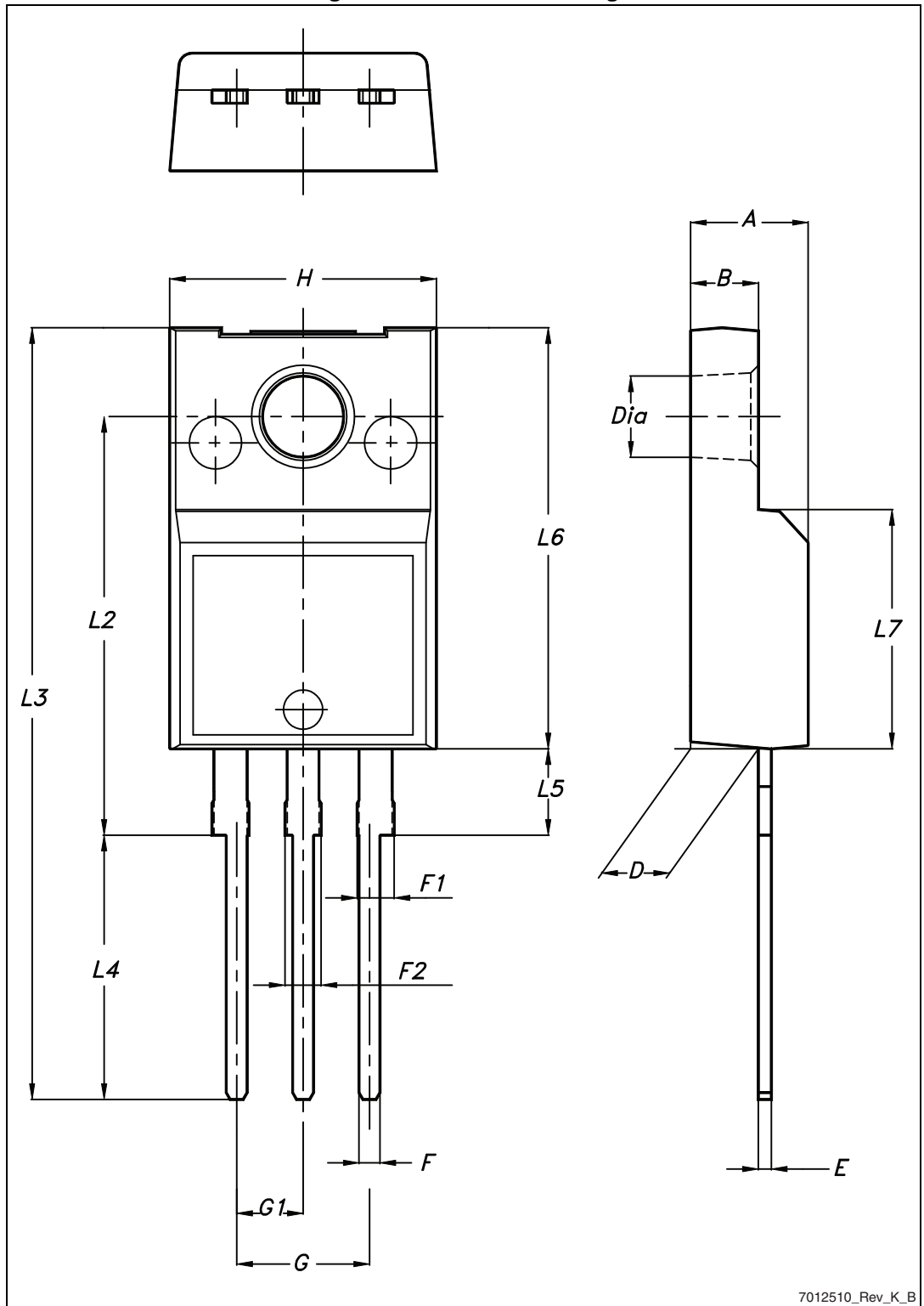
AM01473v1



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

Figure 20. TO-220FP drawing



7012510\_Rev\_K\_B

Table 9. TO-220FP mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
∅	3		3.2

Figure 21. I<sup>2</sup>PAKFP (TO-281) drawing

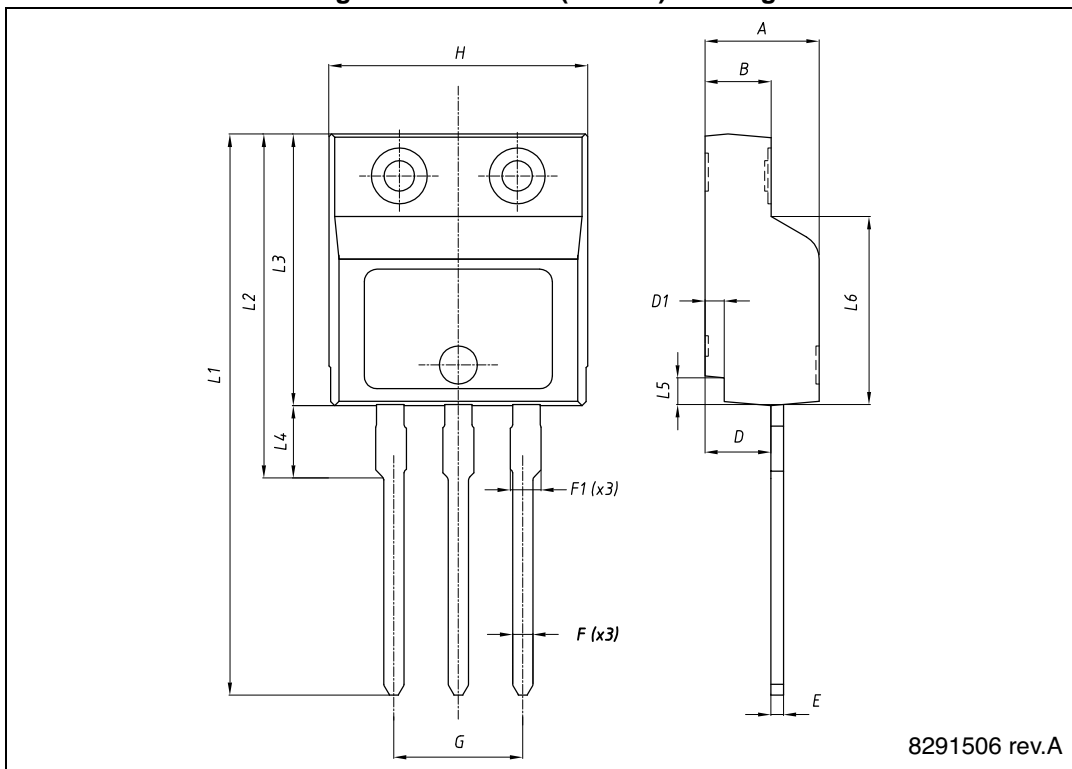


Table 10. I<sup>2</sup>PAKFP (TO-281) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
B	2.50		2.70
D	2.50		2.75
D1	0.65		0.85
E	0.45		0.70
F	0.75		1.00
F1			1.20
G	4.95	-	5.20
H	10.00		10.40
L1	21.00		23.00
L2	13.20		14.10
L3	10.55		10.85
L4	2.70		3.20
L5	0.85		1.25
L6	7.30		7.50

## 5 Revision history

Table 11. Document revision history

Date	Revision	Changes
09-May-2014	1	First release.

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)