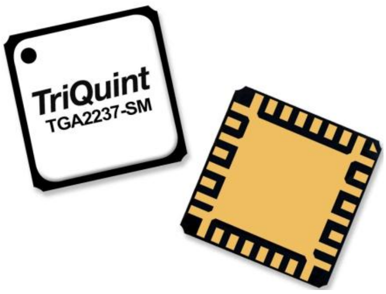
TGA2237-SM

0.03 – 2.5GHz 10W GaN Power Amplifier

Applications

- Commercial and military radar
- Communications
- Electronic Warfare

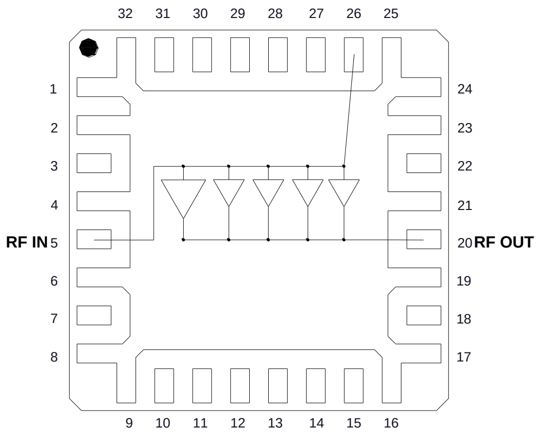


QFN 5x5 mm 32L

Product Features

- Frequency Range: 0.03 – 2.5GHz
- P_{SAT}: >40dBm at PIN = 27dBm
- P1dB: >33dBm
- PAE: >50%
- Large Signal Gain: >13dB
- Small Signal Gain: >19dB
- Input Return Loss: >10dB
- Output Return Loss: >12dB
- Bias: V_D = 32V, I_{DQ} = 360mA, V_G = -2.6V Typical
- Wideband Flat Power
- Package Dimensions: 5.0 x 5.0 x 1.45 mm

Functional Block Diagram



General Description

TriQuint's TGA2237-SM is a wideband distributed amplifier fabricated on TriQuint's production 0.25um GaN on SiC process. The TGA2237-SM operates from 0.03 – 2.5GHz and provides greater than 10W of saturated output power with greater than 13dB of large signal gain and greater than 50% power-added efficiency.

The TGA2237-SM is available in a low-cost, surface mount 32 lead 5x5 AIN QFN. It is ideally suited to support both radar and communication applications across defense and commercial markets as well as electronic warfare. The TGA2237-SM is fully matched to 50Ω at both RF ports allowing for simple system integration. DC blocks are required on both RF ports and the drain voltage must be injected through an off chip bias-tee on the RF output port.

Lead-free and RoHS compliant.

Evaluation boards are available upon request.

Pad Configuration

Pad No.	Symbol
1-2, 4, 6, 8-9, 16-17,19, 21, 23-25, 32	GND
3, 7, 10-15, 18, 22, 27-31	NC
5	RF IN
20	RF OUT, DRAIN
26	GATE

Ordering Information

Part	ECCN	Description
TGA2237-SM	EAR99	0.03 – 2.5GHz 10W GaN Power Amplifier

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Absolute Maximum Ratings

Parameter	Value
Drain Voltage (V_D)	40V
Gate Voltage Range (V_G)	-8 to 0V
Drain Current (I_D)	1.2A
Gate Current (I_G)	-2.4 to 8.4mA
Power Dissipation (P_{DISS}), 85°C	19W
Input Power (P_{IN}), CW, 50 Ω, 85°C	33dBm(*)
Input Power (P_{IN}), CW, VSWR 3:1, V_D = 32V, 85°C	33dBm(*)
Max VSWR, CW, P_{IN} = 27dBm, V_D = 32V, 85°C (Load)	10:1
Channel Temperature (T_{CH})	275°C
Mounting Temperature (30 Seconds)	320°C
Storage Temperature	-55 to 150°C

Operation of this device outside the parameter ranges given above may cause permanent damage. These are stress ratings only, and functional operation of the device at these conditions is not implied.

Recommended Operating Conditions

Parameter	Value
Drain Voltage (V_D)	32V
Drain Current (I_{DQ})	360mA
Gate Voltage (V_G)	-2.6V (Typ.)

Electrical specifications are measured at specified test conditions. Specifications are not guaranteed over all recommended operating conditions.

(*) Operational input power must be limited to 26dBm when operating below 0.6GHz to prevent excessive forward gate current.

Electrical Specifications

Test conditions unless otherwise noted: 25^{0}C, V_D = 32V, I_{DQ} = 360mA, V_G = -2.6V Typical

Parameter	Min	Typical	Max	Units
Operational Frequency Range	0.03		2.5	GHz
Small Signal Gain		> 19		dB
Input Return Loss		> 10		dB
Output Return Loss		> 12		dB
Output Power (Pin = 27dBm)		> 40		dBm
Power Added Efficiency (Pin = 27dBm)		> 50		%
Power @ 1dB Compression (P1dB)		> 33		dBm
IM3 @ POUT/tone = 30dBm		-25		dBc
IM5 @ POUT/tone = 30dBm		-33		dBc
Small Signal Gain Temperature Coefficient		-0.03		dB/°C
Output Power Temperature Coefficient		-0.002		dBm/°C
Recommended Operating Voltage:	20	32		V

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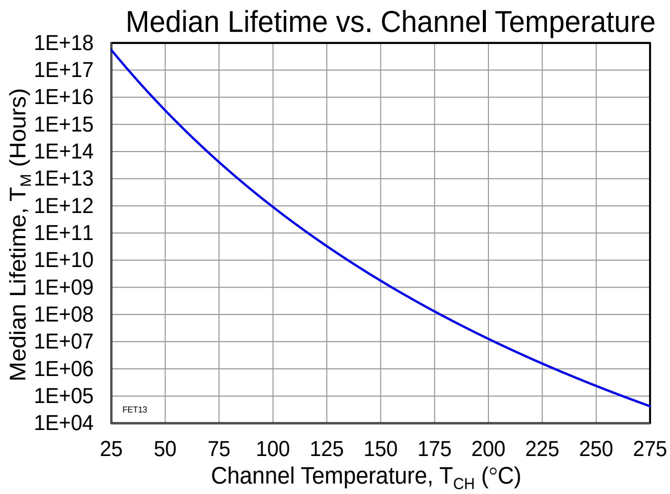
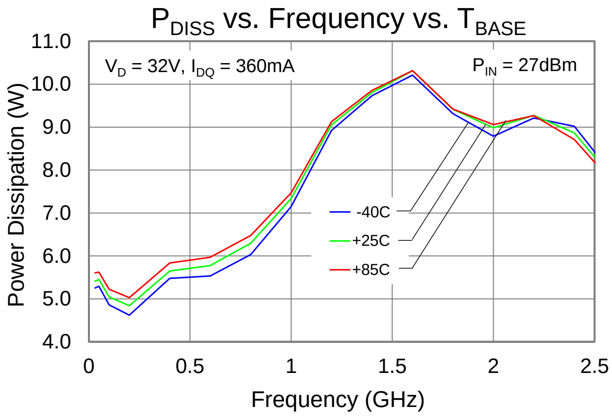
Thermal and Reliability Information

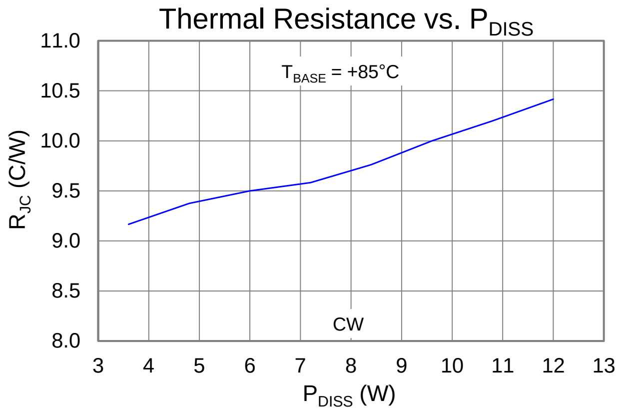
Parameter	Test Conditions	Value	Units
Thermal Resistance (θ_{JC}) (1)	T_{base} = 85°C, V_D = **32V** I_{DQ} = 360mA, $I_{D\ Drive}$ = 630mA P_{IN} = 27dBm, P_{OUT} = 40dBm, P_{DISS} = 10W	10.2	ºC/W
Channel Temperature (T_{CH}) (Under RF drive)		187	°C
Median Lifetime (T_M)		4.12 x 10^7	Hrs

Notes:
1. Thermal resistance measured to back of package.

Test Conditions: V_D = 40 V; Failure Criteria = 10% reduction in I_{D_MAX}







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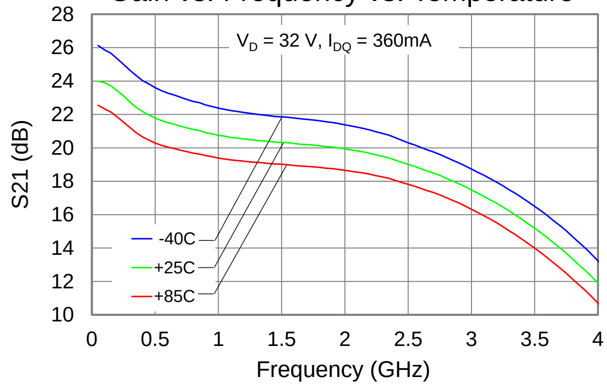
Typical Performance: Small Signal

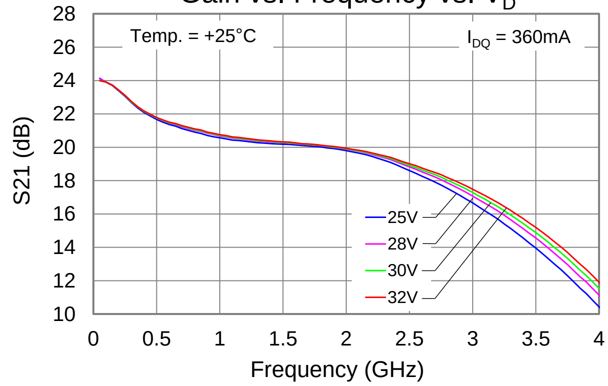
The plots reflect performance measured with an external coaxial bias tee and DC blocks

(See application circuit on page 11)

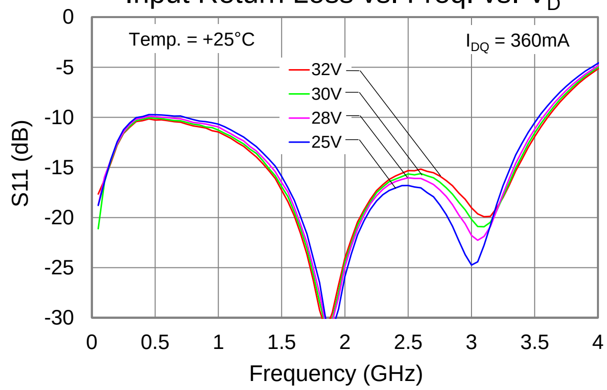
Gain vs. Frequency vs. Temperature



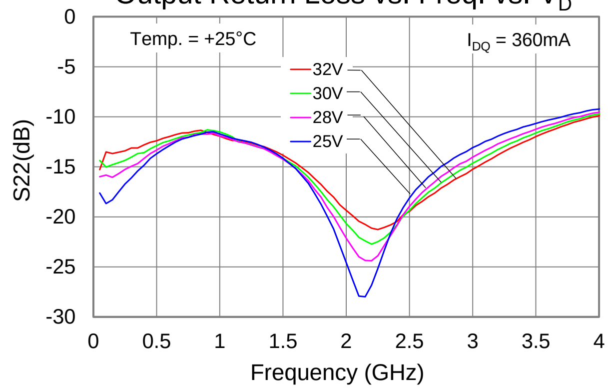
Gain vs. Frequency vs. V_D



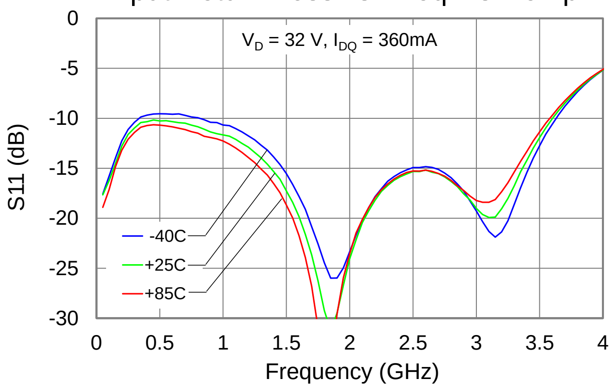
Input Return Loss vs. Freq. vs. V_D



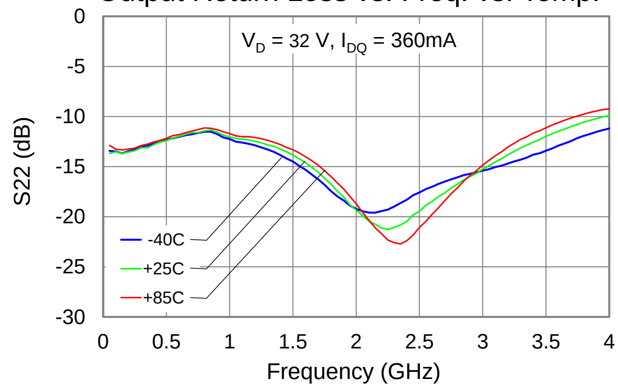
Output Return Loss vs. Freq. vs. V_D



Input Return Loss vs. Freq. vs. Temp.



Output Return Loss vs. Freq. vs. Temp.



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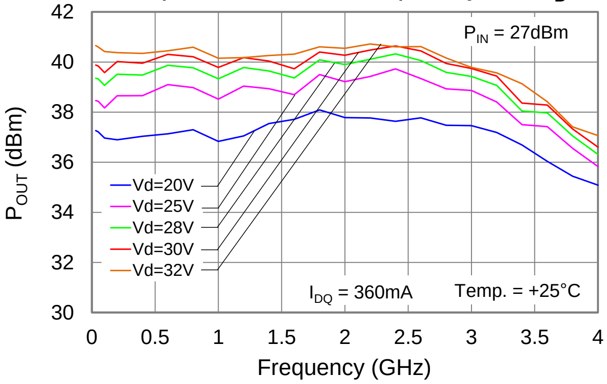
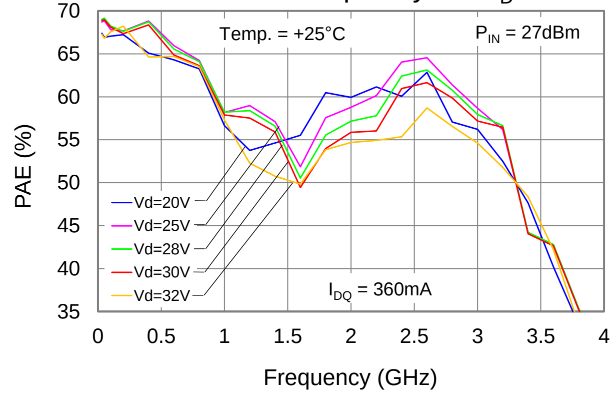
Typical Performance: Large Signal (CW)

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

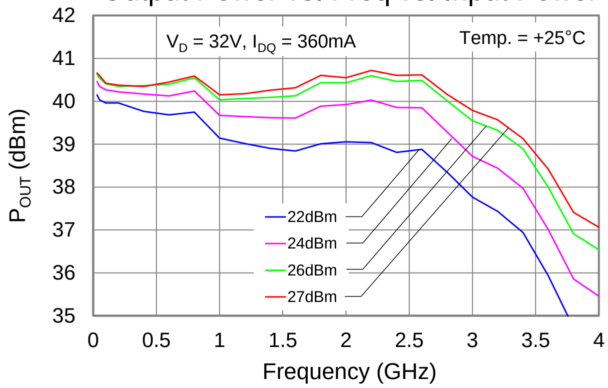
Output Power vs. Frequency vs. V_D



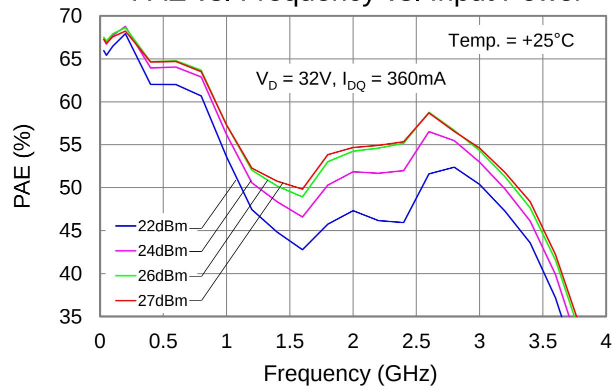
PAE vs. Frequency vs. V_D



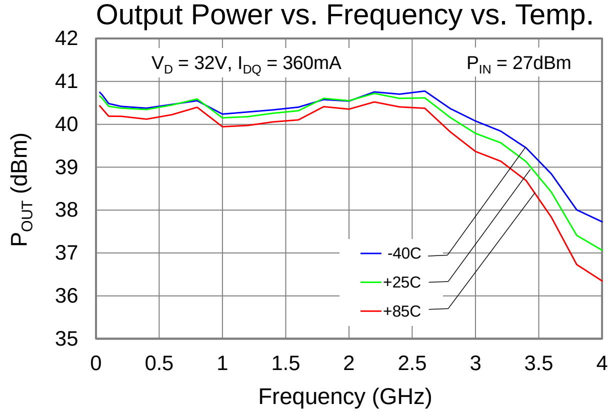
Output Power vs. Freq vs. Input Power



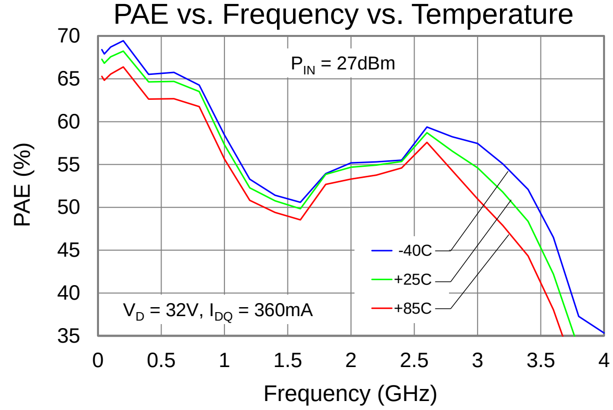
PAE vs. Frequency vs. Input Power



Output Power vs. Frequency vs. Temp.



PAE vs. Frequency vs. Temperature



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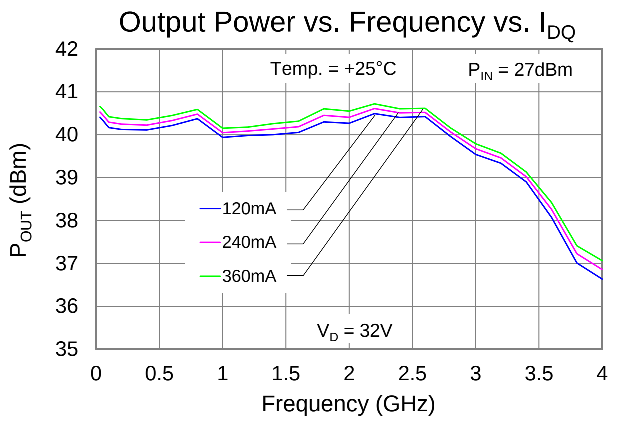
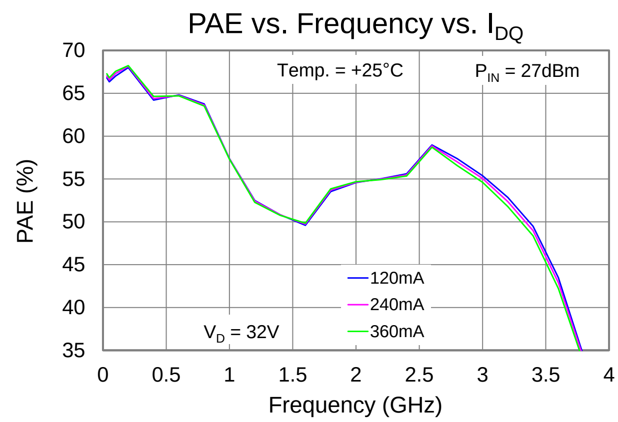
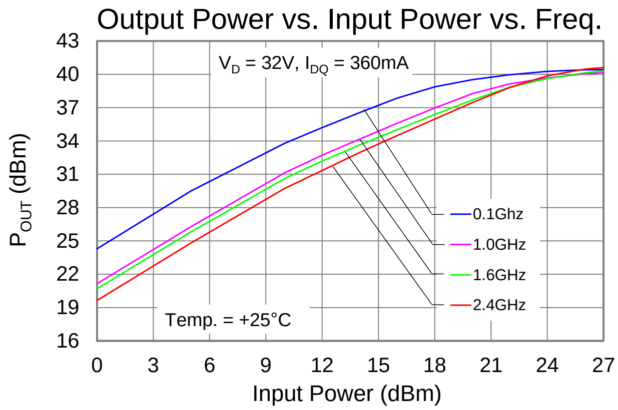
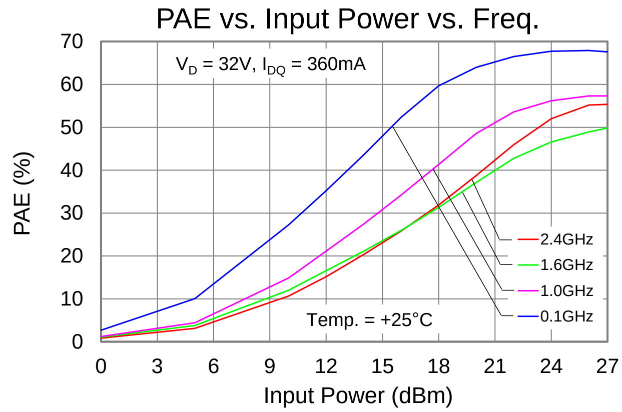
Typical Performance: Large Signal (CW)

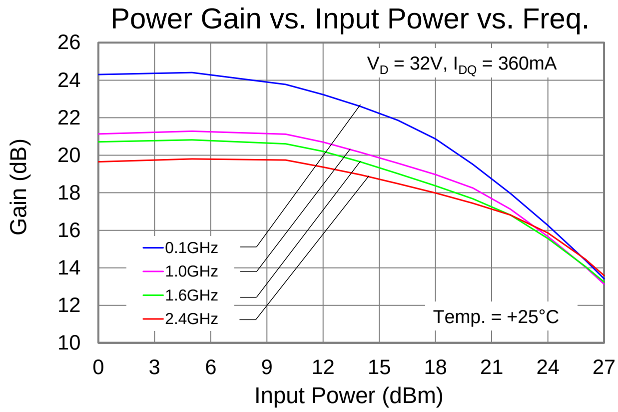
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

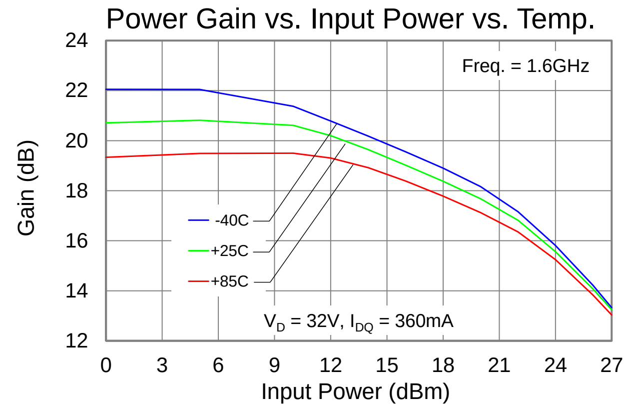












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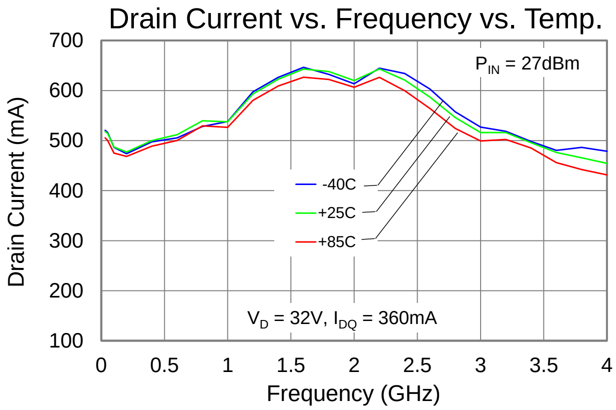
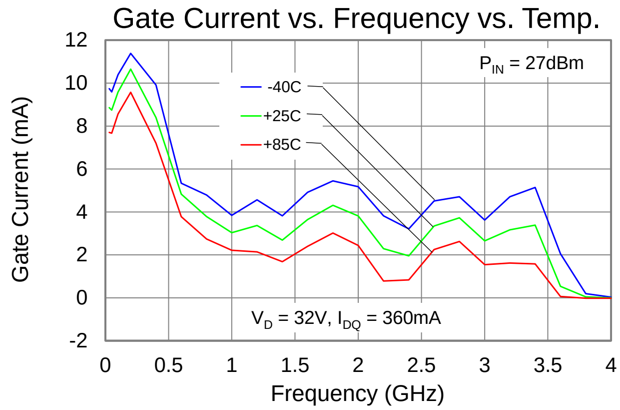
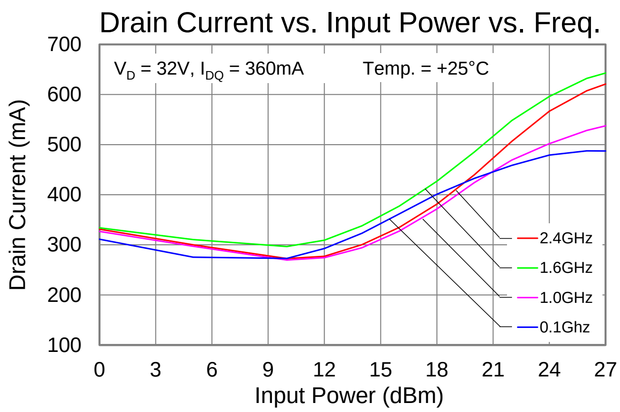
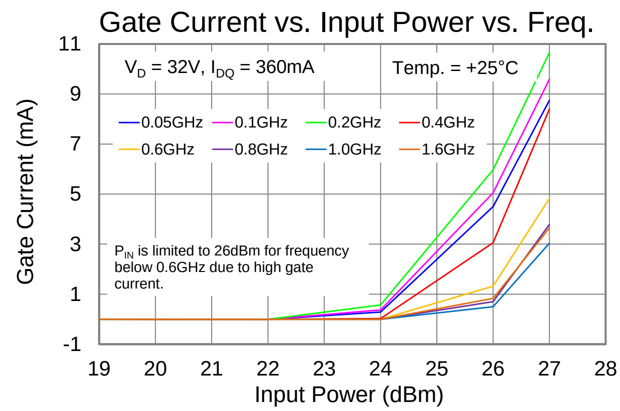
Typical Performance: Large Signal (CW)

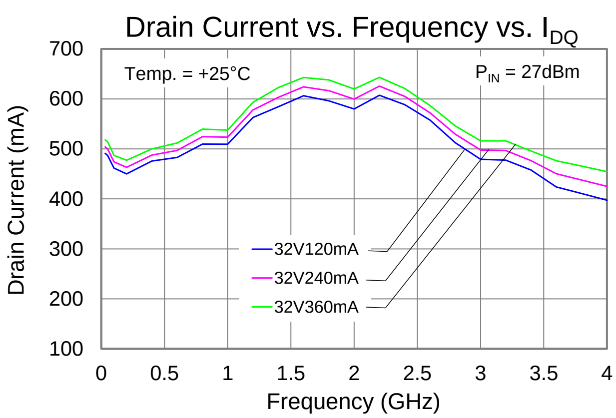
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

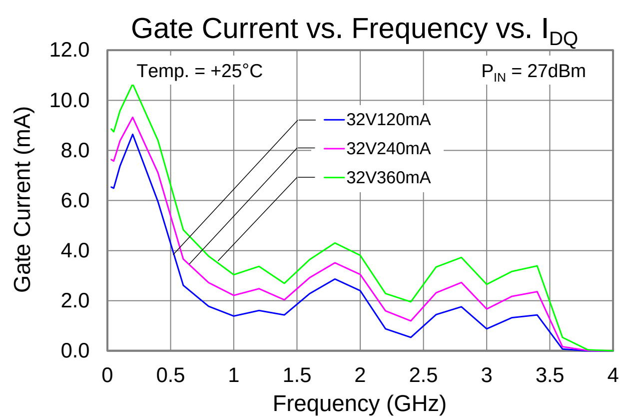












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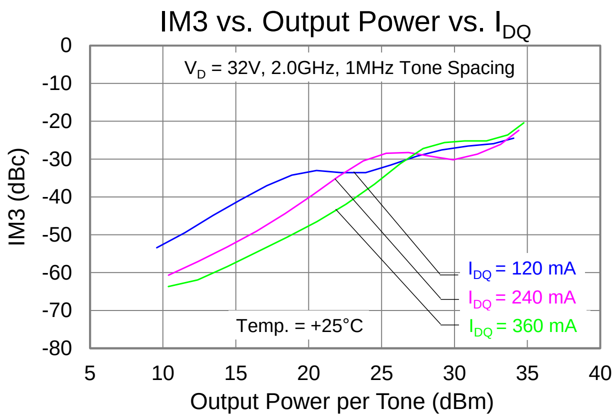
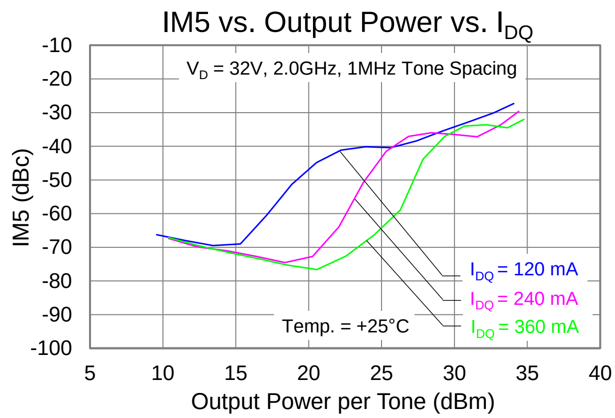
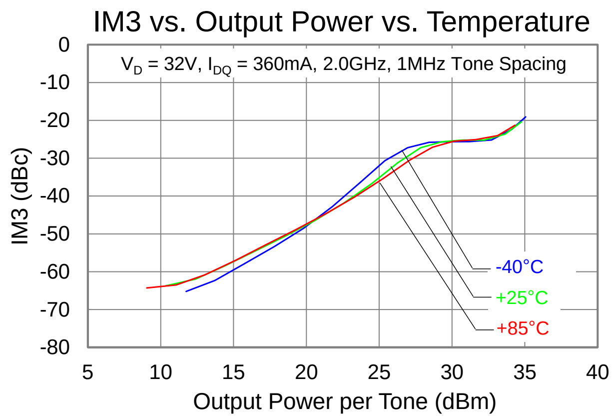
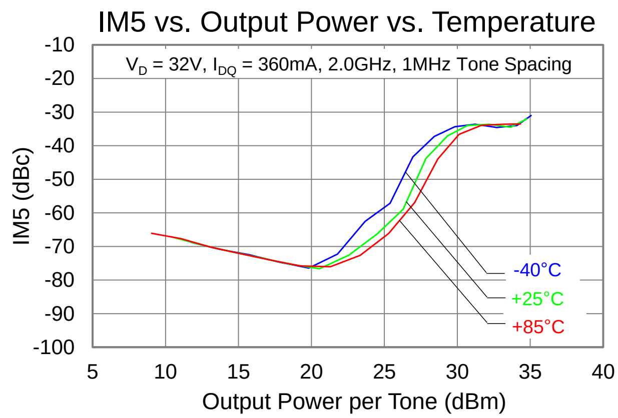
Typical Performance: Linearity

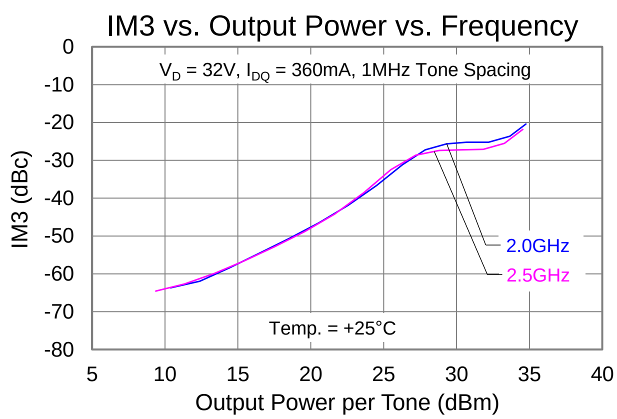
The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

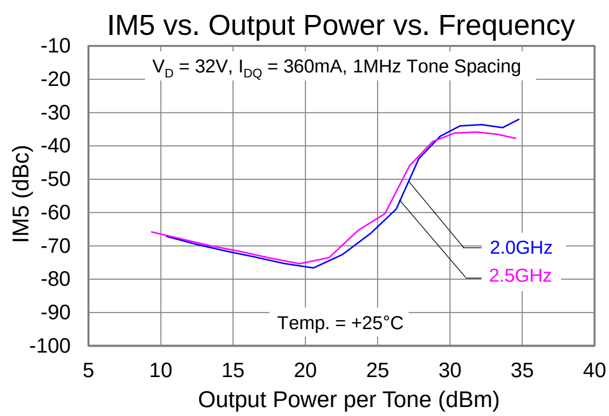












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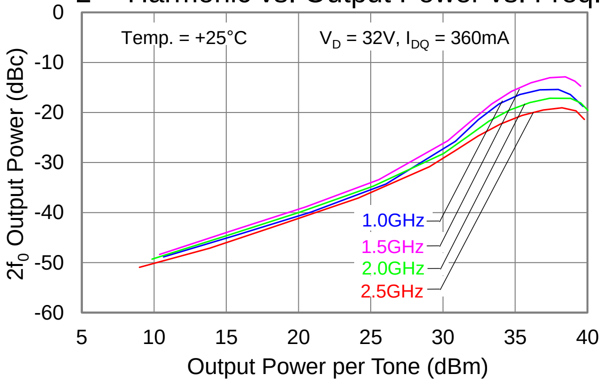
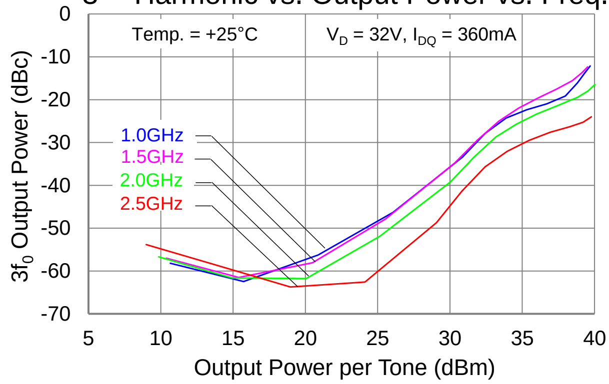
Typical Performance: Linearity

The plots reflect performance measured with an external coaxial bias tee and DC blocks
(See application circuit on page 11)

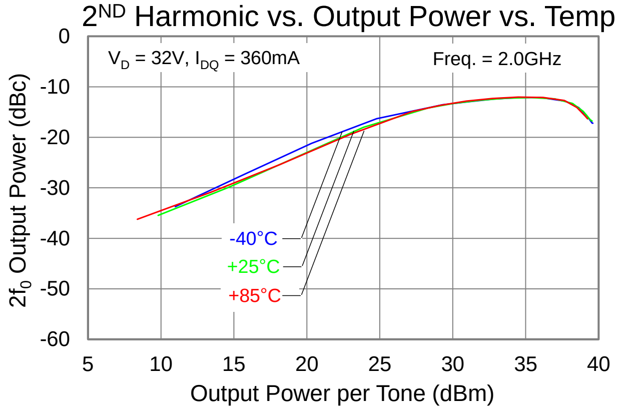
2ND Harmonic vs. Output Power vs. Freq.



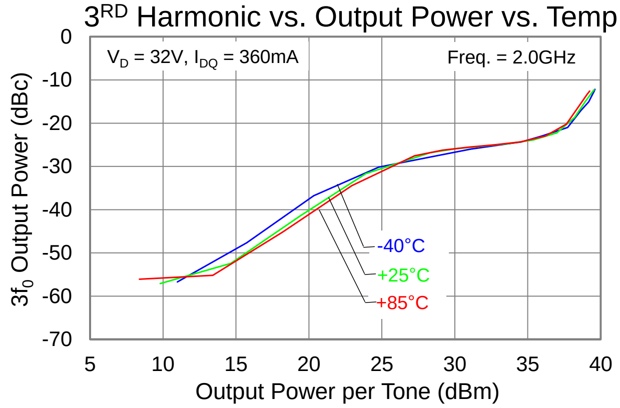
3RD Harmonic vs. Output Power vs. Freq.



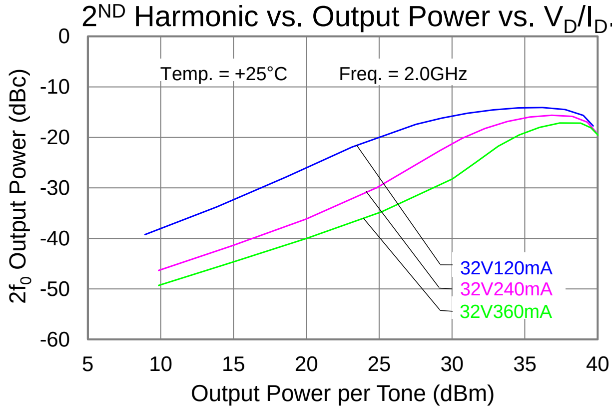
2ND Harmonic vs. Output Power vs. Temp.



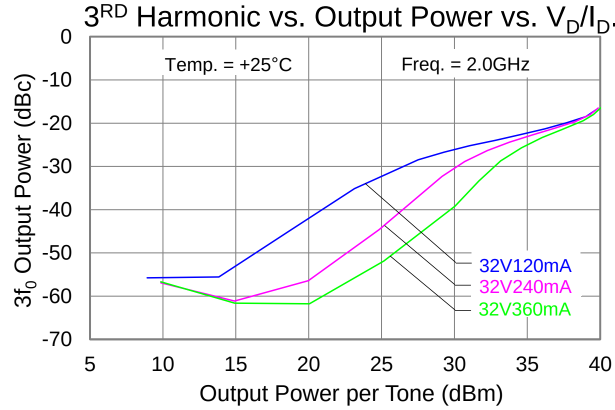
3RD Harmonic vs. Output Power vs. Temp.



2ND Harmonic vs. Output Power vs. V_D/I_D.



3RD Harmonic vs. Output Power vs. V_D/I_D.



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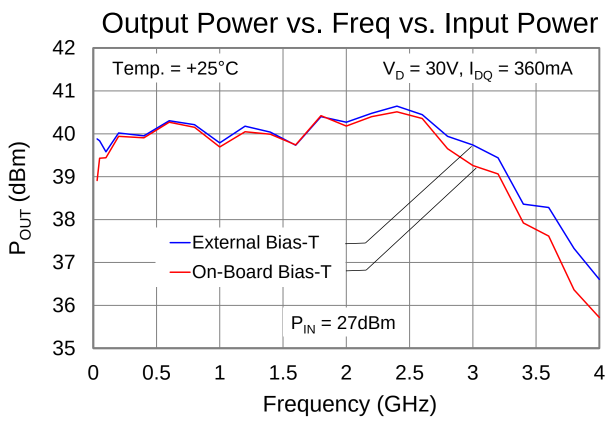
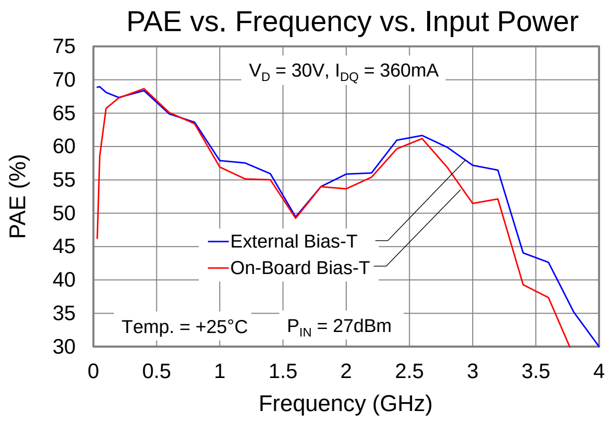
Typical Performance: Large Signal (CW), On-board vs. External Coaxial Bias-T

The plots below reflect performance measured between external bias tee and on-board bias tee
(See application circuit on pages 11 and 13)





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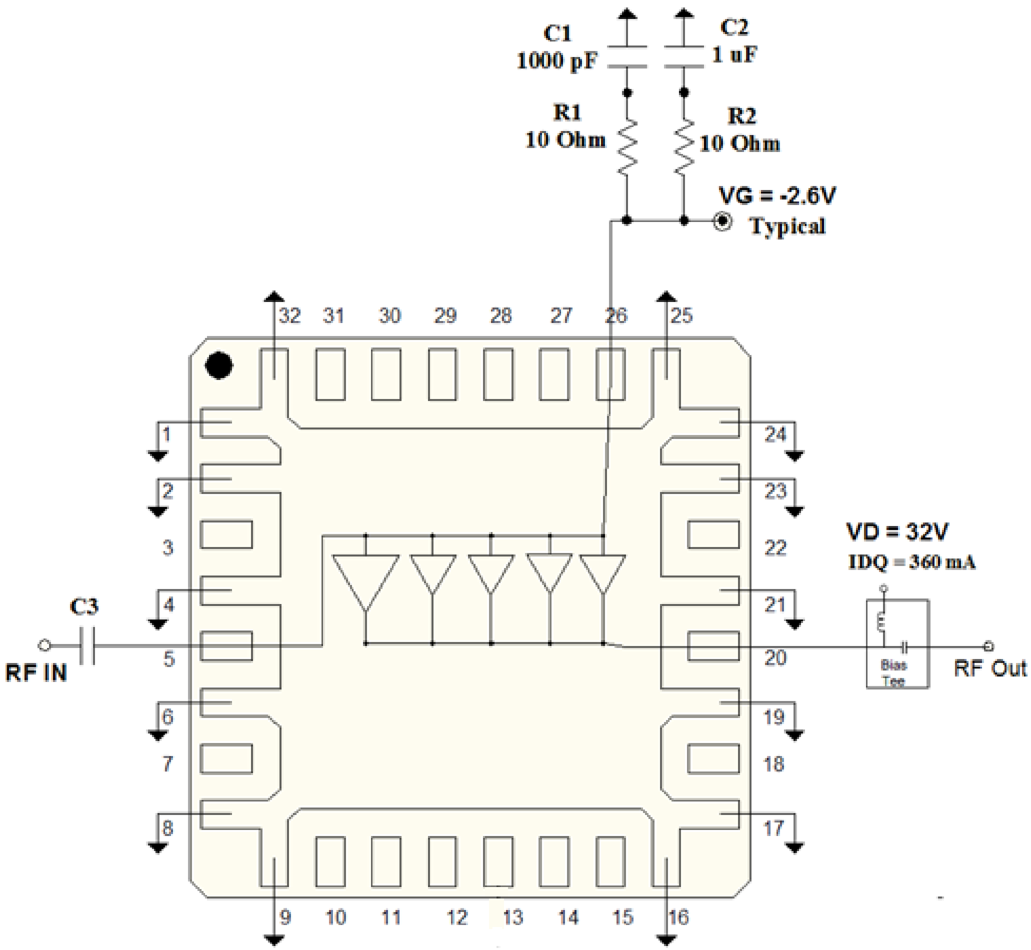
Application Circuit (Coaxial input DC block and coaxial output bias tee)



Notes:

1. Coaxial input DC block (C3) is used for input port (RF In.)
2. External wide bandwidth Bias-Tee is used for output port (RF Out). VD is applied through the output Bias-Tee.

Bias-up Procedure

1. Set I_D limit to 700mA, I_G limit to 7mA
2. Set V_G to -5.0V
3. Set VD +32V
4. Adjust V_G more positive until I_{DQ} = 360mA (V_G ~ -2.6V Typical)
5. Apply RF signal *

Bias-down Procedure

1. Turn off RF signal
2. Reduce V_G to -5.0V. Ensure I_{DQ} ~ 0mA
3. Set V_D to 0V
4. Turn off V_D supply
5. Turn off V_G supply

(*) P_{IN} is limited to 26dBm for frequency < 0.6GHz due to high gate current.

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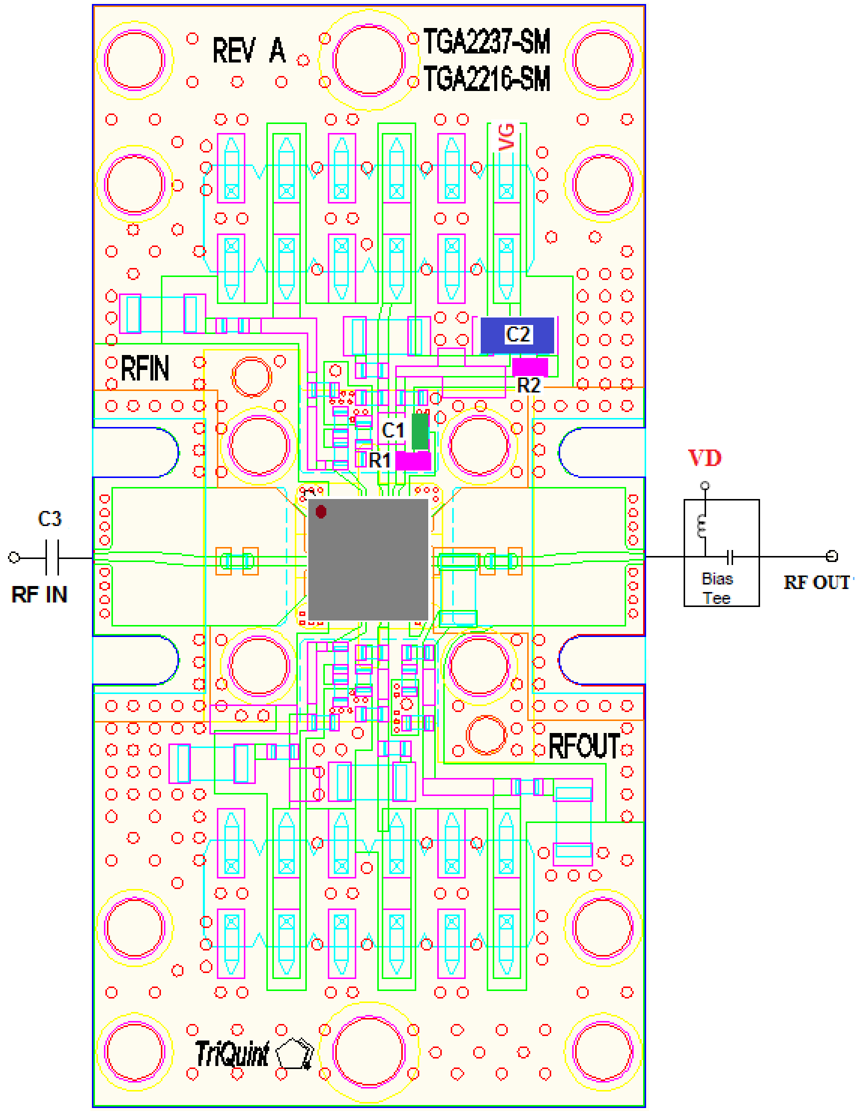
Assembly Drawing (Coaxial input DC block and coaxial output bias tee)



Bill of Materials

Reference Design	Value	Description	Manufacturer	Part Number
C1	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
C2	1uF	Cap, 1206, 50V, 10%, X7R	Various	
C3		DC Block	Various	
R1 – R2	10Ω	Res, 0402	Various	

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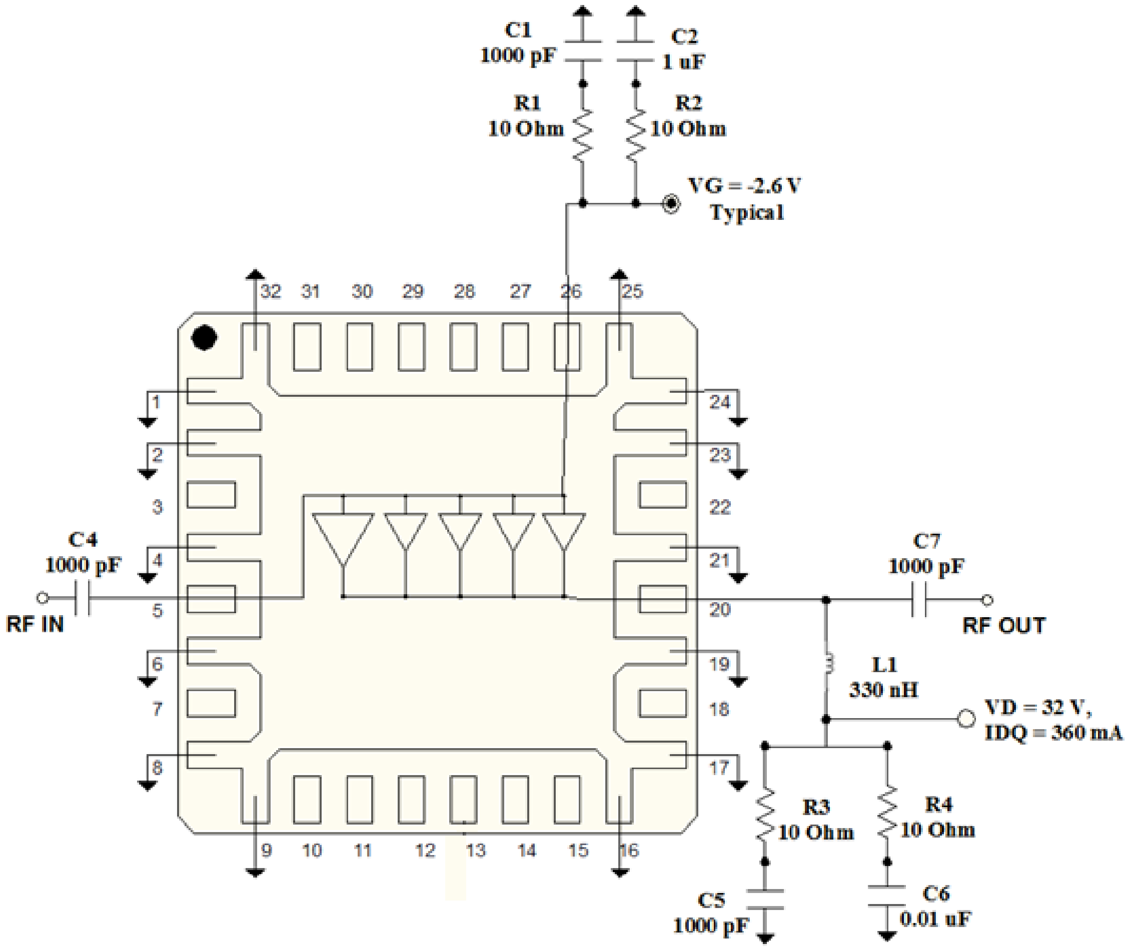
Application Circuit (Option with board-level DC blocks and output bias tee)



Notes:

1. Performance of the DUT with surface mount DC blocks and bias tee components may be degraded relative to the coaxial option. These components should be optimized for the desired operational bandwidth.

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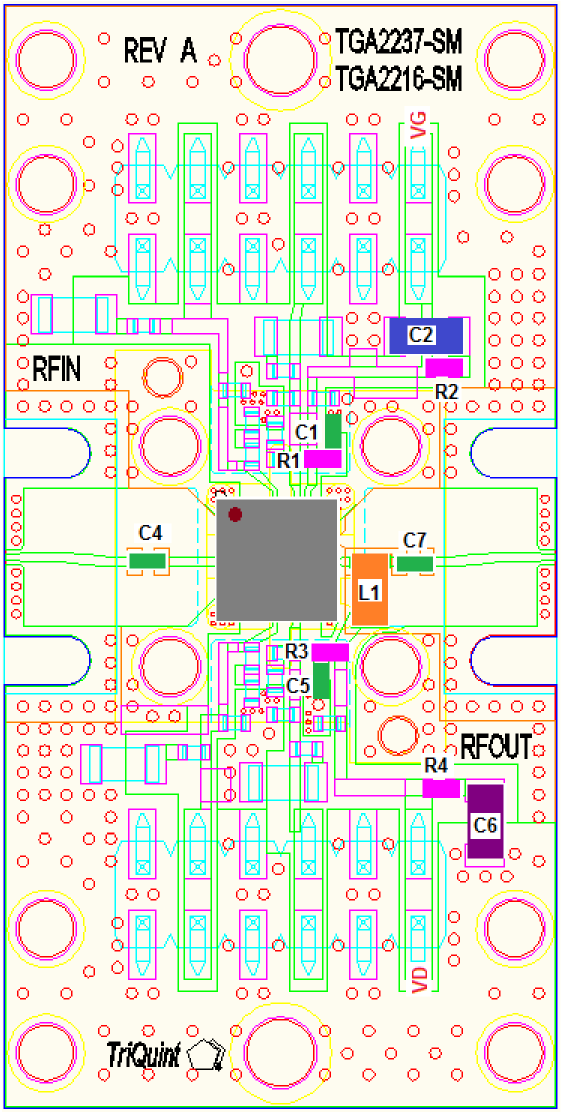
Evaluation Board Layout with On-Board DC Blocks and Output Bias-T Option



Bill of Materials For On-Board Bias-Tee

Reference Design	Value	Description	Manufacturer	Part Number
C1, C4, C5, C7	1000pF	Cap, 0402, 100V, 10%, X7R	Various	
C2	1uF	Cap, 1206, 50V, 10%, X7R	Various	
C6	0.01uF	Cap, 1206, 100V, 10%, X7R	Various	
L1	330nH	Ind, 1206, 100V, 10%, X7R	Various	
R1 – R4	10Ω	Res, 0402	Various	

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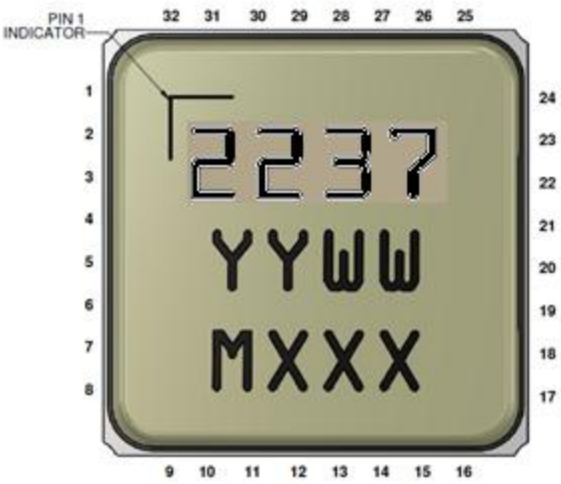
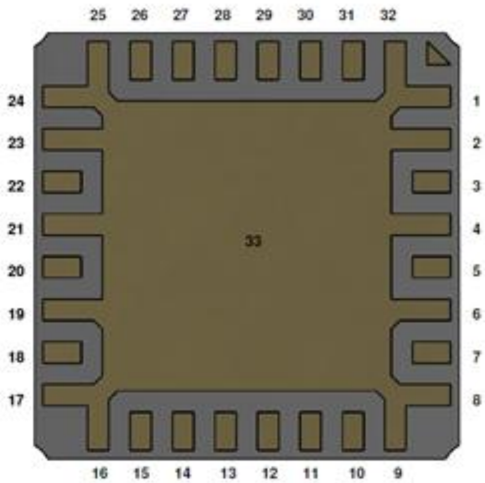
Pin Layout





Pin Description

Pin No.	Symbol	Description
1-2, 4, 6, 8-9, 16-17, 19, 21, 23-25, 32	GND	Connected to ground paddle (pin 33); must be grounded on PCB
3, 7, 10-15, 18, 22, 27-31	NC	No connection
5	RF IN	Input; matched to 50 Ω.
20	RF OUT/ DRAIN	Output; matched to 50 Ω.
26	GATE	GATE voltage; bias network is required; see recommended Application Information on page 11
33	GND	Ground Paddle. Multiple vias should be employed to minimize inductance and thermal resistance.

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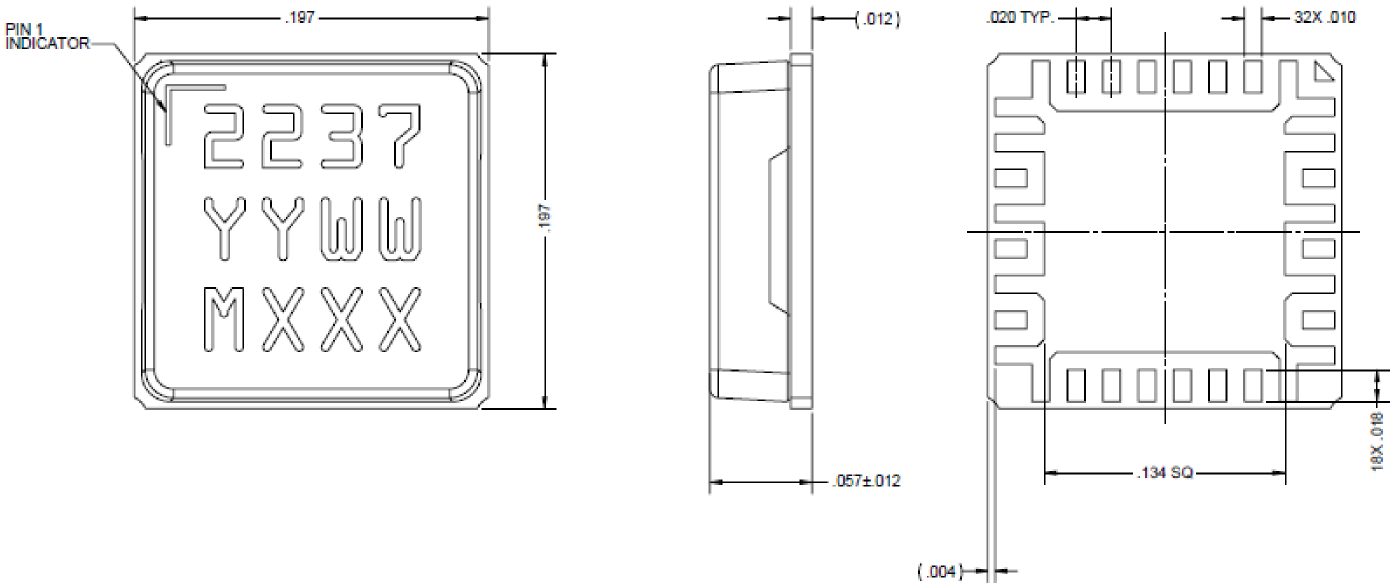
Mechanical Information



Units: inches

Tolerances: unless specified

x.xx = ± 0.01

x.xxx = ± 0.005

Materials:

Base: Ceramic

Lid: Plastic

All metalized features are gold plated

Part is epoxy sealed

Marking:

2237: Part number

YY: Part Assembly year

WW: Part Assembly week

MXXX: Batch ID

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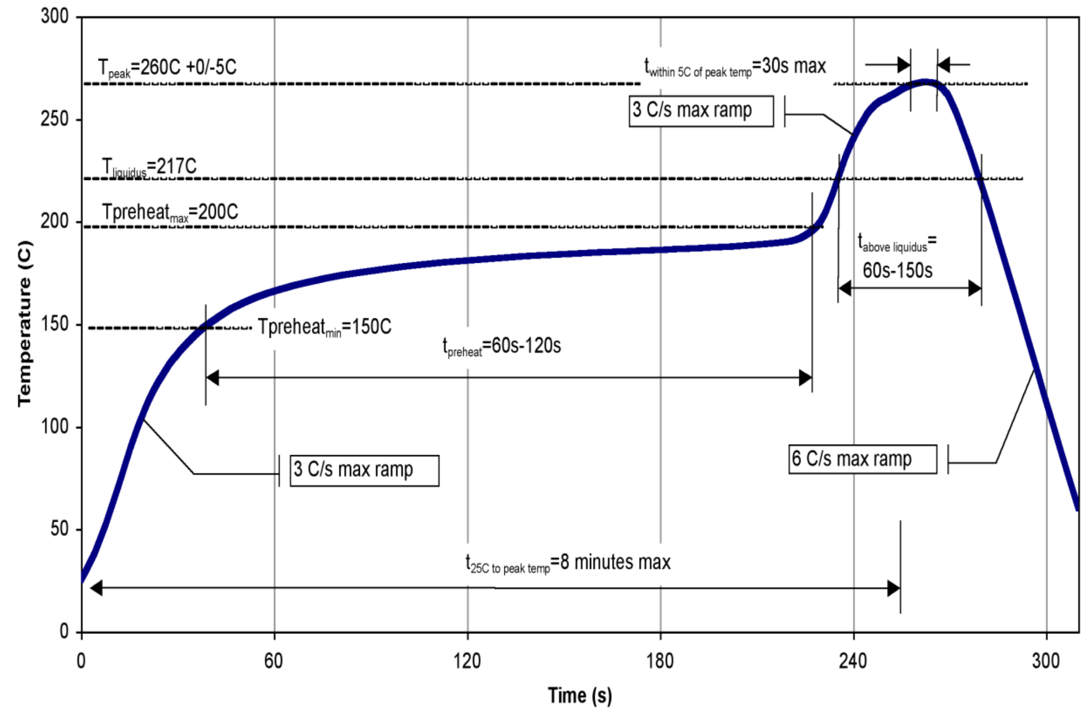
Recommended Soldering Temperature Profile



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Product Compliance Information

ESD Sensitivity Ratings

Caution! ESD-Sensitive Device

ESD Rating: TBD
Value: TBD
Test: Human Body Model (HBM)
Standard: JEDEC Standard JESD22-A114

MSL Rating

Level TBD at 260°C convection reflow
The part is rated Moisture Sensitivity Level TBD at TBD°C per JEDEC standard IPC/JEDEC J-STD-020.

Solderability

Compatible with the latest version of J-STD-020 Lead free solder, 260°C.

This product also has the following attributes:

- Lead Free
- Halogen Free (Chlorine, Bromine)
- Antimony Free
- TBBP-A ($C_{15}H_{12}Br_{4}0_{2}$) Free
- PFOS Free
- SVHC Free

ECCN

US Department of Commerce: EAR99

Contact Information

For the latest specifications, additional product information, worldwide sales and distribution locations, and information about TriQuint:

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