Micropower Quad-Channel Digital Isolators

Data Sheet **ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447**

FEATURES

- **Ultralow power operation**
  - **3.3 V operation (typical)**
    - **5.6 µA per channel quiescent current, refresh enabled**
    - **0.3 µA per channel quiescent current, refresh disabled**
    - **148 µA/Mbps per channel typical dynamic current**
  - **2.5 V operation (typical)**
    - **3.1 µA per channel quiescent current, refresh enabled**
    - **0.1 µA per channel quiescent current, refresh disabled**
    - **117 µA/Mbps per channel typical dynamic current**
- **Small, 16-lead QSOP**
- **Bidirectional communication**
- **Up to 2 Mbps data rate (NRZ)**
- **High temperature operation: 125°C**
- **High common-mode transient immunity: >25 kV/µs**
- **Safety and regulatory approvals**
  - **UL 1577 Component Recognition Program (pending)**
    - **2500 V rms for 1 minute per UL 1577**
  - **CSA Component Acceptance Notice #5A (pending)**
  - **VDE Certificate of Conformity (pending)**
    - **DIN V VDE V 0884-10 (VDE V 0884-10):2006-12**
    - **V_{IORM} = 560 V_{PEAK}**

APPLICATIONS

General-purpose, low power multichannel isolation
1 MHz, low power peripheral interface (SPI)
4 mA to 20 mA loop process controls

GENERAL DESCRIPTION

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447[1] are micropower, 4-channel digital isolators based on the Analog Devices, Inc., *i*Coupler® technology. Combining high speed, complementary metal oxide semiconductor (CMOS) and monolithic air core transformer technologies, these isolation components provide outstanding performance characteristics superior to the alternatives, such as optocoupler devices. As shown in Figure 2, in standard operating mode, when EN_x = 0 (internal refresh enabled), the current per channel is less than 10 µA. When EN_x = 1 (internal refresh disabled), the current per channel drops to less than 1 µA.

FUNCTIONAL BLOCK DIAGRAM

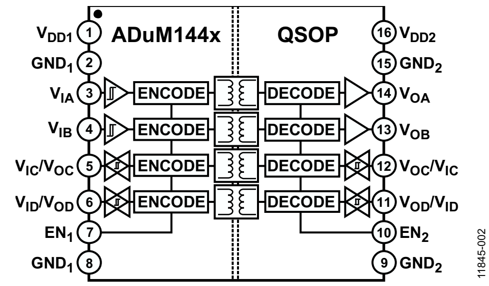

Figure 1.

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 family of quad 2.5 kV digital isolation devices are packaged in a small 16-lead QSOP, freeing almost 70% of board space compared to isolators packages in wide body SOIC packages. The devices withstand high isolation voltages and meet regulatory requirements, such as UL and CSA standards (pending). In addition to the space savings, the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 operate with supplies as low as 2.25 V.

Despite the low power consumption, all models of the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 provide low, pulse width distortion at <8 ns. In addition, every model has an input glitch filter to protect against extraneous noise disturbances.

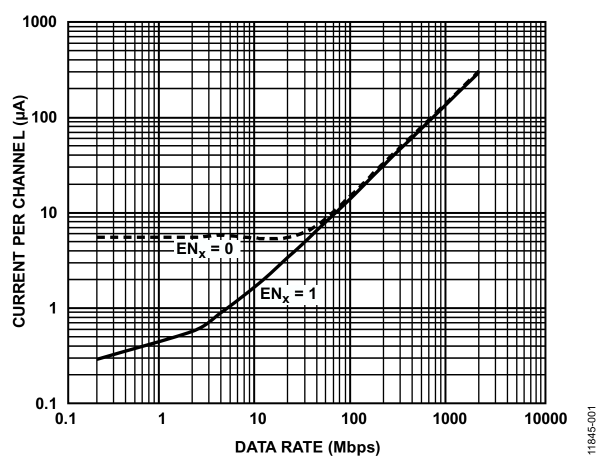

Figure 2. Typical Total Supply Current per Channel (V_{DDx} = 3.3 V)

[1] Protected by U.S. Patents 5,952,849, 6,873,065, 7,075,329, 6,262,600. Other patents pending.

Rev. 0 Document Feedback

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REVISION HISTORY

10/13—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF, and CMOS signal levels, unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within pulse-width distortion (PWD) limit
Propagation Delay	t_{PHL}, t_{PLH}		80	180	ns	50% input to 50% output
Change vs. Temperature			200		ps/°C	
Minimum Pulse Width	PW	500			ns	Within PWD limit
Pulse-Width Distortion	PWD			8	ns	$\lvert t_{PLH} - t_{PHL}\rvert$
Propagation Delay Skew[1]	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			15	ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} and t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1440/ADuM1445	I_{DD1}		732	1000	μA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		492	750	μA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
ADuM1441/ADuM1446	I_{DD1}		672	900	μA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		552	900	μA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
ADuM1442/ADuM1447	I_{DD1}		612	900	μA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		612	900	μA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V

Table 3. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 V_{DDx}[1]			V	
Logic Low	V_{IL}			0.3 V_{DDx}[1]	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx}[1] − 0.1	3.0		V	$I_{OUTx} = −20$ μA, $V_{Ix} = V_{IxH}$
		V_{DDx}[1] − 0.4	2.8		V	$I_{OUTx} = −4$ mA, $V_{Ix} = V_{IxH}$
Logic Low	V_{OL}		0.0	0.1	V	$I_{OUTx} = 20$ μA, $V_{Ix} = V_{IxL}$
			0.2	0.4	V	$I_{OUTx} = 4$ mA, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_I	−1	+0.01	+1	μA	0 V ≤ V_{Ix} ≤ V_{DDx}[1]
Input Switching Thresholds						
Positive Threshold Voltage	V_{T+}		1.8		V	
Negative Going Threshold	V_{T-}		1.2		V	
Input Hysteresis	ΔV_T		0.6		V	
Undervoltage Lockout, V_{DD1} or V_{DD2}	UVLO		1.5		V	
Supply Current per Channel						
Quiescent Current						
Input Supply	$I_{DDI (Q)}$		4.8	10	μA	EN_X low
Output Supply	$I_{DDO (Q)}$		0.8	3.3	μA	EN_X low
Input (Refresh Off)	$I_{DDI (Q)}$		0.12		μA	EN_X high
Output (Refresh Off)	$I_{DDO (Q)}$		0.13		μA	EN_X high
Dynamic Supply Current						
Input	$I_{DDI (D)}$		88		μA/Mbps	
Output	$I_{DDO (D)}$		60		μA/Mbps	
AC SPECIFICATIONS						
Output Rise Time/Fall Time	t_R/t_F		2		ns	10% to 90%
Common-Mode Transient Immunity[2]	|CM|	25	40		kV/μs	$V_{Ix} = V_{DDx}$[1], $V_{CM} = 1000$ V, transient magnitude = 800 V
Refresh Rate	f_r		14		kbps	

[1] $V_{DDx} = V_{DD1}$ or V_{DD2}.
[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining $V_{OUT} > 0.8\ V_{DDx}$. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—2.5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V ≤ V_{DD1} ≤ 2.75 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF, and CMOS signal levels, unless otherwise noted.

Table 4.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within PWD limit
Propagation Delay	t_{PHL}, t_{PLH}		112	180	ns	50% input to 50% output
Change vs. Temperature			280		ps/°C	
Pulse-Width Distortion	PWD			12	ns	$\|t_{PLH} - t_{PHL}\|$
Minimum Pulse Width	PW	500			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			30	ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 5.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1440/ADuM1445	I_{DD1}		623	800	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		337	500	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
ADuM1441/ADuM1446	I_{DD1}		552	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		409	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
ADuM1442/ADuM1447	I_{DD1}		480	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		480	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V

Table 6. For All Models

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
DC SPECIFICATIONS						
Input Threshold						
Logic High	V_{IH}	0.7 V_{DDx}[1]			V	
Logic Low	V_{IL}			0.3 V_{DDx}[1]	V	
Output Voltages						
Logic High	V_{OH}	V_{DDx}[1] − 0.1	2.5		V	I_{Ox} = −20 µA, $V_{Ix} = V_{IxH}$
		V_{DDx}[1] − 0.4	2.35		V	I_{Ox} = −4 mA, $V_{Ix} = V_{IxH}$
Logic Low	V_{OL}		0.0	0.1	V	I_{Ox} = 20 µA, $V_{Ix} = V_{IxL}$
			0.1	0.4	V	I_{Ox} = 4 mA, $V_{Ix} = V_{IxL}$
Input Current per Channel	I_I	−1	+0.01	+1	µA	0 V ≤ V_{Ix} ≤ V_{DDx}[1]
Input Switching Thresholds						
Positive Threshold Voltage	V_{T+}		1.5		V	
Negative Going Threshold	V_{T-}		1.0		V	
Input Hysteresis	ΔV_T		0.5		V	
Undervoltage Lockout, V_{DD1} or V_{DD2}	UVLO		1.5		V	
Supply Current per Channel						
Quiescent Current						
Input Supply	$I_{DDI\,(Q)}$		2.6	3.3	µA	EN_X low
Output Supply	$I_{DDO\,(Q)}$		0.5	1.8	µA	EN_X low
Input (Refresh Off)	$I_{DDI\,(Q)}$		0.05		µA	EN_X high
Output (Refresh Off)	$I_{DDO\,(Q)}$		0.05		µA	EN_X high
Dynamic Supply Current						
Input	$I_{DDI\,(D)}$		76		µA/Mbps	
Output	$I_{DDO\,(D)}$		41		µA/Mbps	
AC SPECIFICATIONS						
Output Rise Time/Fall Time	t_R/t_F		2		ns	10% to 90%
Common-Mode Transient Immunity[2]	|CM|	25	40		kV/µs	$V_{Ix} = V_{DDx}$[1], V_{CM} = 1000 V, transient magnitude = 800 V
Refresh Rate	f_r		14		kbps	

[1] $V_{DDx} = V_{DD1}$ or V_{DD2}.

[2] |CM| is the maximum common-mode voltage slew rate that can be sustained while maintaining V_{OUT} > 0.8 V_{DDx}. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

ELECTRICAL CHARACTERISTICS—V_{DD1} = 3.3 V, V_{DD2} = 2.5 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 3.3 V, and V_{DD2} = 2.5 V. Minimum/maximum specifications apply over the entire recommended operating range of 3.0 V ≤ V_{DD1} ≤ 3.6 V, 2.25 V ≤ V_{DD2} ≤ 2.75 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF, and CMOS signal levels, unless otherwise noted.

For dc specifications and ac specifications, see Table 3 for Side 1 and see Table 6 for Side 2.

Table 7.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within PWD limit
Propagation Delay						
Side 1 to Side 2	t_{PHL}, t_{PLH}		84	180	ns	50% input to 50% output
Side 2 to Side 1	t_{PHL}, t_{PLH}		120	180	ns	50% input to 50% output
Change vs. Temperature			280		ps/°C	
Pulse-Width Distortion	PWD			12	ns	$\lvert t_{PLH} - t_{PHL}\rvert$
Pulse Width	PW	500			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			60	ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 8.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1440/ADuM1445	I_{DD1}		732	1000	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		337	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
ADuM1441/ADuM1446	I_{DD1}		672	900	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		409	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
ADuM1442/ADuM1447	I_{DD1}		612	900	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		480	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V

ELECTRICAL CHARACTERISTICS—V_{DD1} = 2.5 V, V_{DD2} = 3.3 V OPERATION

All typical specifications are at T_A = 25°C, V_{DD1} = 2.5, and V_{DD2} = 3.3 V. Minimum/maximum specifications apply over the entire recommended operating range of 2.25 V ≤ V_{DD1} ≤ 2.75 V, 3.0 V ≤ V_{DD2} ≤ 3.6 V, and −40°C ≤ T_A ≤ +125°C, unless otherwise noted. Switching specifications are tested with C_L = 15 pF, and CMOS signal levels, unless otherwise noted.

For dc specifications and ac specifications, see Table 6 for Side 1 and see Table 3 for Side 2.

Table 9.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SWITCHING SPECIFICATIONS						
Data Rate				2	Mbps	Within PWD limit
Propagation Delay						
Side 1 to Side 2	t_{PHL}, t_{PLH}		120	180	ns	50% input to 50% output
Side 2 to Side 1	t_{PHL}, t_{PLH}		84	180	ns	50% input to 50% output
Change vs. Temperature			200		ps/°C	
Pulse-Width Distortion	PWD			12	ns	$\|t_{PLH} − t_{PHL}\|$
Pulse Width	PW	500			ns	Within PWD limit
Propagation Delay Skew[1]	t_{PSK}			10	ns	
Channel Matching						
Codirectional	t_{PSKCD}			10	ns	
Opposing Direction	t_{PSKOD}			60	ns	

[1] t_{PSK} is the magnitude of the worst-case difference in t_{PHL} or t_{PLH} that is measured between units at the same operating temperature, supply voltages, and output load within the recommended operating conditions.

Table 10.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
SUPPLY CURRENT						2 Mbps, no load
ADuM1440/ADuM1445	I_{DD1}		623	1000	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		492	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
ADuM1441/ADuM1446	I_{DD1}		552	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		552	900	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
ADuM1442/ADuM1447	I_{DD1}		480	750	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V
	I_{DD2}		612	900	µA	EN_X = 0 V, V_{IH} = V_{DD}, V_{IL} = 0 V

PACKAGE CHARACTERISTICS

Table 11.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
Resistance (Input-to-Output)[1]	R_{I-O}		10^{13}		Ω	
Capacitance (Input-to-Output)[1]	C_{I-O}		2		pF	f = 1 MHz
Input Capacitance[2]	C_I		4.0		pF	
IC Junction-to-Ambient Thermal Resistance	$θ_{JA}$		76		°C/W	Thermocouple located at center of package underside

[1] The device is considered a 2-terminal device: Pin 1 through Pin 8 are shorted together, and Pin 9 through Pin 16 are shorted together.
[2] Input capacitance is from any input data pin to ground.

REGULATORY INFORMATION

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 are pending approval by the organizations listed in Table 12. See Table 17 and the Insulation Lifetime section for the recommended maximum working voltages for specific cross-isolation waveforms and insulation levels.

Table 12.

UL (Pending)	CSA (Pending)	VDE (Pending)
Recognized under UL 1577 Component Recognition Program[1]	Approved under CSA Component Acceptance Notice #5A	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10):2006-12[2]
Single protection, 2500 V rms isolation voltage	Basic insulation per CSA 60950-1-03 and IEC 60950-1, 400 V rms (566 V_{PEAK}) maximum working voltage	Reinforced insulation, 565 V_{PEAK}
File E214100	File 205078	File 2471900-4880-0001

[1] In accordance with UL 1577, each ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 is proof tested by applying an insulation test voltage of ≥3000 V rms for 1 sec (current leakage detection limit = 5 μA).
[2] In accordance with DIN V VDE V 0884-10, each ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 is proof tested by applying an insulation test voltage ≥1050 V_{PEAK} for 1 second (partial discharge detection limit = 5 pC). The asterisk (*) marked on the component designates DIN V VDE V 0884-10 approval.

INSULATION AND SAFETY-RELATED SPECIFICATIONS

Table 13.

Parameter	Symbol	Value	Unit	Test Conditions/Comments
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Tracking and Air Gap (Creepage and Clearance)	L(I02)	3.1	mm min	Measured from input terminals to output terminals, shortest distance path along body
Minimum Clearance in the Plane of the Printed Circuit Board (PCB Clearance)	L(I01)	3.8	mm min	Measured from input terminals to output terminals, shortest distance through air, line of sight, in the PCB mounting plane
Minimum Internal Gap (Internal Clearance)		0.017	mm min	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>400	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		II		Material Group (DIN VDE 0110, 1/89, Table 1)

DIN V VDE V 0884-10 (VDE V 0884-10):2006-12 INSULATION CHARACTERISTICS

These isolators are suitable for reinforced electrical isolation within the safety limit data only. Maintenance of the safety data is ensured by protective circuits. The asterisk (*) marked on packages denotes DIN V VDE V 0884-10 approval.

Table 14.

Description	Test Conditions/Comments	Symbol	Characteristic	Unit
Installation Classification per DIN VDE 0110				
For Rated Mains Voltage ≤ 150 V rms			I to IV	
For Rated Mains Voltage ≤ 300 V rms			I to III	
For Rated Mains Voltage ≤ 400 V rms			I to II	
Climatic Classification			40/105/21	
Pollution Degree per DIN VDE 0110, Table 1			2	
Maximum Working Insulation Voltage		V_{IORM}	560	V_{PEAK}
Input-to-Output Test Voltage, Method b1	$V_{IORM} \times 1.875 = V_{pd(m)}$, 100% production test, $t_{ini} = t_m = 1$ sec, partial discharge < 5 pC	$V_{pd(m)}$	1050	V_{PEAK}
Input-to-Output Test Voltage, Method a				
After Environmental Tests Subgroup 1	$V_{IORM} \times 1.5 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	840	V_{PEAK}
After Input and/or Safety Test Subgroup 2 and Subgroup 3	$V_{IORM} \times 1.2 = V_{pd(m)}$, $t_{ini} = 60$ sec, $t_m = 10$ sec, partial discharge < 5 pC	$V_{pd(m)}$	672	V_{PEAK}
Highest Allowable Overvoltage		V_{IOTM}	3500	V_{PEAK}
Surge Isolation Voltage	$V_{PEAK} = 10$ kV, 1.2 μs rise time, 50 μs, 50% fall time	V_{IOSM}	4000	V_{PEAK}
Safety Limiting Values	Maximum value allowed in the event of a failure (see Figure 3)			
Case Temperature		T_S	150	°C
Total Power Dissipation at 25°C		I_{S1}	1.64	W
Insulation Resistance at T_S	$V_{IO} = 500$ V	R_S	$>10^9$	Ω

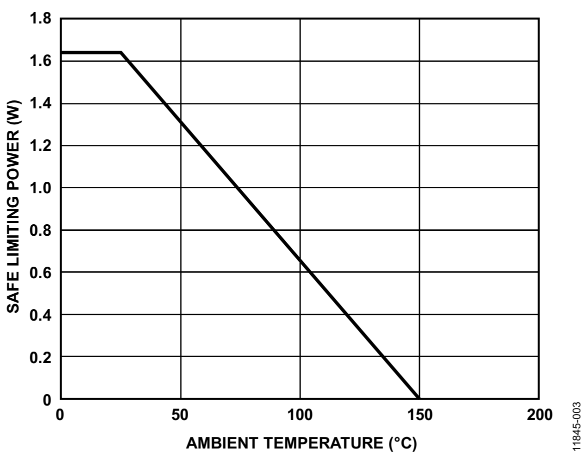


Figure 3. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per DIN V VDE V 0884-10

RECOMMENDED OPERATING CONDITIONS

Table 15.

Parameter	Symbol	Value
Operating Temperature	T_A	−40°C to +125°C
Supply Voltages[1]	V_{DD1}, V_{DD2}	2.25 V to 3.6 V
Input Signal Rise and Fall Times		1.0 ms

[1] All voltages are relative to their respective grounds. See the DC Correctness section for information on immunity to external magnetic fields.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 16.

Parameter	Rating
Supply Voltages (V_{DD1}, V_{DD2})	−0.5 V to +3.6 V
Input Voltages (V_{IA}, V_{IB})	−0.5 V to V_{DDI} + 0.5 V
Output Voltages (V_{OA}, V_{OB})	−0.5 V to V_{DD2} + 0.5 V
Average Output Current per Pin[1]	
Side 1 (I_{O1})	−10 mA to +10 mA
Side 2 (I_{O2})	−10 mA to +10 mA
Common-Mode Transients[2]	−100 kV/µs to +100 kV/µs
Storage Temperature (T_{ST}) Range	−65°C to +150°C
Ambient Operating Temperature (T_A) Range	−40°C to +125°C

[1] See Figure 3 for maximum safety power values for various temperatures.
[2] Refers to common-mode transients across the insulation barrier. Common-mode transients exceeding the absolute maximum ratings can cause latch-up or permanent damage.

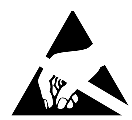
Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 17. Maximum Continuous Working Voltage[1]

Parameter	Value	Constraint
AC Voltage		
60 Hz Bipolar Waveform	565 V_{PEAK}	50-year minimum lifetime
60 Hz Unipolar Waveform		
Basic Insulation	975 V_{PEAK}	50-year minimum lifetime
DC Voltage		
Basic Insulation	975 V_{PEAK}	50-year minimum lifetime

[1] Refers to continuous voltage magnitude imposed across the isolation barrier. See the Insulation Lifetime section for more details.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

Table 18. Truth Table (Positive Logic) for all Models

V_{Ix} Input[1, 2]	V_{DDI} State[3]	V_{DDO} State[4]	EN_x Input[1]	V_{Ox} Output[1]	Description
H	Powered	Powered	L	H	Normal operation; data is high and refresh is enabled.
L	Powered	Powered	L	L	Normal operation; data is low and refresh is enabled.
H	Powered	Powered	H	H	Output is high, and refresh is disabled.
L	Powered	Powered	H	L[5]	Output is low, and refresh is disabled.
L	Unpowered	Powered	L	Default	Input unpowered. Outputs are in the default state, high for ADuM1440, ADuM1441, and ADuM1442, and low ADuM1445, ADuM1446, and ADuM1447. Outputs return to input state within 150 µs of V_{DDI} power restoration. See the pin function descriptions (Table 19 through Table 21) for more details.
L	Unpowered	Powered	H	Hold	Input unpowered. Outputs are the last state before input power is shut down.
X	Powered	Unpowered	X	Z	Output unpowered. Output pins are in high impedance state. Outputs return to input state within 34 µs of V_{DDO} power restoration. See the pin function descriptions (Table 19 through Table 21) for more details.

[1] H = high, L = low, X = don't care, and Z = high impedance.
[2] V_{Ix} and V_{Ox} refer to the input and output signals of a given channel (A, B, C, or D).
[3] V_{DDI} refers to the power supply on the input side of a given channel (A, B, C, or D).
[4] V_{DDO} refers to the power supply on the output side of a given channel (A, B, C, or D).
[5] Low input must follow a falling edge; otherwise, it can be in the default low state.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

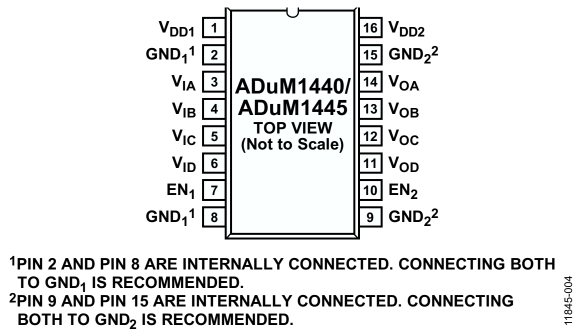


Figure 4. ADuM1440/ADuM1445 Pin Configuration

Table 19. ADuM1440/ADuM1445 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 μF to 0.1 μF range between V_{DD1} (Pin 1) and GND_1 (Pin 2).
2, 8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{ID}	Logic Input D.
7	EN_1	Refresh/Watchdog Enable 1. Connecting Pin 7 to GND_1 enables input/output refresh and watchdog functionality for Side 1, supporting standard *i*Coupler operation. Tying Pin 7 to V_{DD1} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for a detailed description of this mode. EN_1 and EN_2 must be set to the same logic state.
9, 15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
10	EN_2	Refresh/Watchdog Enable 2. Connecting Pin 10 to GND_2 enables input/output refresh and watchdog functionality for Side 2, supporting standard *i*Coupler operation. Tying Pin 10 to V_{DD2} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for a detailed description of this mode. EN_1 and EN_2 must be set to the same logic state.
11	V_{OD}	Logic Output D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 μF to 0.1 μF range between V_{DD2} (Pin 16) and GND_2 (Pin 15).

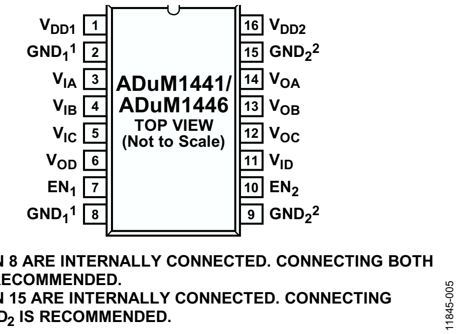


Figure 5. ADuM1441/ADuM1446 Pin Configuration

Table 20. ADuM1441/ADuM1446 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 µF to 0.1 µF range between V_{DD1} (Pin 1) and GND_1 (Pin 2).
2, 8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{IC}	Logic Input C.
6	V_{OD}	Logic Output D.
7	EN_1	Refresh/Watchdog Enable 1. Connecting Pin 7 to GND_1 enables input/output refresh and watchdog functionality for Side 1, supporting standard *i*Coupler operation. Tying Pin 7 to V_{DD1} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for a detailed description of this mode. EN_1 and EN_2 must be set to the same logic state.
9, 15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
10	EN_2	Refresh/Watchdog Enable 2. Connecting Pin 10 to GND_2 enables input/output refresh and watchdog functionality for Side 2, supporting standard *i*Coupler operation. Tying Pin 10 to V_{DD2} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for a detailed description of this mode. EN_1 and EN_2 must be set to the same logic state.
11	V_{ID}	Logic Input D.
12	V_{OC}	Logic Output C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 µF to 0.1 µF range between V_{DD2} (Pin 16) and GND_2 (Pin 15).

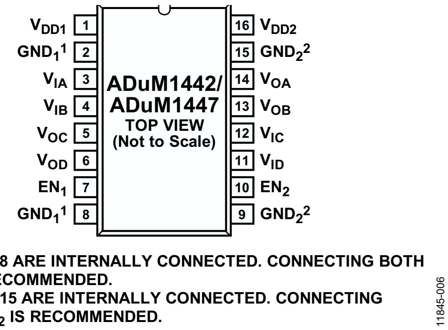


Figure 6. ADuM1442/ADuM1447 Pin Configuration

Table 21. ADuM1442/ADuM1447 Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{DD1}	Supply Voltage for Isolator Side 1 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 µF to 0.1 µF range between V_{DD1} (Pin 1) and GND_1 (Pin 2).
2, 8	GND_1	Ground 1. Ground reference for Isolator Side 1. Pin 2 and Pin 8 are internally connected, and connecting both to GND_1 is recommended.
3	V_{IA}	Logic Input A.
4	V_{IB}	Logic Input B.
5	V_{OC}	Logic Output C.
6	V_{OD}	Logic Output D.
7	EN_1	Refresh/Watchdog Enable 1. Connecting Pin 7 to GND_1 enables input/output refresh and watchdog functionality for Side 1, supporting standard *i*Coupler operation. Tying Pin 7 to V_{DD1} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for detailed description of this mode. EN_1 and EN_2 must be set to the same logic state.
9, 15	GND_2	Ground 2. Ground reference for Isolator Side 2. Pin 9 and Pin 15 are internally connected, and connecting both to GND_2 is recommended.
10	EN_2	Refresh/Watchdog Enable 2. Connecting Pin 10 to GND_2 enables input/output refresh and watchdog functionality for Side 2, supporting standard *i*Coupler operation. Tying Pin 10 to V_{DD2} disables refresh and watchdog functionality for lowest power operation, see the Applications Information section for a detailed description of this mode. EN_1 and EN_2 must be set to the same logic state.
11	V_{ID}	Logic Input D.
12	V_{IC}	Logic Input C.
13	V_{OB}	Logic Output B.
14	V_{OA}	Logic Output A.
16	V_{DD2}	Supply Voltage for Isolator Side 2 (2.25 V to 3.6 V). Connect a ceramic bypass capacitor in the 0.01 µF to 0.1 µF range between V_{DD2} (Pin 16) and GND_2 (Pin 15).

TYPICAL PERFORMANCE CHARACTERISTICS

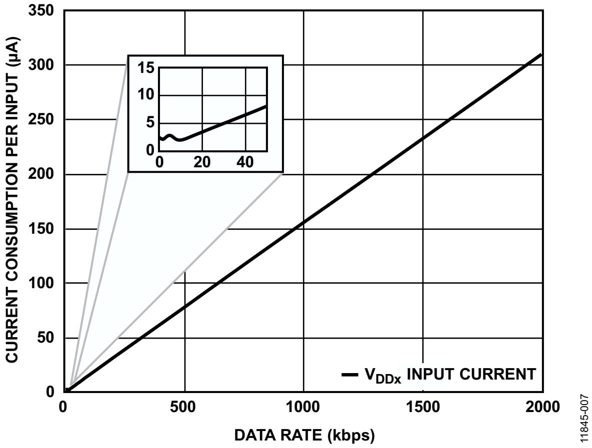


Figure 7. Current Consumption per Input vs. Data Rate for 2.5 V, EN_x = Low Operation

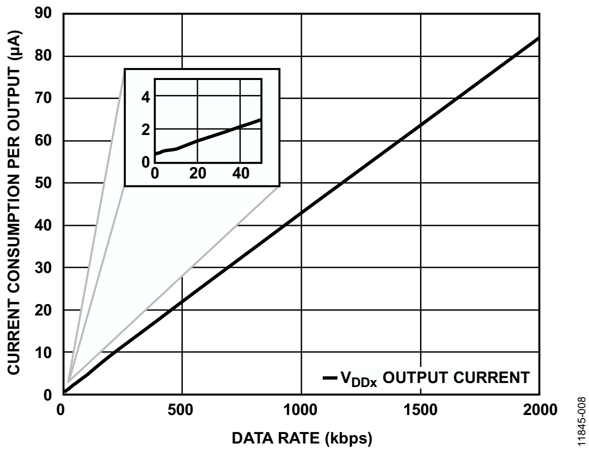


Figure 8. Current Consumption per Output vs. Data Rate for 2.5 V, EN_x = Low Operation

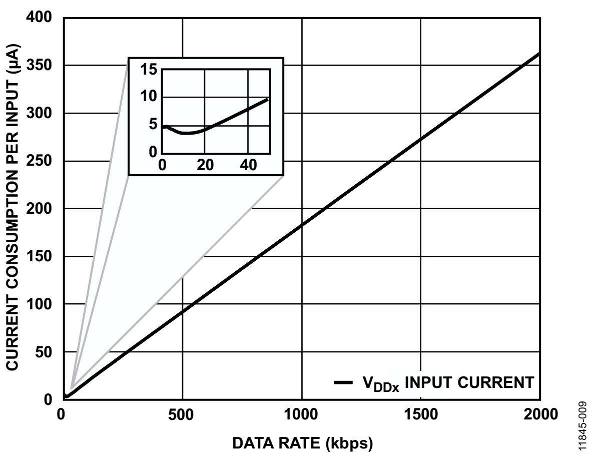


Figure 9. Current Consumption per Input vs. Data Rate for 3.3 V, EN_x = Low Operation

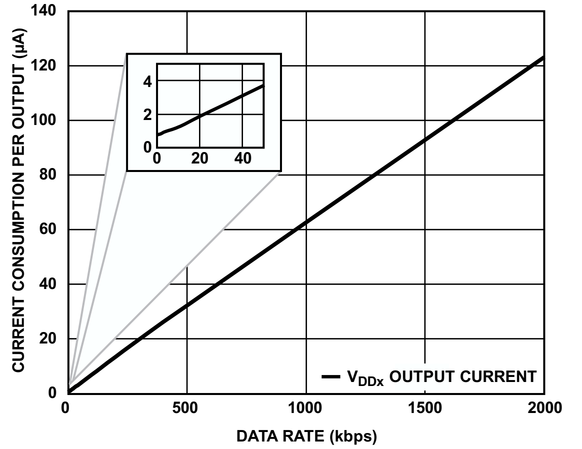


Figure 10. Current Consumption per Output vs. Data Rate for 3.3 V, EN_x = Low Operation

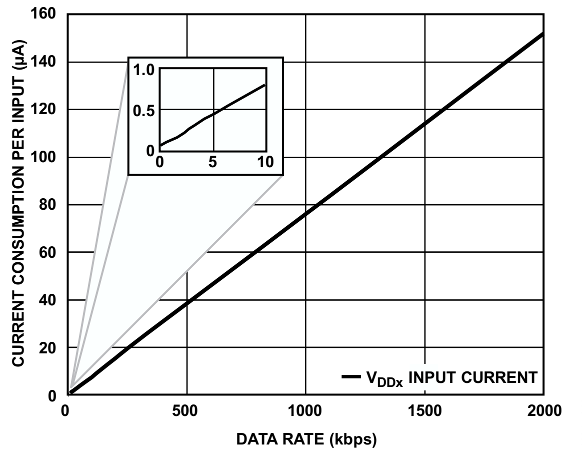


Figure 11. Current Consumption per Input vs. Data Rate for 2.5 V, EN_x = High Operation

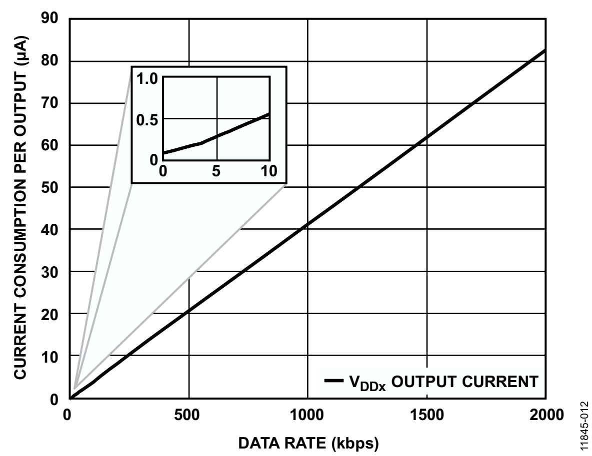


Figure 12. Current Consumption per Output vs. Data Rate for 2.5 V, EN_x = High Operation

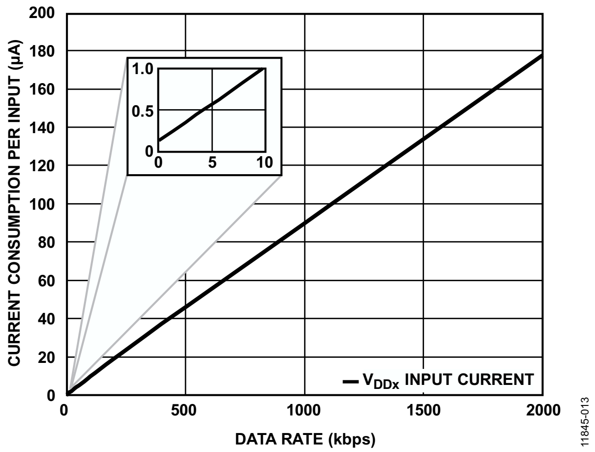


Figure 13. Current Consumption per Input vs. Data Rate for V_{DDX} = 3.3 V, EN_x = High Operation

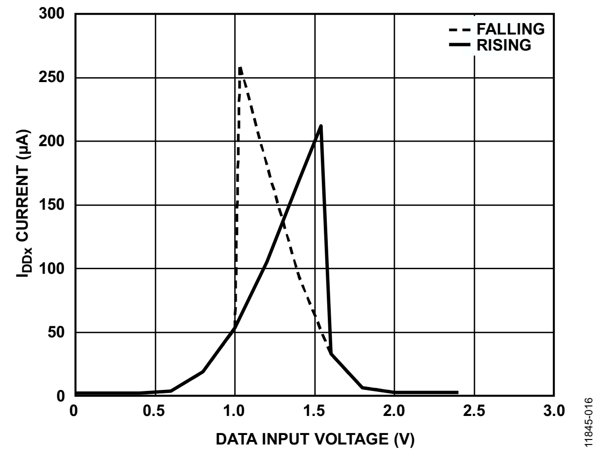


Figure 16. I_{DDx} Current per Input vs. Data Input Voltage for V_{DDx} = 2.5 V

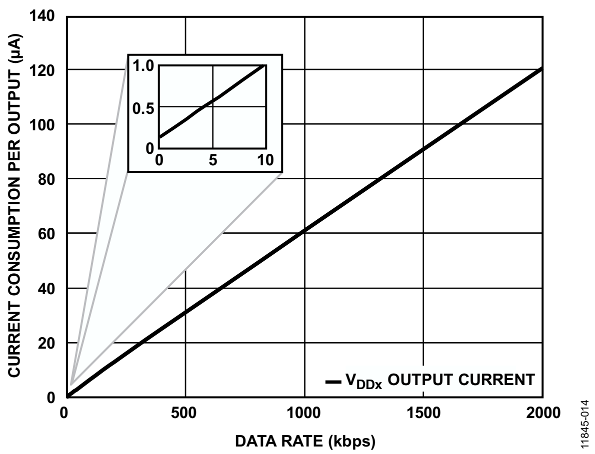


Figure 14. Current Consumption per Output vs. Data Rate for V_{DDx} = 3.3 V, EN_x = High Operation

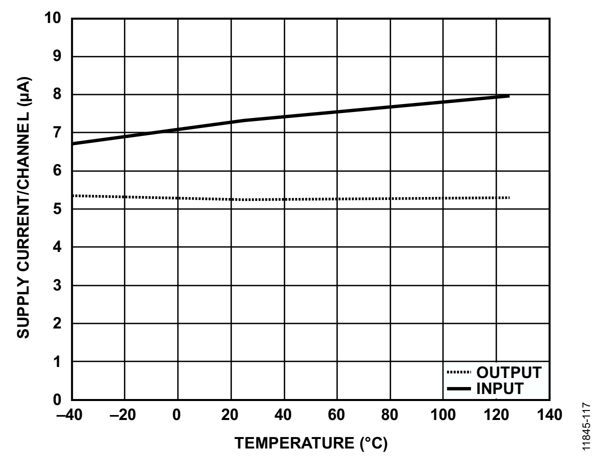


Figure 17. Typical Input and Output Supply Current per Channel vs. Temperature for V_{DDx} = 2.5 V, Data Rate = 100 kbps

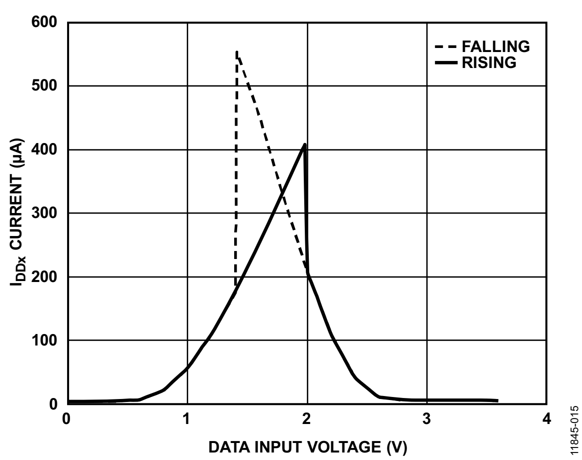


Figure 15. Typical I_{DDx} Current per Input vs. Data Input Voltage for V_{DDx} = 3.3 V

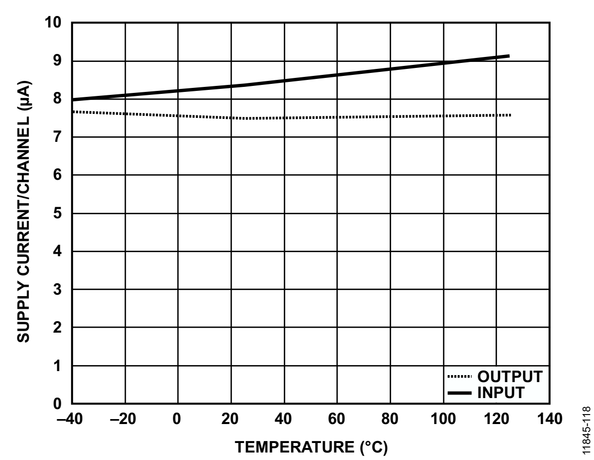


Figure 18. Typical Input and Output Supply Current per Channel vs. Temperature for V_{DDx} = 3.3 V, Data Rate = 100 kbps

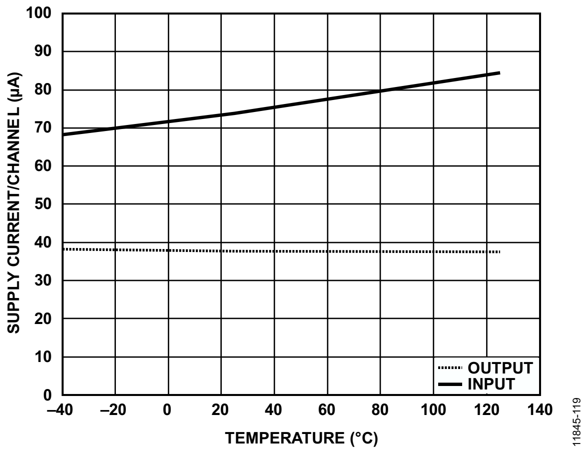


Figure 19. Typical Input and Output Supply Current per Channel vs. Temperature for V_{DDx} = 2.5 V, Data Rate = 1000 kbps

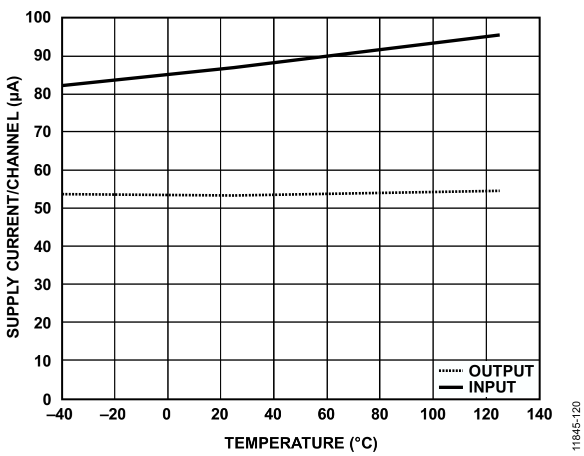


Figure 20. Typical Input and Output Supply Current per Channel vs. Temperature for V_{DDx} = 3.3 V, Data Rate = 1000 kbps

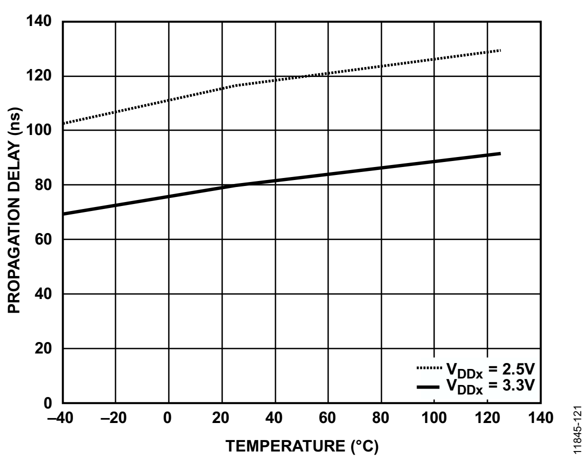


Figure 21. Typical Propagation Delay vs. Temperature for V_{DDx} = 3.3 V or V_{DDx} = 2.5 V

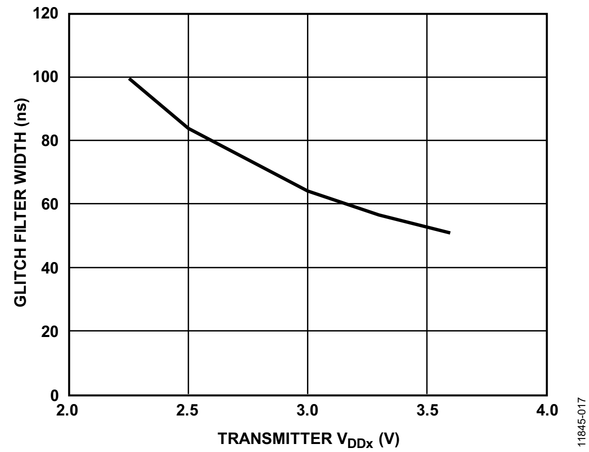


Figure 22. Typical Glitch Filter Operation Threshold

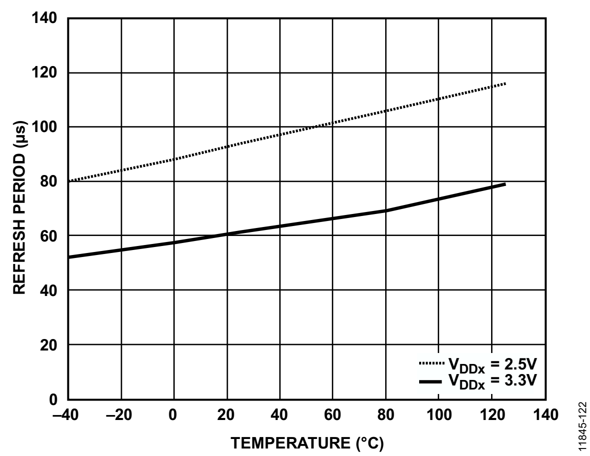


Figure 23. Typical Refresh Period vs. Temperature for 3.3 V and 2.5 V Operation

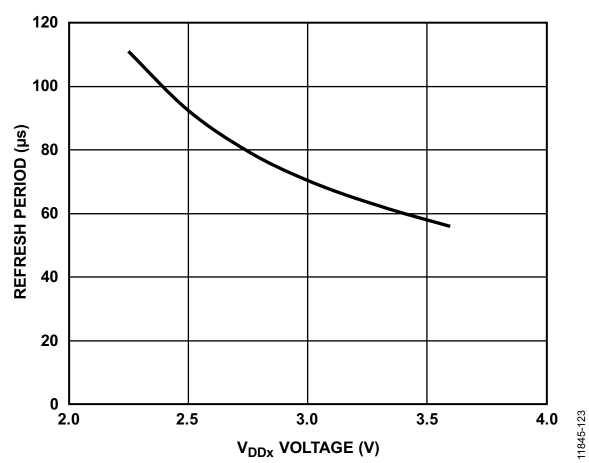


Figure 24. Typical Refresh Period vs. V_{DDX} Voltage

APPLICATIONS INFORMATION

PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 digital isolators require no external interface circuitry for the logic interfaces. Power supply bypassing is strongly recommended at both input and output supply pins: V_{DD1} and V_{DD2} (see Figure 25). Choose a capacitor value between 0.01 µF and 0.1 µF. The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm.

Using proper PCB design choices, the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 readily meets CISPR 22 Class A (and FCC Class A) emissions standards, as well as the more stringent CISPR 22 Class B (and FCC Class B) standards in an unshielded environment. Refer to the AN-1109 Application Note, *Recommendations for Control of Radiated Emissions with iCoupler Devices*, for PCB-related EMI mitigation techniques, including board layout and stack-up issues.

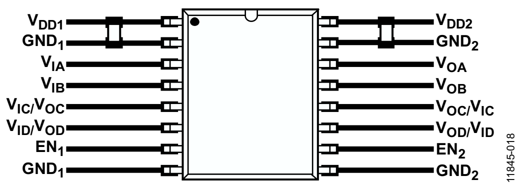


Figure 25. Recommended Printed Circuit Board Layout

For applications involving high common-mode transients, it is important to minimize board coupling across the isolation barrier. Furthermore, design the board layout so that any coupling that does occur equally affects all pins on a given component side. Failure to ensure this can cause voltage differentials between pins exceeding the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

PROPAGATION DELAY-RELATED PARAMETERS

These products are optimized for minimum power consumption by eliminating as many internal bias currents as possible. As a result, the timing characteristics are more sensitive to operating voltage and temperature than in standard *i*Coupler products. Refer to Figure 17 through Figure 24 for the expected variation of these parameters.

Propagation delay is a parameter defined as the time it takes a logic signal to propagate through a component. The input-to-output propagation delay time for a high-to-low transition can differ from the propagation delay time of a low-to-high transition.

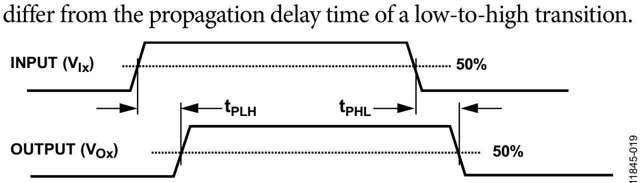


Figure 26. Propagation Delay Parameters

Pulse width distortion is the maximum difference between these two propagation delay values and an indication of how accurately the timing of the input signal is preserved.

Channel-to-channel matching is the maximum amount of time the propagation delay differs between channels within a single ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 component.

Propagation delay skew is the maximum amount of time the propagation delay differs between multiple ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 components operating under the same conditions.

In edge-based systems, it is critical to reject pulses that are too short to be handled by the encode and decode circuits. The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 implement a glitch filter to reject pulses less than the glitch filter operating threshold. This threshold depends on the operating voltage, as shown in Figure 22. Any pulse shorter than the glitch filter does not pass to the output. When the refresh circuit is enabled, pulses that match the glitch filter width have a small probability of being stretched until corrected by the next refresh cycle, or by the next valid data through that channel. To avoid issues with pulse stretching, observe the minimum pulse width requirements listed in the switching specifications.

DC CORRECTNESS

Standard Operating Mode

Positive and negative logic transitions at the isolator input cause narrow (~1 ns) pulses to be sent to the decoder using the transformer. The decoder is bistable and is, therefore, either set or reset by the pulses, indicating input logic transitions. When refresh and watchdog functions are enabled by pulling EN_1 and EN_2 low, in the absence of logic transitions at the input for more than ~140 µs, a periodic set of refresh pulses indicative of the correct input state is sent to ensure dc correctness at the output. If the decoder receives no internal pulses of more than approximately 200 µs, the input side is assumed unpowered or nonfunctional, in which case, the isolator watchdog circuit forces the output to a default state. The default state is either high as in the ADuM1440, ADuM1441, and ADuM1442 versions, or low as in the ADuM1445, ADuM1446, and ADuM1447 versions.

Low Power Operating Mode

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 allow the refresh and watchdog functions to be disabled by pulling EN_1 and EN_2 to logic high for the lowest power consumption. These control pins must be set to the same value on each side of the component for proper operation.

In this mode, the current consumption of the chip drops to the microamp range. However, be careful when using this mode because dc correctness is no longer guaranteed at startup. For example, if the following sequence of events occurs:

1. Power is applied to Side 1
2. A high level is asserted on the V_{IA} input
3. Power is applied to Side 2

The high on V_{IA} is not automatically transferred to the Side 2 V_{OA}, and there can be a level mismatch that is not corrected until a transition occurs at V_{IA}. After power is stable on each side and a transition occurs on the input of the channel, that channel's input and output state is correctly matched. This contingency can be addressed in several ways, such as sending dummy data, or toggling refresh on for a short period to force synchronization after turn on.

Recommended Input Voltage for Low Power Operation

The ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 implement Schmitt trigger input buffers so that the devices operate cleanly in low data rate or noisy environments. Schmitt triggers allow a small amount of shoot through current when their input voltage is not approximate to either V_{DDx} or GND_x levels. This is because the two transistors are both slightly on when input voltages are in the middle of the supply range. For many digital devices, this leakage is not a large portion of the total supply current and may not be noticed; however, in the ultralow power ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447, this leakage can be larger than the total operating current of the device and cannot be ignored.

To achieve optimum power consumption with the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447, always drive the inputs as near to V_{DDx} or GND_x levels as possible. Figure 15 and Figure 16 illustrate the shoot through leakage of an input; therefore, whereas the logic thresholds of the input are standard CMOS levels, optimum power performance is achieved when the input logic levels are driven within 0.5 V of either V_{DDx} or GND_x levels.

MAGNETIC FIELD IMMUNITY

The magnetic field immunity of the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 is determined by the changing magnetic field, which induces a voltage in the receiving coil of the transformer large enough to either falsely set or reset the decoder. The following analysis defines the conditions under which this can occur. The 3.3 V operating condition of the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 is examined because it represents the most typical mode of operation.

The pulses at the transformer output have an amplitude greater than 1.0 V. The decoder has a sensing threshold at about 0.5 V, thus establishing a 0.5 V margin in which induced voltages can be tolerated. The voltage induced across the receiving coil is given by

$$V = (-d\beta/dt) \sum \pi r_n^2;\ n = 1, 2, \ldots, N$$

where:
β is magnetic flux density (gauss).
r_n is the radius of the n[th] turn in the receiving coil (cm).
N is the number of turns in the receiving coil.

Given the geometry of the receiving coil in the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 and an imposed requirement that the induced voltage be, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field at a given frequency can be calculated. The result is shown in Figure 27.

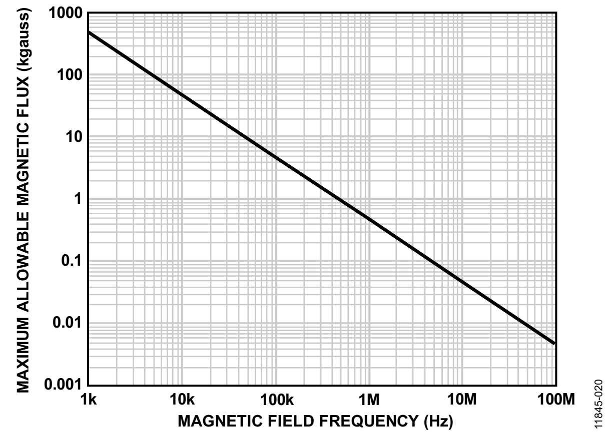


Figure 27. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.5 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurred during a transmitted pulse (and was of the worst-case polarity), it would reduce the received pulse from >1.0 V to 0.75 V, still well above the 0.5 V sensing threshold of the decoder.

The preceding magnetic flux density values correspond to specific current magnitudes at given distances from the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 transformers. Figure 28 shows these allowable current magnitudes as a function of frequency for selected distances. As shown, the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 are extremely immune and can be affected only by extremely large currents operating at a high frequency very near to the component. For the 1 MHz example noted previously, a 1.2 kA current would have to be placed 5 mm away from the ADuM1440/ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 to affect the operation of the component.

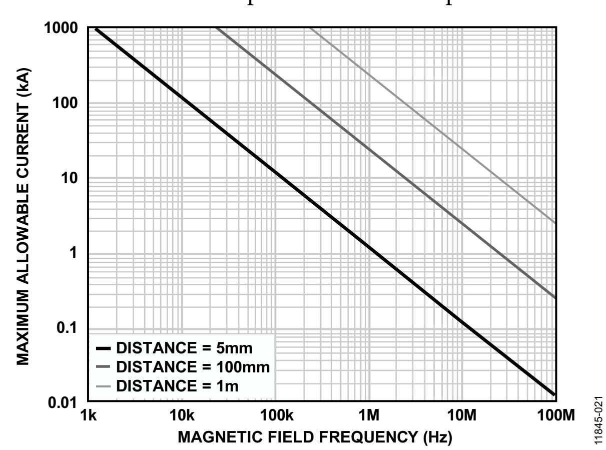


Figure 28. Maximum Allowable Current for Various Current-to-ADuM144x Spacings

Note that at combinations of strong magnetic field and high frequency, any loops formed by PCB traces can induce error voltages sufficiently large enough to trigger the thresholds of succeeding circuitry. Take care in the layout of such traces to avoid this possibility.

POWER CONSUMPTION

The supply current at a given channel of the ADuM1440/ ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447 isolator is a function of the supply voltage, the data rate of the channel, and the output load of the channel.

For each input channel, the supply current is given by

$$I_{DDI} = I_{DDI\,(Q)} \qquad f \le 0.5\,f_r$$

$$I_{DDI} = I_{DDI\,(D)} \times (2f - f_r) + I_{DDI\,(Q)} \qquad f > 0.5\,f_r$$

For each output channel, the supply current is given by

$$I_{DDO} = I_{DDO\,(Q)} \qquad f \le 0.5\,f_r$$

$$I_{DDO} = (I_{DDO\,(D)} + (0.5 \times 10^{-3}) \times C_L \times V_{DDO}) \times (2f - f_r) + I_{DDO\,(Q)} \qquad f > 0.5\,f_r$$

where:

$I_{DDI\,(D)}$, $I_{DDO\,(D)}$ are the input and output dynamic supply currents per channel (mA/Mbps).
$I_{DDI\,(Q)}$, $I_{DDO\,(Q)}$ are the specified input and output quiescent supply currents (mA).
f is the input logic signal frequency (MHz); it is half the input data rate, expressed in units of Mbps.
f_r is the input stage refresh rate (Mbps).
C_L is the output load capacitance (pF).
V_{DDO} is the output supply voltage (V).

To calculate the total V_{DD1} and V_{DD2} supply current, the supply currents for each input and output channel corresponding to V_{DD1} and V_{DD2} are calculated and totaled. Figure 7 through Figure 14 show per channel supply currents as a function of data rate for an unloaded output condition.

INSULATION LIFETIME

All insulation structures eventually break down when subjected to voltage stress over a sufficiently long period. The rate of insulation degradation is dependent on the characteristics of the voltage waveform applied across the insulation. In addition to the testing performed by the regulatory agencies, Analog Devices carries out an extensive set of evaluations to determine the lifetime of the insulation structure within the ADuM1440/ ADuM1441/ADuM1442/ADuM1445/ADuM1446/ADuM1447.

Analog Devices performs accelerated life testing using voltage levels higher than the rated continuous working voltage. Acceleration factors for several operating conditions are determined. These factors allow calculation of the time to failure at the actual working voltage. The values shown in Table 17 summarize the peak voltage for 50 years of service life for a bipolar ac operating condition and the maximum CSA approved working voltages. In many cases, the approved working voltage is higher than the 50-year service life voltage. Operation at these high working voltages can lead to shortened insulation life, in some cases.

The insulation lifetime of the ADuM1440/ADuM1441/ ADuM1442/ADuM1445/ADuM1446/ADuM1447 depends on the voltage waveform type imposed across the isolation barrier. The *i*Coupler insulation structure degrades at different rates depending on whether the waveform is bipolar ac, unipolar ac, or dc. Figure 29, Figure 30, and Figure 31 illustrate these different isolation voltage waveforms.

Bipolar ac voltage is the most stringent environment. The goal of a 50-year operating lifetime under the ac bipolar condition determines the Analog Devices recommended maximum working voltage.

In the case of unipolar ac or dc voltage, the stress on the insulation is significantly lower. This allows operation at higher working voltages while still achieving a 50-year service life. The working voltages listed in Table 17 can be applied while maintaining the 50-year minimum lifetime provided the voltage conforms to either the unipolar ac or dc voltage case. Treat any cross-insulation voltage waveform that does not conform to Figure 30 or Figure 31 as a bipolar ac waveform, and limit its peak voltage to the 50-year lifetime voltage value listed in Table 17.

Note that the voltage presented in Figure 30 is shown as sinusoidal for illustration purposes only. It is meant to represent any voltage waveform varying between 0 V and some limiting value. The limiting value can be positive or negative, but the voltage cannot cross 0 V.

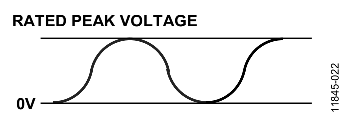


Figure 29. Bipolar AC Waveform

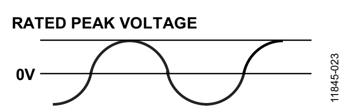


Figure 30. Unipolar AC Waveform

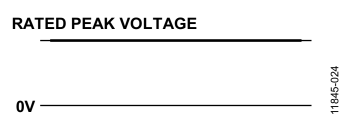


Figure 31. DC Waveform

OUTLINE DIMENSIONS

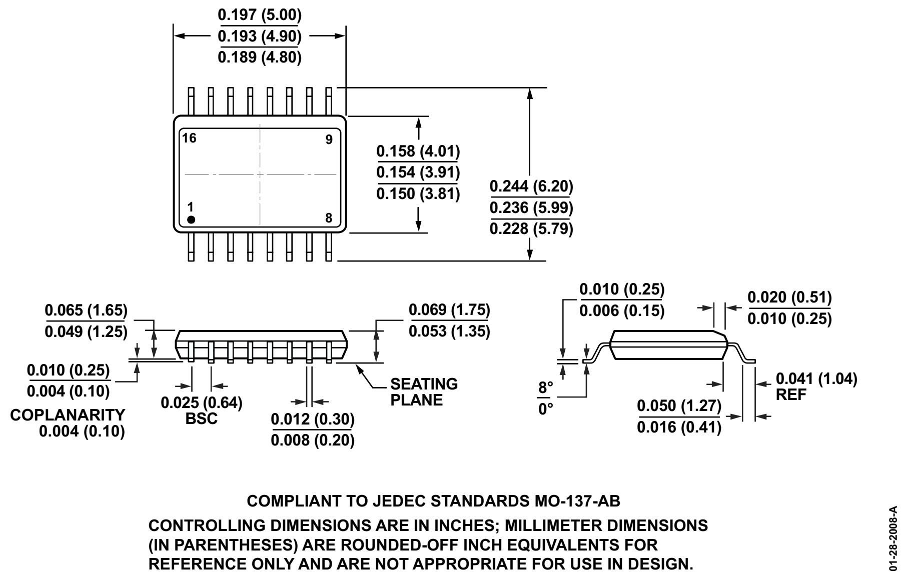


Figure 32. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
(Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model[1, 2]	Number of Inputs, V_{DD1} Side	Number of Inputs, V_{DD2} Side	Maximum Data Rate (Mbps)	Default Output State	Maximum Propagation Delay, 3.3 V (ns)	Temperature Range	Package Description	Package Option
ADuM1440ARQZ	4	0	2	High	180	−40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1441ARQZ	3	1	2	High	180	−40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1442ARQZ	2	2	2	High	180	−40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1445ARQZ	4	0	2	Low	180	−40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1446ARQZ	3	1	2	Low	180	−40°C to +125°C	16-Lead QSOP	RQ-16
ADuM1447ARQZ	2	2	2	Low	180	−40°C to +125°C	16-Lead QSOP	RQ-16

[1] Z = RoHS Compliant Part.
[2] Tape and reel is available. The addition of the –RL7 suffix indicates that the product is shipped on 7” tape and reel.

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