AN3008
Application note

STOD2540, single inductor DC-DC converter generates multiple supply voltages for E-paper display

Introduction

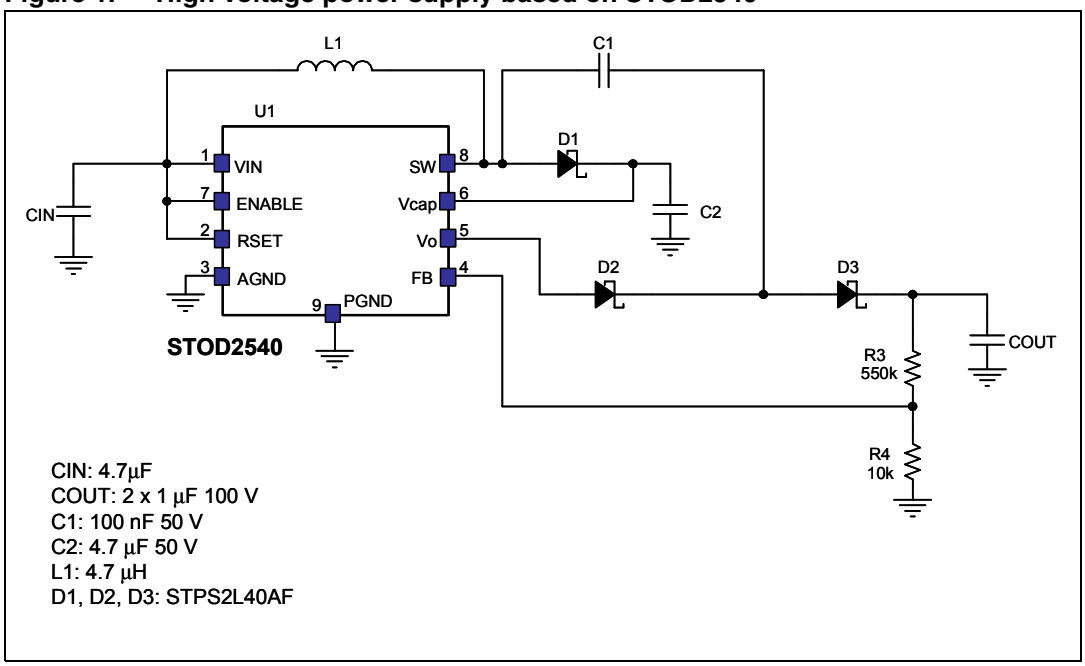
This application note describes how to use the STOD2540 DC-DC converter to generate two output voltages using a single inductor and an external charge pump. The circuit shown in *Figure 1* generates a 70 V output from a 3.7 V input voltage.

The STOD2540 is a highly integrated boost converter that can provide an adjustable output up to 35 V from a 3.0 to 5.5 V input voltage.

The STOD2540 operates in PFM (pulsed frequency modulation) mode. PFM control simply means that the part only switches when the charge needs to be delivered to the output in order to keep the output voltage regulated.

The converter is ideal for generating the necessary voltages to supply thin-film transistor (TFT) LCDs, OLEDs and E-paper shelf labels. The low operating supply current makes the device ideal for small, portable, battery supplied applications. In shutdown mode the load is disconnected from the input and the quiescent current is less than 3 µA.

Figure 1. High voltage power supply based on STOD2540



Contents

1 High voltage power supply based on STOD2540

1.1 STOD2540 function description

The STOD2540 uses a PFM control scheme to reach high efficiency in low load conditions. The DC-DC has a current mode control scheme that uses a minimum OFF time and a maximum ON time.

The converter monitors the output voltage through the resistor dividers R1 and R2 by comparing the feedback voltage with the internal reference voltage of 1.24 V.

The integrated main power switch is turned on as soon as the feedback voltage falls below the internal reference. The switch stays on until the inductor current reaches the peak current limit or for a maximum ON time equal to 5.5 µsec. The peak current limit value is adjustable through an external resistor connected between the RSET pin and GND. The main switch stays off for at least a minimum OFF time (300 ns typical) and remains in the off state for as long as the feedback voltage remains above the internal reference voltage.

During the ON time, the load current is only supplied by the charge stored in the output capacitor until the feedback voltage drops below the reference voltage again.

PFM regulation is particularly useful when output currents are low and the part is prevalently in the OFF state.

1.2 Load disconnect

When the device is in shutdown mode, a DC current path exists between the power source and the load. A high-side switch LDS isolates the load from the source when the device is disabled.

1.3 Output adjust

Choose the R4 value in the range of 10 to 200 kΩ. The value of R3 can be calculated from the following equation.

Equation 1

$$R_U = R_L \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

Where

R_U is the upper resistor of the voltage divider.

R_L is the lower resistor of the voltage divider.

1% tolerance resistors should be chosen for a more accurate V_{OUT}.

The STOD2540 shows a pulses burst behavior that causes a high output voltage ripple. To decrease the output ripple it is possible to insert a capacitor across the upper feedback resistor. The following formula can be used to obtain a first estimation of the value of the capacitor.

Equation 2

$$CF = \frac{1}{2 \times \pi \times \frac{F_{SW}}{20} \times R_U}$$

Where

R_U is the upper resistor of the voltage divider.

F_{SW} is the switching frequency.

The following equation gives the switching frequency at the nominal load current.

Equation 3

$$F_{SW}(I_{LOAD}) = \frac{2 \times I_{LOAD} \times (V_{OUT} - V_{IN})}{L \times I_{PK}^{2}}$$

The CF capacitor increases the amplitude of the voltage ripple on the FB pin, causing a deterioration of the line regulation; therefore, the value of CF should be as small as possible.

1.4 Inductor selection

Since the hysteretic control scheme is inherently stable, the inductor value does not affect the stability of the regulator. Using the PFM peak current control scheme, the converter operates in discontinuous conduction mode (DCM).

The inductance value must be calculated so as to ensure that the inductor current reaches the current limit before the maximum ON time expires. The following equation can be used to calculate the maximum value of the inductance.

Equation 4

$$L \leq \frac{V_{IN\_MIN}}{I_{PK}} \times T_{ON\_MAX}$$

Where I_{PK} is the controlled inductor peak current.

In this case the maximum value of the load current is given by *Equation 5*.

Equation 5

$$I_{LOAD\_MAX} = \frac{I_{PK}^{2} \times L}{2 \times (V_{OUT} + Vd - V_{IN}) \times \left(\frac{I_{PK} \times L}{V_{IN}} + toff_{MIN} \right)}$$

1.5 C_{OUT} selection

The output voltage ripple very much depends on the application conditions. The output capacitor has a significant effect on the output voltage ripple magnitude because it supplies the load current through the charge stored during the ON state.

The output voltage ripple consists of two parts: the first is caused by the ESR, the second by the charging and discharging process of the output capacitor.

The output ripple can be approximately given by the following equation.

Equation 6

$$\Delta V_{OUT} = \frac{I_{OUT}}{C_{OUT}} \times \left(\frac{1}{F_{SW}} - \frac{I_{PK} \times L}{V_{OUT} + V_D - V_{IN}} \right)$$

The magnitude of the ripple will typically be linearly proportional to the output capacitance present. For the best output voltage filtering, a low ESR output capacitor is recommended.

1.6 Diode selection

The output diode in a boost converter conducts current only when the power switch is off. The average current is equal to the output current and the maximum current is equal to the peak inductor current.

To maximize efficiency, we recommend using a Schottky diode characterized by:

1. a small forward voltage drop.
2. a rated current larger than the peak inductor current.
3. a reverse voltage larger than the output voltage.
4. a small reverse leakage current.

1.7 Single inductor circuit based on STOD2540 derives 35 V/70 V

The circuit shown in *Figure 2* is capable of deriving +35 / +70 V from a [3; 5.5] input voltage range. The STOD2540 DC-DC converter generates the 35 V output voltage. The addition of an external charge pump consisting of two Schottky diodes (D2 and D3) and two capacitors (C1 and C2) allows delivering output voltages of over 70 V.

In steady-state operation, the voltage on C2 is 35 V and the voltage on C_{OUT} is 70 V. During the ON time the main switch is closed and the current flows from the input to ground through L1 and the internal switch. During this time, the voltage at node SW is 0 V and C1 is charged up to 35 V. In these conditions, D1 is reverse-biased, D2 is forward-biased, D3 is reverse-biased and the load current is supplied only by the output capacitor C_{OUT}.

Figure 2. External charge pump - T_{ON} state

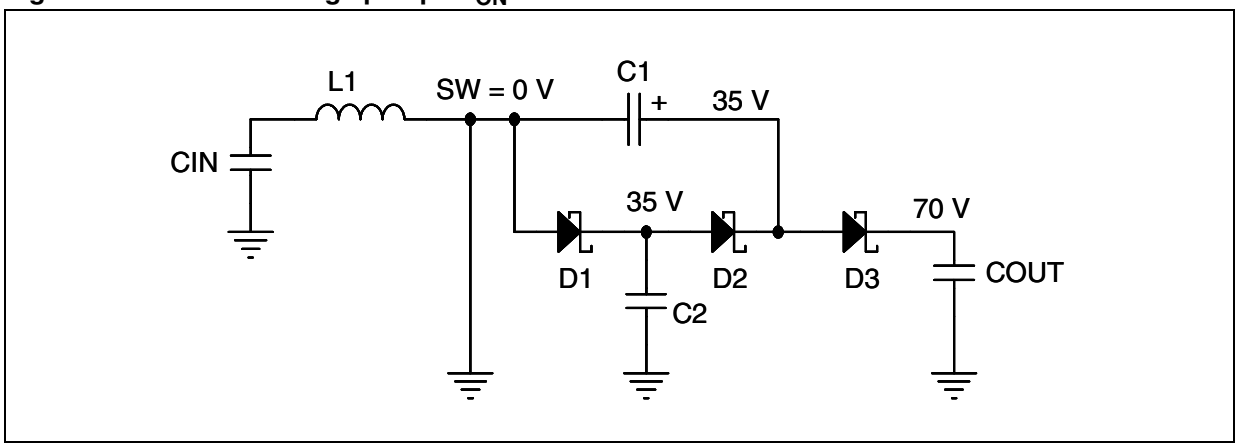
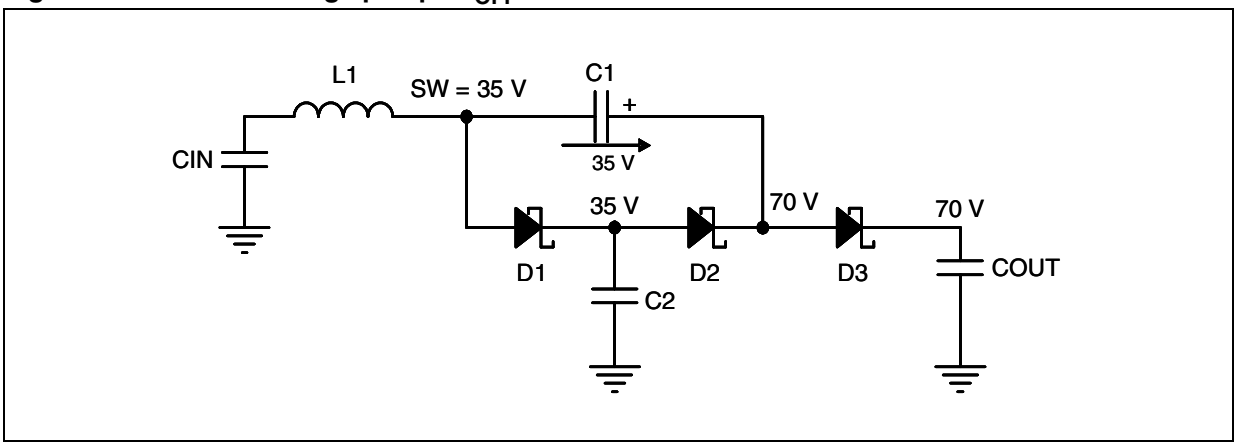


Figure 3. External charge pump - T_{OFF} state



When the power switch is opened, D1 is forward-biased and current flows through L1 and D1 into C2. Therefore, the voltage at node SW is equal to the voltage on C2 (35 V).

C1, which was previously charged to 35 V, is now referenced to node 35 V. The voltage across C1 remains at 35 V, but the left side is 35 V with respect to ground and the right side is 70 V with respect to ground. D3 becomes forward-biased and C_{OUT} is charged to 70 V. D2 is reverse-biased during this time period.

The output is regulated to 70 V through the feedback divider that goes back to the FB pin of the STOD2540. An unregulated output voltage of 35 V is available from the C2 output capacitor in this configuration. Since the 35 V output voltage is not regulated, it is not stable like the 70 V output voltage and varies with the current drawn from the 70 V.

If desired, the feedback can be recalculated for a 35 V output. This provides a regulated 35 V output and an unregulated 70 V output.

D1, D2 and D3 must be rated for at least half the higher output voltage. The peak current ratings for the diodes must be greater than half the peak switch current of the STOD2540. C2 and C3 must have voltage ratings greater than half the output voltage, while C4 must be rated for the full output voltage.

2 Test results

2.1 Start-up

Figure 4 and *Figure 5* show the output voltage and inductor current waveforms of the evaluation module in the following conditions.

- V_{IN} = 3.7 V
- V_{OUT} = 73 V
- I_{LOAD} = 5 mA

Figure 4. Start-up/V_{OUT}

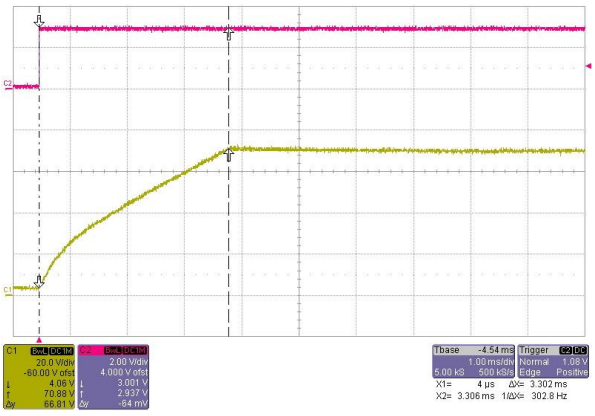
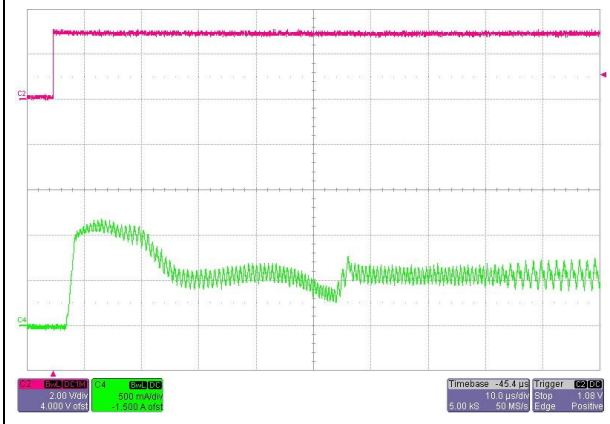


Figure 5. Start-up/inductor current



2.2 Output voltage ripple

The traces in *Figure 6* and *Figure 7* show the output voltage ripple on a 70 V output with different input voltages and I_{LOAD} equal to 10 mA.

Figure 6. 70 V output voltage ripple vs. V_{IN}

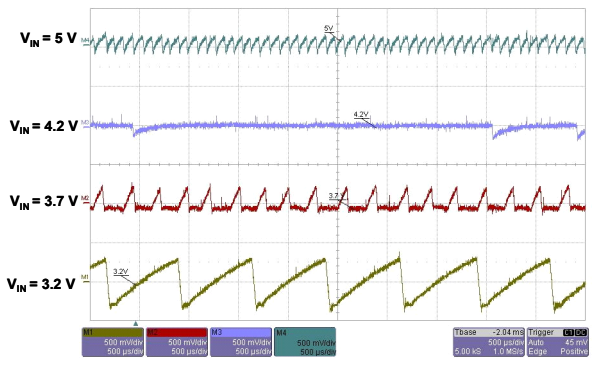
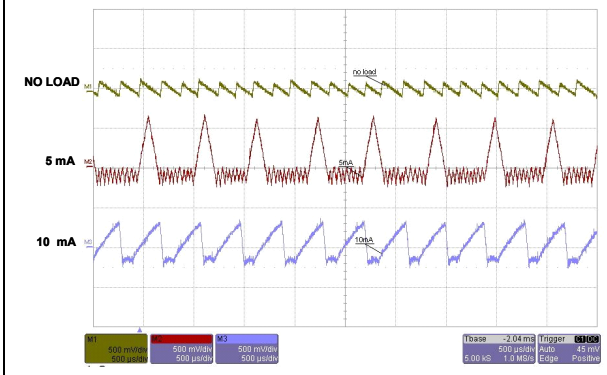
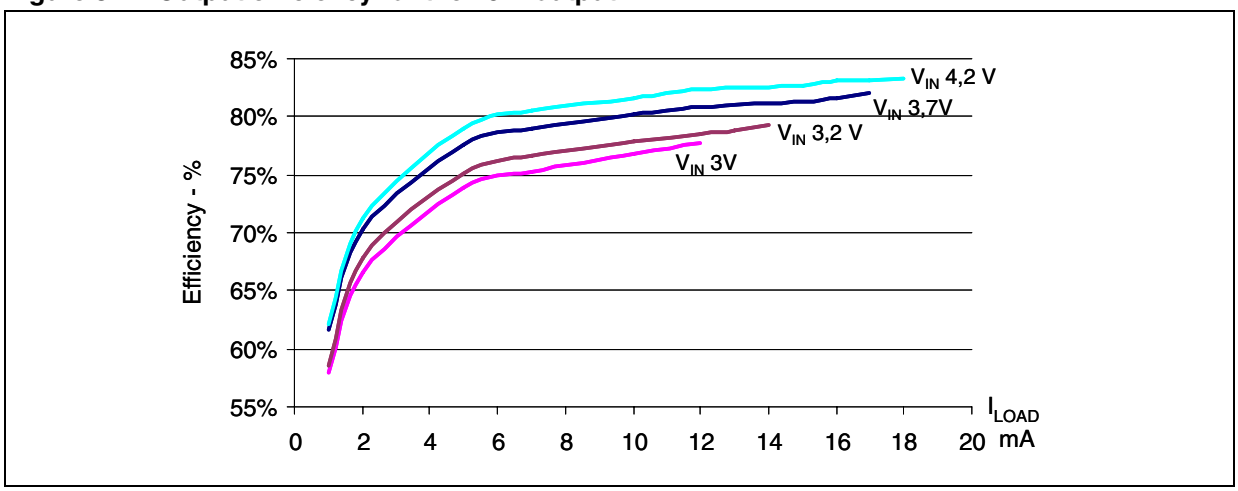


Figure 7. 70 V output voltage ripple vs. I_{LOAD}



2.3 Efficiency

Figure 8. Output efficiency for the 70 V output



2.4 Line regulation 70 V / 35 V

Figure 9. 70 V line regulation

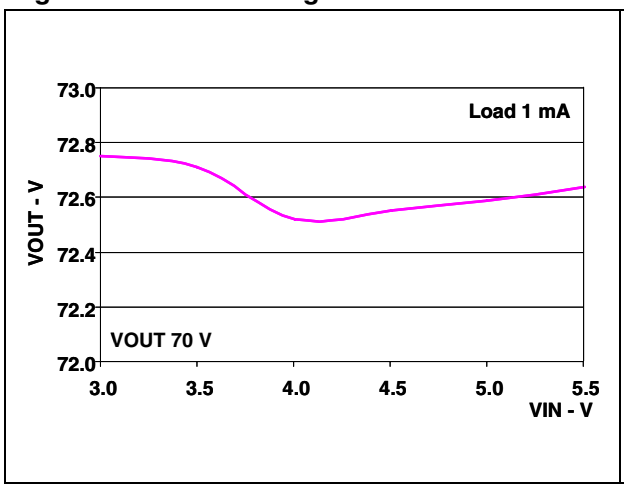
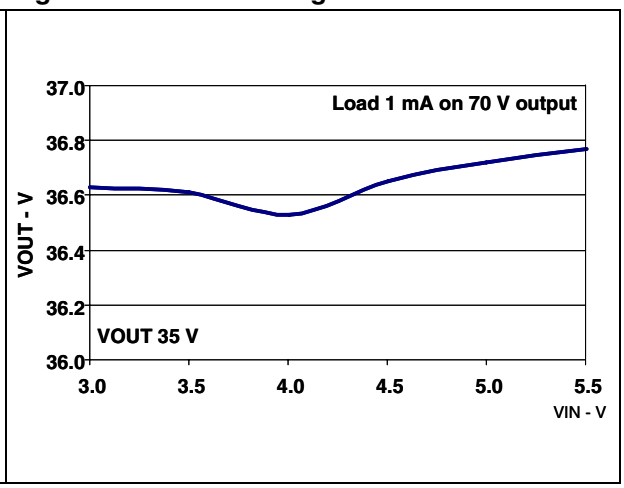


Figure 10. 35 V line regulation



2.5 Load regulation

Figure 11. 70 V output load regulation

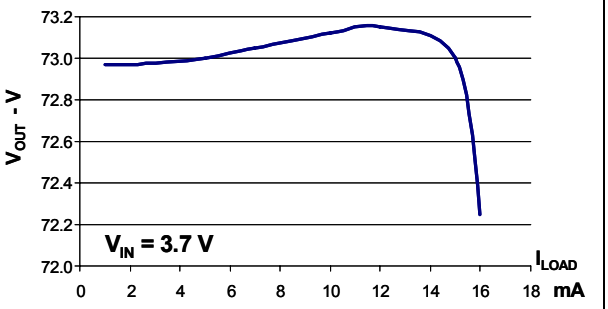


Figure 12. 35 V output changes when load current is drowned from the 70 V

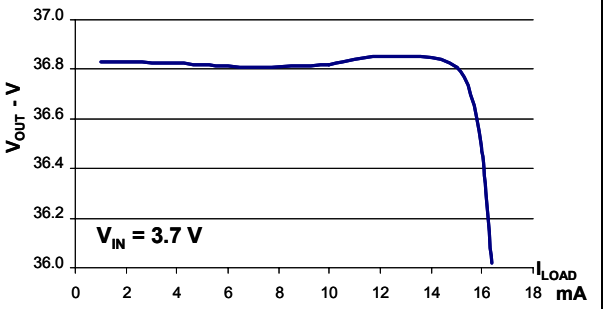
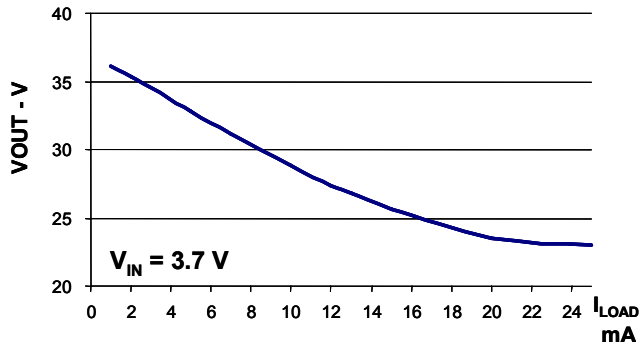


Figure 13 shows the behavior of the 35 V output when the load current is drowned from 35 V and the FB pin is closed on 70 V.

Figure 13. 35 V unregulated output



3 Layout

To minimize the occurrence of problems related to noise and duty cycle jitter, attention has been given to the routing of high-frequency current loops. It is essential to keep the high switching current circulating paths as small as possible. In general the following rules should be applied.

- The GND connections of the COUT, CIN capacitors and STOD2540 PGND should be placed as close as possible to each other.
- The connection from the IC pins (VIN, SW) and the inductor must be kept short.
- CIN should be placed close to the VIN pin of the chip.
- The ground area should be as large as possible. If a two-layer PCB is used, one layer should be assigned as the ground layer and a good connectivity between both layers should be observed.

Figure 14. Assembly layer

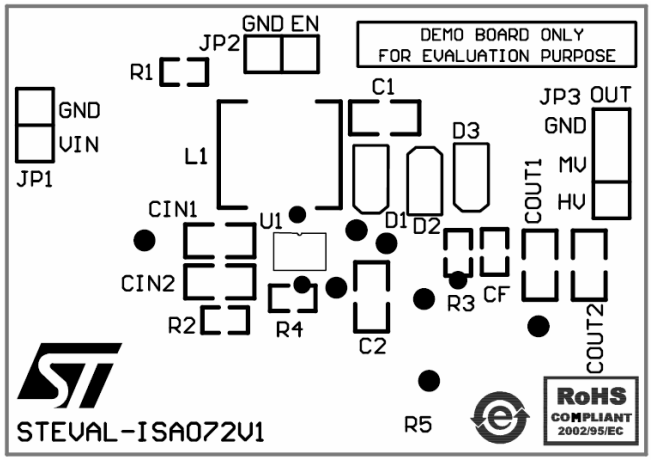


Figure 15. Top layer

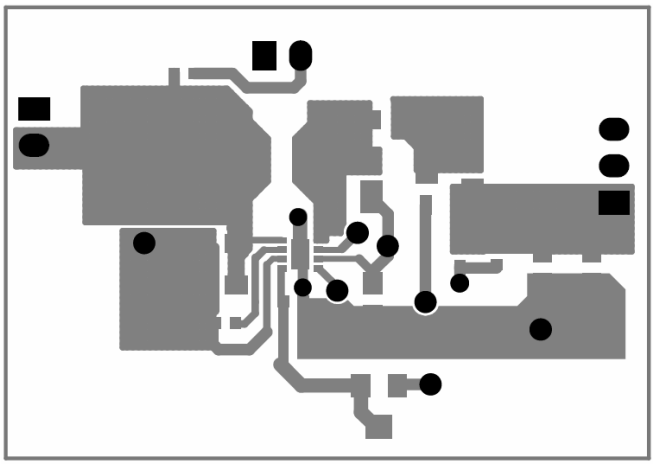
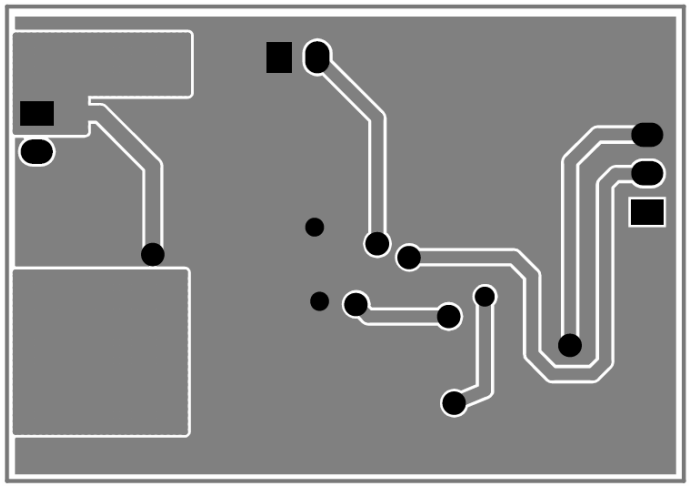


Figure 16. Bottom layer



3.1 Input / output connections

Table 1. Input / output connections

Reference designator	Name	Description
JP1	VIN/GND	VIN: positive connection to the input power supply. GND: return connection to the input power supply.
JP2	En	Use this connector to enable and disable the DC-DC converter. Connect the EN pin to GND to disable the converter. If the EN pin is left floating, the EVM operates correctly.
JP3	V_{OUT}	HV: high voltage – 70 V. Positive connection for the load. MV: medium voltage – 35 V. Positive connection for the load. GND: return pin for the load.

4 Application schematic and bill of materials

Figure 17. Demonstration board schematic

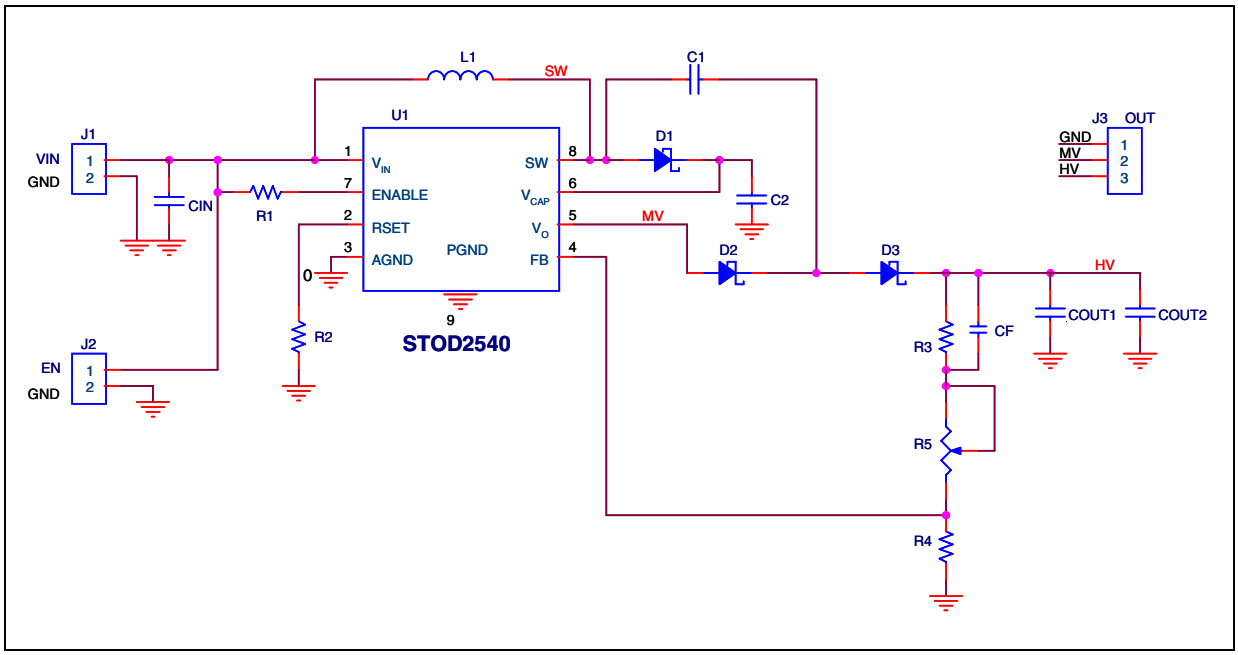


Table 2. Bill of materials

Quantity	Reference	Description	Part/Value	PCB Footprint
1	U1	DC-DC converter	STOD2540PMR	QFN8 3 x 3 mm
1	CIN	Capacitor, ceramic, 4.7 µF, 16 V, X5R		0805
1	C1	Capacitor, ceramic, 100 nF, 50 V, X5R		0805
2	COUT	Capacitor, ceramic, 1 µF, 100 V, X5R	GRM31CR72A105KA01L	0805
1	CF	Capacitor, ceramic, 47 pF		0603
1	L1	Inductor, 4.7 µH	LPS3314-472MLC	
3	D1, D2, D3	Diode, Schottky 2 A 30 V	STPS2L40AF	SMAflat
1	R1	Resistor, 1 kΩ, 1/16 W, 1%		0603
1	R2	Resistor, 1/16 W, 1%		0603
1	R3	Resistor, 680 kΩ, 1/16 W, 1%		0603
1	R4	Resistor, 10 kΩ, 1/16 W, 1%		0603
1	R5	Potentiometer, 100 kΩ		
2	JP1, JP2	Header, 2-pin, 100-mil spacing		
1	JP3	Header, 3-pin, 100-mil spacing		

5 Revision history

Table 3. Document revision history

Date	Revision	Changes
10-Nov-2009	1	Initial release.
08-Jan-2010	2	Modified: *Figure 14 on page 10*, *Figure 15 on page 10*, *Figure 16 on page 11*, *Figure 17* and *Table 2 on page 12*.