



September 2010

# FDMS3604S

## Dual N-Channel PowerTrench<sup>®</sup> MOSFET

N-Channel: 30 V, 30 A, 6.8 mΩ N-Channel: 30 V, 40 A, 2.6 mΩ

### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 6.8 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 13 A
- Max  $r_{DS(on)}$  = 9.8 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 11 A

Q2: N-Channel

- Max  $r_{DS(on)}$  = 2.6 mΩ at  $V_{GS}$  = 10 V,  $I_D$  = 23 A
- Max  $r_{DS(on)}$  = 3.5 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 21 A
- Low inductance packaging shortens rise/fall times, resulting in lower switching losses
- MOSFET integration enables optimum layout for lower circuit inductance and reduced switch node ringing
- RoHS Compliant

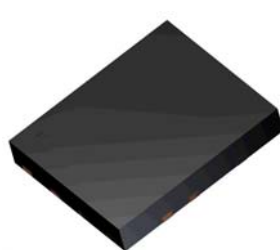


### General Description

This device includes two specialized N-Channel MOSFETs in a dual PQFN package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

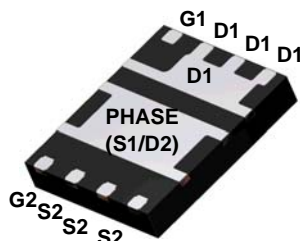
### Applications

- Computing
- Communications
- General Purpose Point of Load
- Notebook VCORE

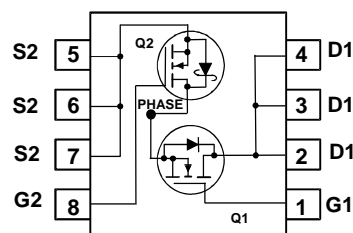


Top

Power 56



Bottom



### MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
$V_{DS}$	Drain to Source Voltage	30	30	V
$V_{GS}$	Gate to Source Voltage (Note 3)	$\pm 20$	$\pm 20$	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25^\circ\text{C}$	30	40	A
	-Continuous (Silicon limited) $T_C = 25^\circ\text{C}$	60	130	
	-Continuous $T_A = 25^\circ\text{C}$	13 <sup>1a</sup>	23 <sup>1b</sup>	
	-Pulsed	40	100	
$E_{AS}$	Single Pulse Avalanche Energy	40 <sup>4</sup>	112 <sup>5</sup>	mJ
$P_D$	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	2.2 <sup>1a</sup>	2.5 <sup>1b</sup>	W
	Power Dissipation for Single Operation $T_A = 25^\circ\text{C}$	1.0 <sup>1c</sup>	1.0 <sup>1d</sup>	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

### Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	57 <sup>1a</sup>	50 <sup>1b</sup>	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	125 <sup>1c</sup>	120 <sup>1d</sup>	
$R_{\theta JC}$	Thermal Resistance, Junction to Case	3.5	2	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
22CA N7CC	FDMS3604S	Power 56	13 "	12 mm	3000 units

**Electrical Characteristics**  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
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**Off Characteristics**

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$ $I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	Q1 Q2	30 30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$ $I_D = 10\text{ mA}$ , referenced to $25\text{ }^{\circ}\text{C}$	Q1 Q2		15 12		mV/ $^{\circ}\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$	Q1 Q2			1 500	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$	Q1 Q2			100 100	nA nA

**On Characteristics**

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$ $V_{GS} = V_{DS}$ , $I_D = 1\text{ mA}$	Q1 Q2	1.1 1.1	2 1.8	2.7 3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^{\circ}\text{C}$ $I_D = 10\text{ mA}$ , referenced to $25\text{ }^{\circ}\text{C}$	Q1 Q2		-6 -5		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 13\text{ A}$	Q1		5.2 7.5	6.8 9.8	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 11\text{ A}$			6.2	9.2	
		$V_{GS} = 10\text{ V}$ , $I_D = 13\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$	Q2		2 2.6	2.6 3.5	
		$V_{GS} = 4.5\text{ V}$ , $I_D = 21\text{ A}$ $V_{GS} = 10\text{ V}$ , $I_D = 23\text{ A}$ , $T_J = 125\text{ }^{\circ}\text{C}$			2.6	4	
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}$ , $I_D = 13\text{ A}$	Q1		61		S
		$V_{DS} = 5\text{ V}$ , $I_D = 23\text{ A}$	Q2		130		

**Dynamic Characteristics**

$C_{iss}$	Input Capacitance	Q1: $V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		1340 3240	1785 4310	pF
$C_{oss}$	Output Capacitance	Q2: $V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ , $f = 1\text{ MHz}$	Q1 Q2		485 1230	645 1635	pF
$C_{rss}$	Reverse Transfer Capacitance		Q1 Q2		53 103	80 155	pF
$R_g$	Gate Resistance		Q1	0.2	0.6	2.0	$\Omega$
			Q2	0.2	0.8	3.0	

**Switching Characteristics**

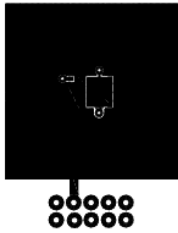
$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 15\text{ V}$ , $I_D = 13\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$ Q2: $V_{DD} = 15\text{ V}$ , $I_D = 23\text{ A}$ , $R_{GEN} = 6\text{ }\Omega$	Q1 Q2		8.2 13	16 23	ns
$t_r$	Rise Time		Q1 Q2		2.5 4.8	10 10	ns
$t_{d(off)}$	Turn-Off Delay Time		Q1 Q2		20 31	32 50	ns
$t_f$	Fall Time		Q1 Q2		2.2 3.4	10 10	ns
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V}$ to $10\text{ V}$	Q1 Q2		21 47	29 66	nC
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V}$ to $4.5\text{ V}$	Q1 Q2		10 22	14 31	nC
$Q_{gs}$	Gate to Source Gate Charge	Q2 $V_{DD} = 15\text{ V}$ , $I_D = 23\text{ A}$	Q1 Q2		3.9 9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge		Q1 Q2		3.1 5.5		nC

# Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>Drain-Source Diode Characteristics</b>							
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 13\text{ A}$ (Note 2) $V_{GS} = 0\text{ V}$ , $I_S = 23\text{ A}$ (Note 2)	Q1 Q2		0.8 0.8	1.2 1.2	V
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 13\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	Q1 Q2		25 32	40 51	ns
$Q_{rr}$	Reverse Recovery Charge	Q2 $I_F = 23\text{ A}$ , $di/dt = 300\text{ A}/\mu\text{s}$	Q1 Q2		9 39	18 62	nC

## Notes:

1:  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



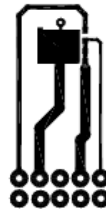
a. 57 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b. 50 °C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



c. 125 °C/W when mounted on a minimum pad of 2 oz copper



d. 120 °C/W when mounted on a minimum pad of 2 oz copper

2: Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

3: As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

4:  $E_{AS}$  of 40 mJ is based on starting  $T_J = 25\text{ }^{\circ}\text{C}$ ; N-ch:  $L = 1\text{ mH}$ ,  $I_{AS} = 9\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 14\text{ A}$ .

5:  $E_{AS}$  of 112 mJ is based on starting  $T_J = 25\text{ }^{\circ}\text{C}$ ; N-ch:  $L = 1\text{ mH}$ ,  $I_{AS} = 15\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% test at  $L = 0.3\text{ mH}$ ,  $I_{AS} = 22\text{ A}$ .

Typical Characteristics (Q1 N-Channel)  $T_J = 25^\circ\text{C}$  unless otherwise noted

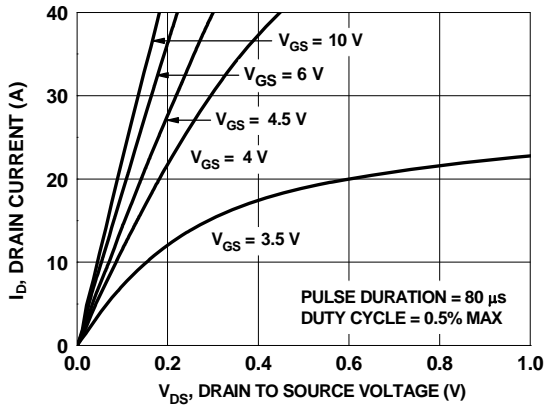


Figure 1. On Region Characteristics

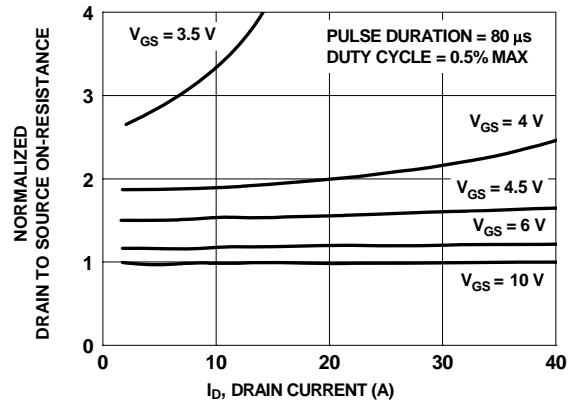


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

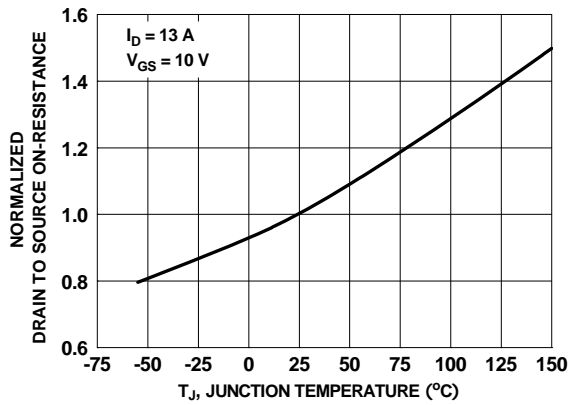


Figure 3. Normalized On Resistance vs Junction Temperature

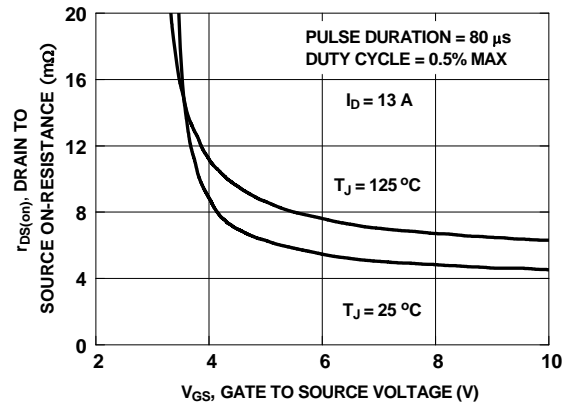


Figure 4. On-Resistance vs Gate to Source Voltage

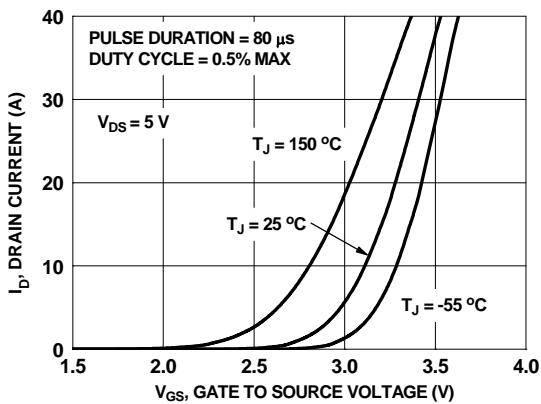


Figure 5. Transfer Characteristics

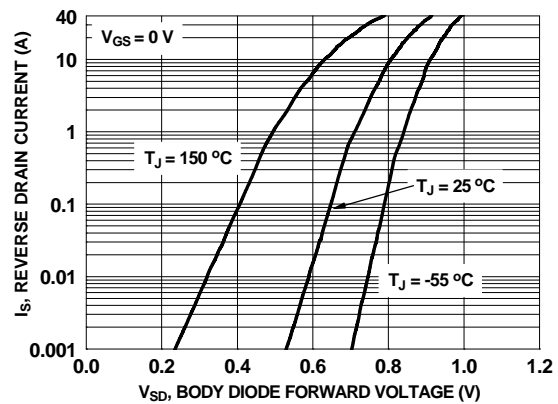


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

# Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

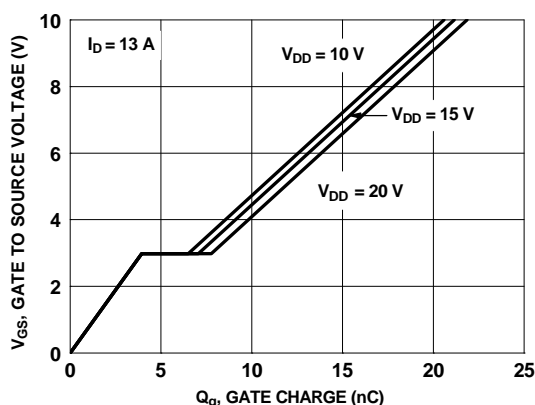


Figure 7. Gate Charge Characteristics

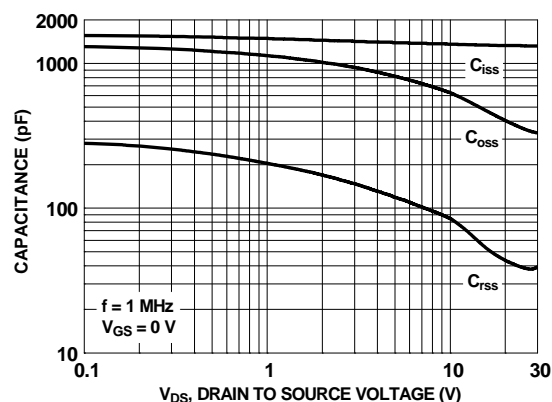


Figure 8. Capacitance vs Drain to Source Voltage

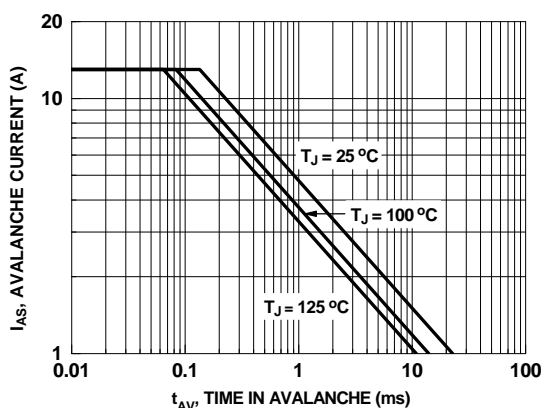


Figure 9. Unclamped Inductive Switching Capability

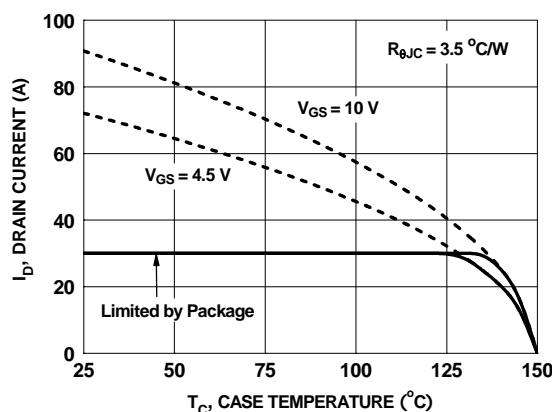


Figure 10. Maximum Continuous Drain Current vs Case Temperature

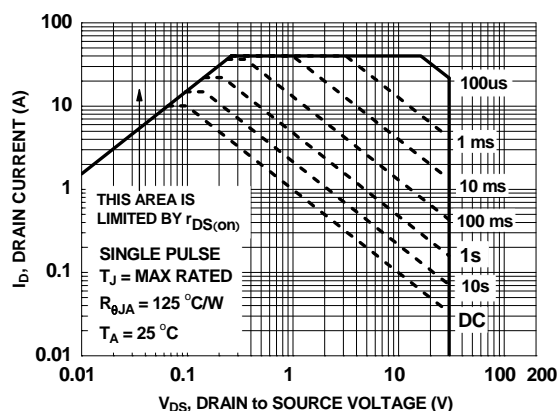


Figure 11. Forward Bias Safe Operating Area

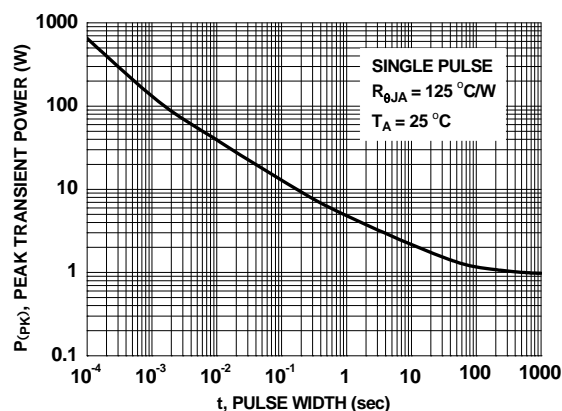


Figure 12. Single Pulse Maximum Power Dissipation

# Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

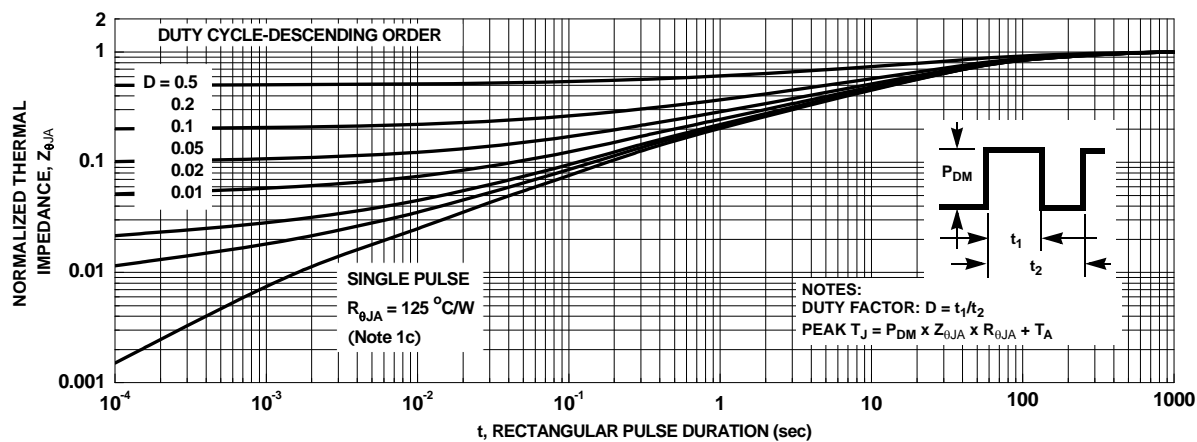


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Typical Characteristics (Q2 N-Channel)  $T_J = 25^\circ\text{C}$  unless otherwise noted

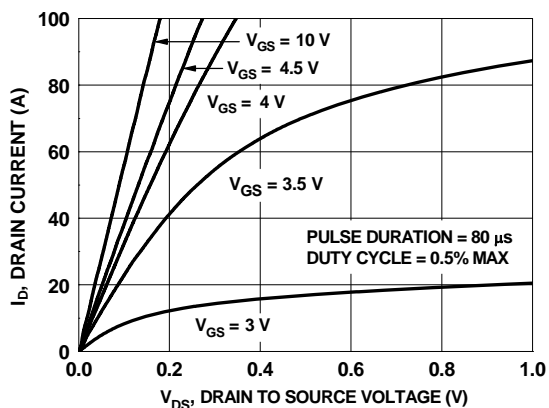


Figure 14. On-Region Characteristics

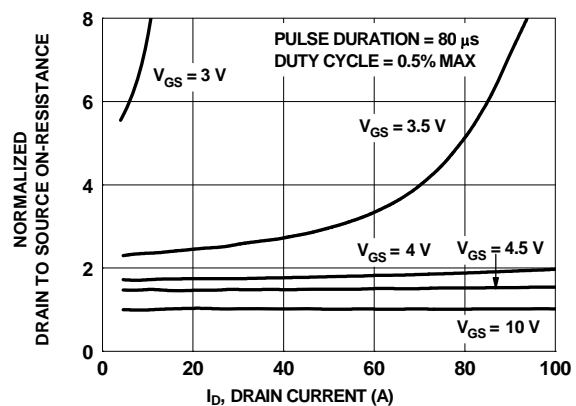


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

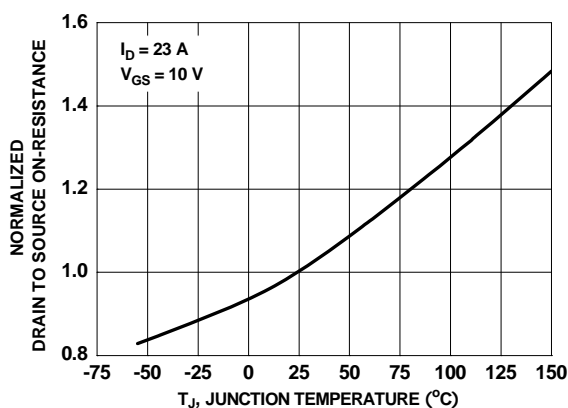


Figure 16. Normalized On-Resistance vs Junction Temperature

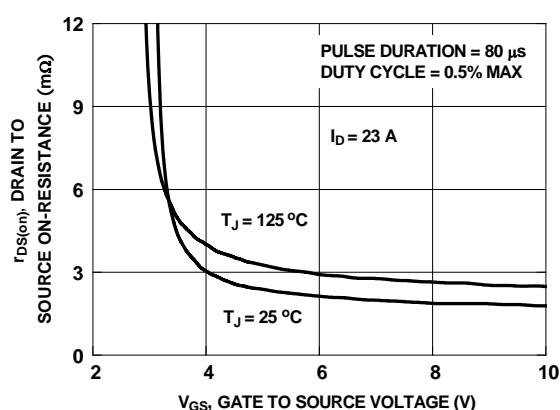


Figure 17. On-Resistance vs Gate to Source Voltage

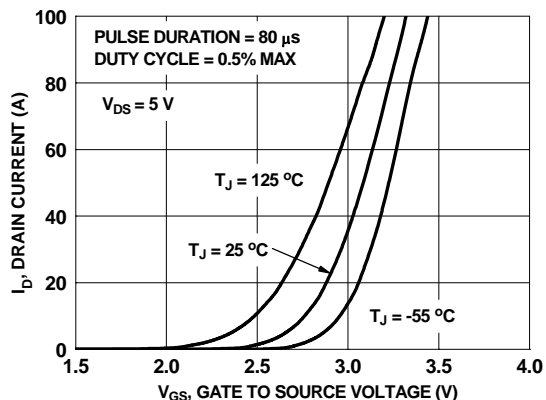


Figure 18. Transfer Characteristics

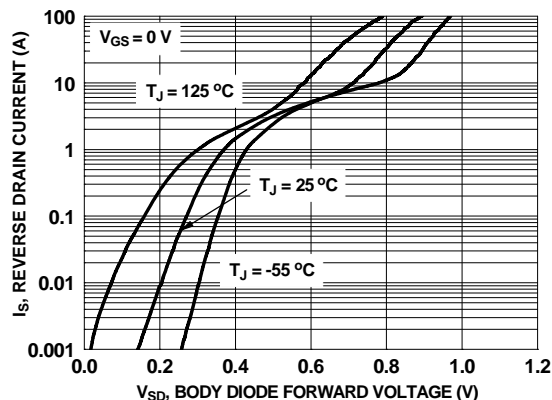


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 N-Channel)  $T_J = 25^\circ\text{C}$  unless otherwise noted

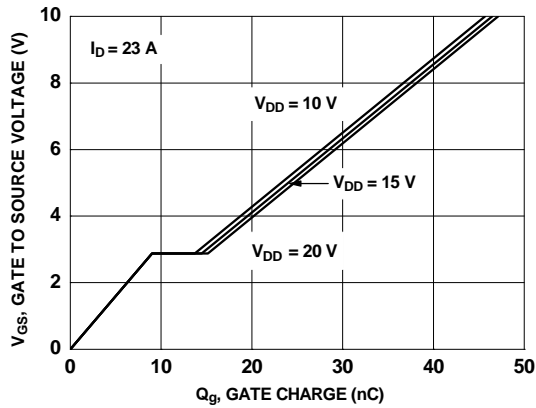


Figure 20. Gate Charge Characteristics

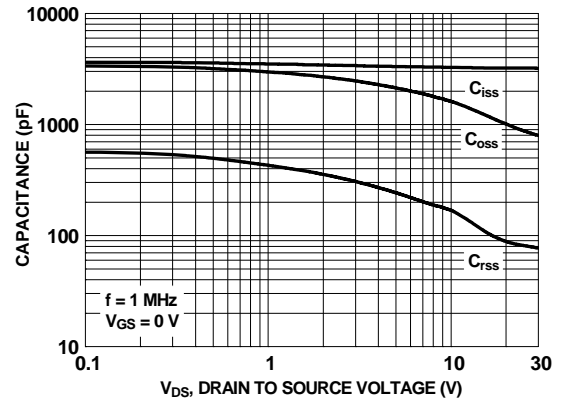


Figure 21. Capacitance vs Drain to Source Voltage

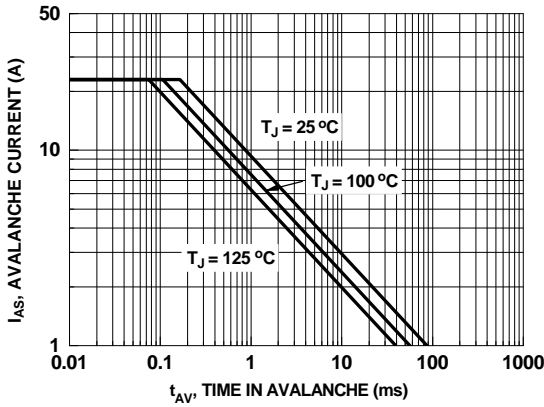


Figure 22. Unclamped Inductive Switching Capability

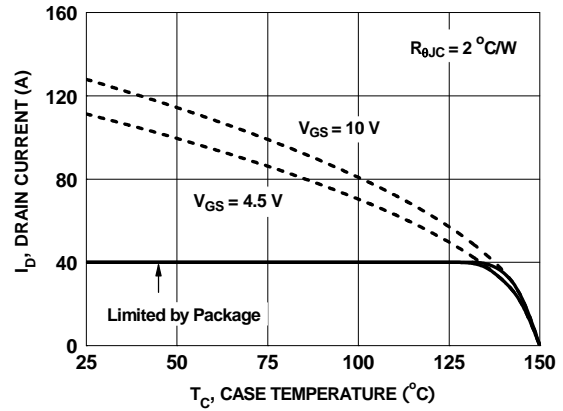


Figure 23. Maximum Continuous Drain Current vs Case Temperature

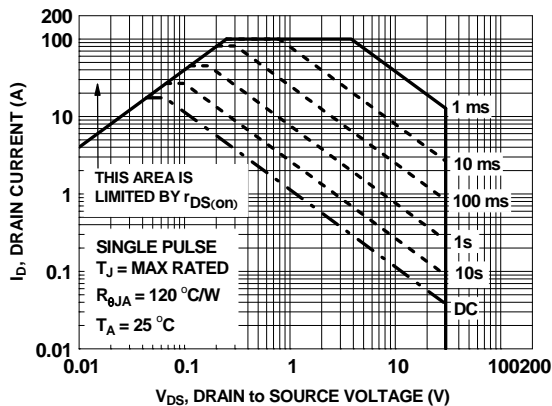


Figure 24. Forward Bias Safe Operating Area

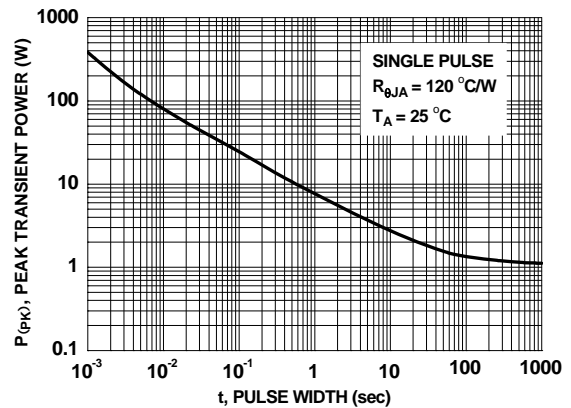


Figure 25. Single Pulse Maximum Power Dissipation



Typical Characteristics (Q2 N-Channel)  $T_J = 25\text{ }^{\circ}\text{C}$  unless otherwise noted

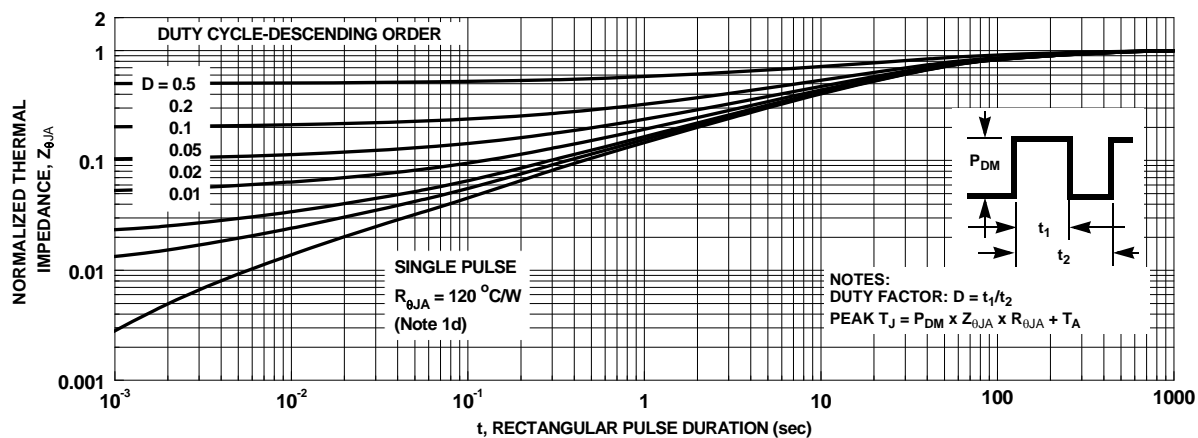


Figure 26. Junction-to-Ambient Transient Thermal Response Curve

## Typical Characteristics (continued)

### SyncFET Schottky body diode Characteristics

Fairchild's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS3604S.

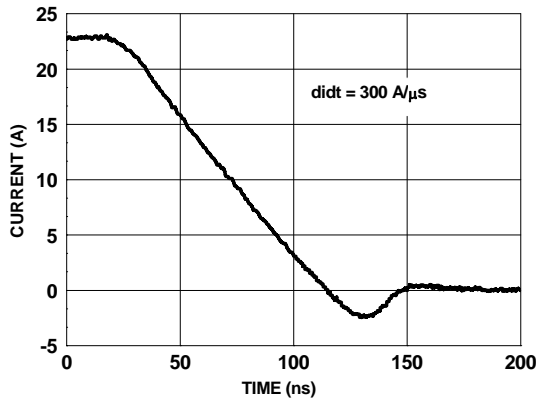


Figure 27. FDMS3604S SyncFET body diode reverse recovery characteristic

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

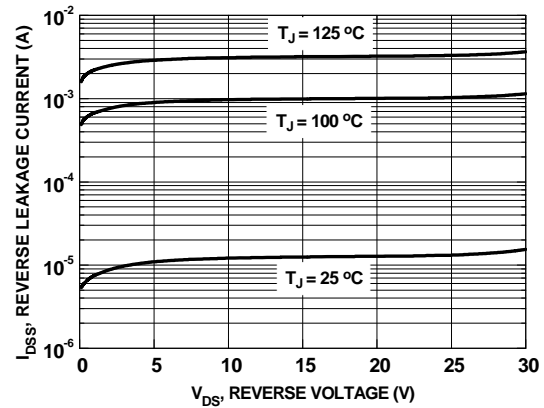
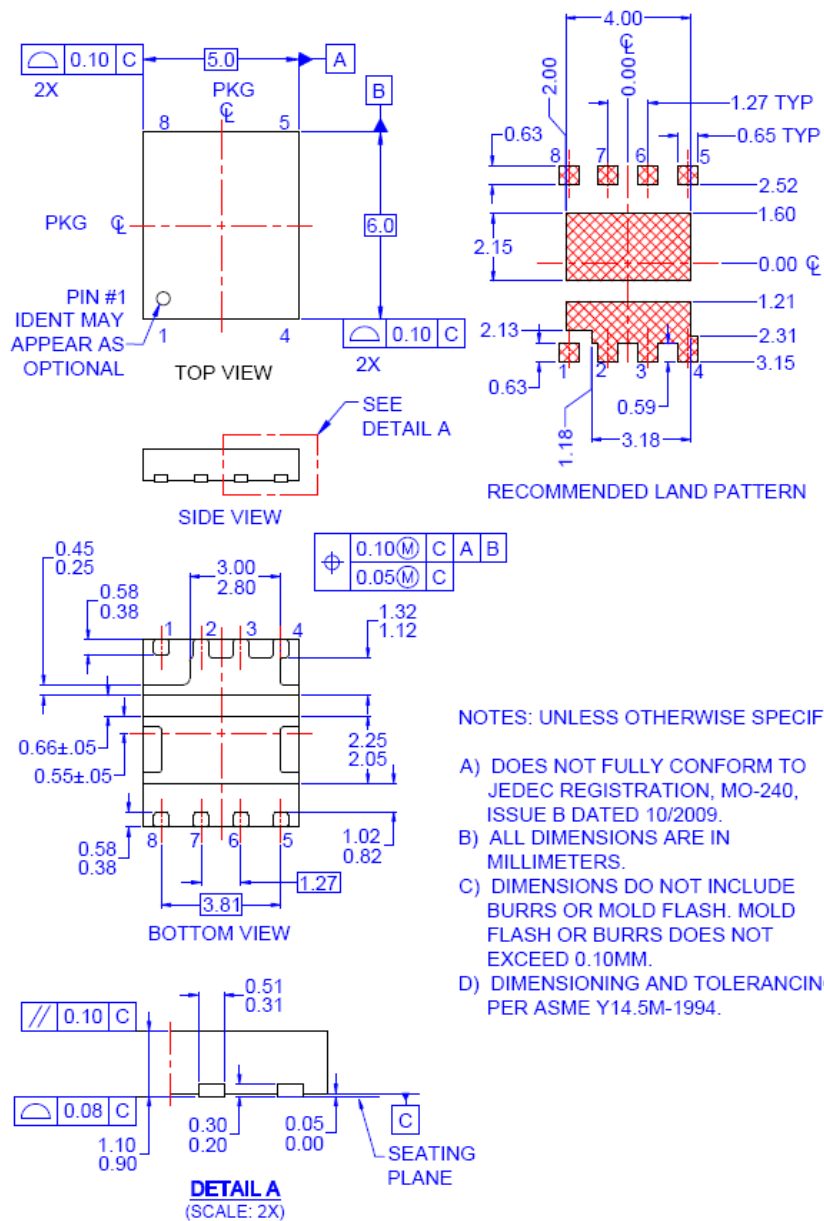


Figure 28. SyncFET body diode reverse leakage versus drain-source voltage

# Dimensional Outline and Pad Layout





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**PRODUCT STATUS DEFINITIONS****Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

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