HT2269

GENERAL DESCRIPTION

HT2269 is a highly integrated current mode PWM control IC optimized for high performance, low standby power and cost effective offline flyback converter applications.

PWM switching frequency at normal operation is externally programmable and trimmed to tight range. At no load or light load condition, the IC operates in extended 'burst mode' to minimize switching loss. Lower standby power and higher conversion efficiency is thus achieved.

VDD low startup current and low operating current contribute to a reliable power on startup design with HT2269. A large value resistor could thus be used in the startup circuit to minimize the standby power.

The internal slope compensation improves system large signal stability and reduces the possible sub-harmonic oscillation at high PWM duty cycle output. Leading-edge blanking on current sense input removes the signal glitch due to snubber circuit diode reverse recovery. This greatly helps to reduce the external component count and system cost in application.

HT2269 offers complete protection coverage with automatic self-recovery feature including Cycle-by-Cycle current limiting (OCP), over load protection (OLP), over temperature protection (OTP), VDD over voltage protection (OVP) and under voltage lockout (UVLO). The Gate-drive output is clamped at 18V to protect the power MOSFET.

In HT2269, OCP threshold slope is internally optimized to reach constant output power limit over universal AC input range.

Excellent EMI performance is achieved frequency shuffling technique together with soft switching control at the totem pole gate drive output.

The tone energy at below 20KHZ is minimized in operation. Consequently, audio noise erformance is greatly improved. HT2269 is offered in both SOP-8 and DIP-8 packages.

FEATURES

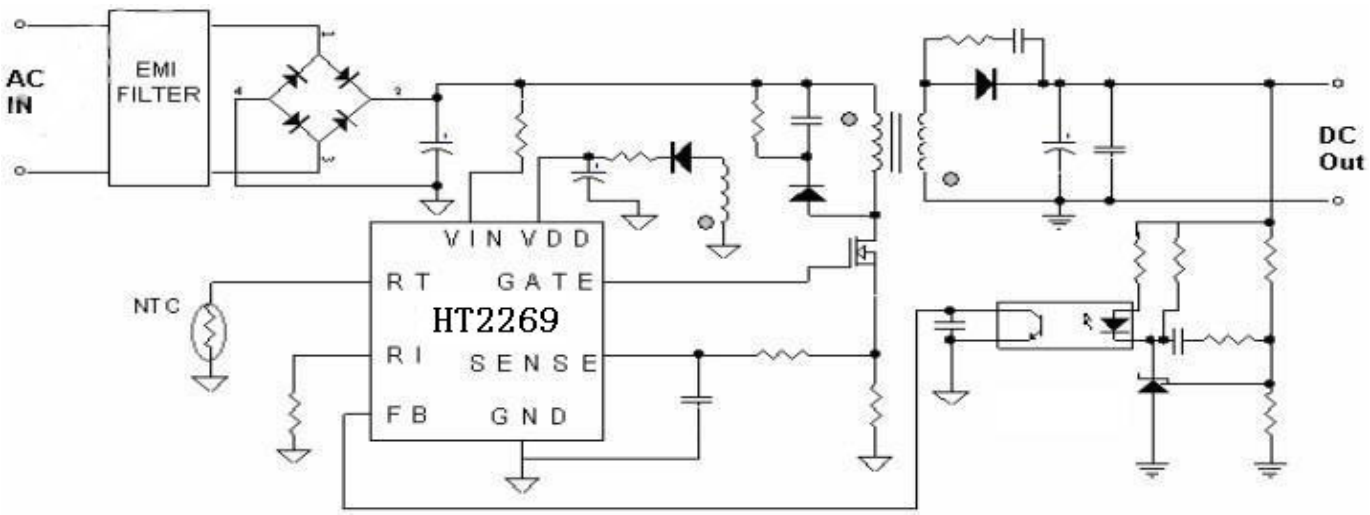
- Extended Burst Mode Control For Improved Efficiency and Minimum Standby Power Design.
- Audio Noise Free Operation
- External Programmable PWM Switching Frequency
- Internal Synchronized Slope Compensation
- Low VIN/VDD Startup Current(6.5uA) and Low Operating Current (2.3mA)
- Leading Edge Blanking on Current Sense Input
- Complete Protection Coverage With Auto Self-Recovery
- External Programmable Over Temperature Protection (OTP)
- On-chip VDD OVP for System OVP
- Under Voltage Lockout with Hysteresis (UVLO)
- Gate Output Maximum Voltage Clamp (18V)
- Line Compensated Cycle-by-Cycle Over-current Threshold Setting For Constant Output Current Limiting Over Universal Input Voltage Range (OCP)
- Over Load Protection. (OLP)

APPLICATIONS

Offline AC/DC flyback converter for

- Laptop Power Adaptor
- PC/TV/Set-Top Box Power Supplies
- Open-frame SMPS
- Battery Charge

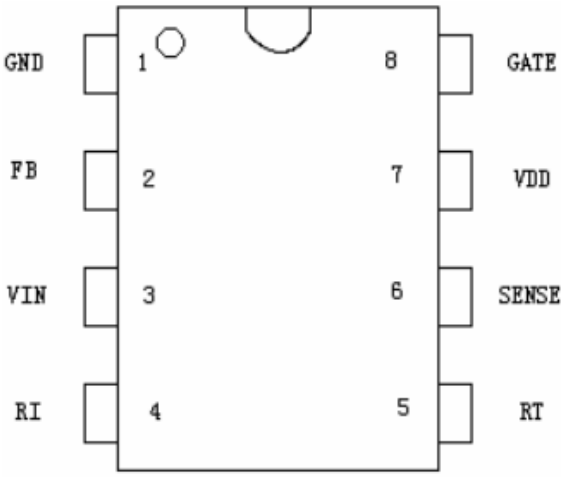
TYPICAL APPLICATION



GENERAL INFORMATION

Pin Configuration

The HT2269 is offered in DIP and SOP packages
shown as below.



Ordering Information

Part Number	Description
HT2269AP	With Frequency Shuffling, DIP8, Pb-free, Have OVP
HT2269CP	With Frequency Shuffling, SOP8, Pb-free, Have OVP

Package Dissipation Rating

Package	RθJA (°C/W)
DIP8	90
SOP8	150

Absolute Maximum Ratings

Parameter	Value
VDD/VIN DC Supply Voltage	30 V
VDD Zener Clamp Voltage[Note]	VDD_Clamp+ 0.1V
VDD Clamp Continuous Current	10 mA
V_{FB} Input Voltage	-0.3 to 7V
V_{SENSE} Input Voltage to ense Pin	-0.3 to 7V
V_{RT} Input Voltage to RT Pin	-0.3 to 7V
V_{RI} Input Voltage to RI Pin	-0.3 to 7V
Min/Max Operating Junction Temperature T_J	-20 to 150 °C
Min/Max Storage Temperature T_{stg}	-55 to 150 °C
Lead Temperature (Soldering,10secs)	260°C

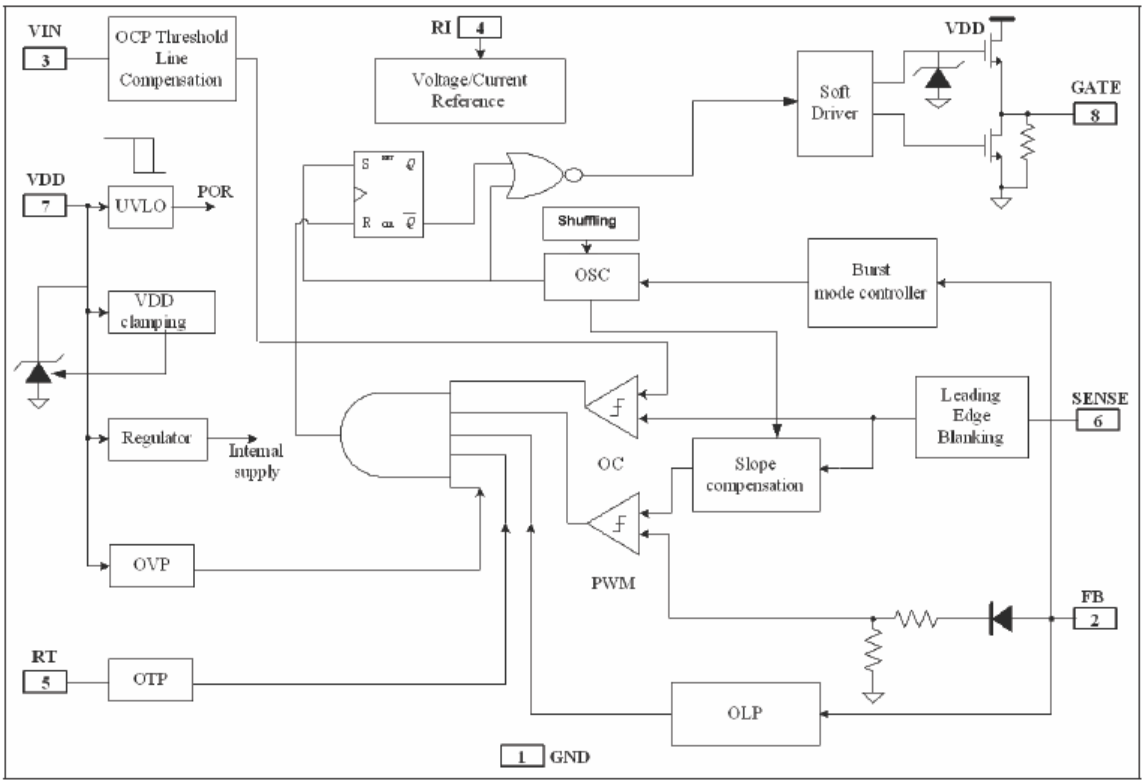
Note: VDD_Clamp has a nominal value of 35V.

Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute maximum-rated conditions for extended periods may affect device reliability.

TERMINAL ASSIGNMENTS

Pin Num	Pin Name	I/O	Description
1	GND	P	Ground
2	FB	I	Feedback input pin. PWM duty cycle is determined by voltage level into this pin and current-sense signal level at Pin 6.
3	VIN	I	Connected through a large value resistor to rectified line input for Startup IC supply and line voltage sensing.
4	RI	I	Internal Oscillator frequency setting pin. A resistor connected between RI and GND sets the PWM frequency.
5	RT	I	Temperature sensing input pin. Connected through a NTC resistor to GND.
6	SENSE	I	Current sense input pin. Connected to MOSFET current sensing resistor node.
7	VDD	P	DC power supply pin.
8	GATE	O	Totem-pole gate drive output for power MOSFET.

BLOCK DIAGRAM



RECOMMENDED OPERATING CONDITION

Symbol	Parameter	Min	Max	Unit
VDD	VDD Supply Voltage	12	23	V
RI	RI Resistor Value	24	31	Kohm
T_A	Operating Ambient Temperature	-20	85	^oC

ESD INFORMATION

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
HBM[Note]	Human Body Model on All Pins Except VIN and VDD	MIL-STD		3		KV
MM	Machine Model on All Pins	JEDEC-STD		250		V

Note: HBM all pins pass 3KV except High Voltage Input pin. The details are VIN passes 1kV, VDD passes 1.5KV, all other I/Os pass 3KV. In system application, High Voltage Input pin is either a high impedance input or connected to a cap. The lower rating has minimum impacts on system ESD performance.

ELECTRICAL CHARACTERISTICS

(T_A = 25^{O}C, VDD=16V, RI=24Kohm if not otherwise noted)

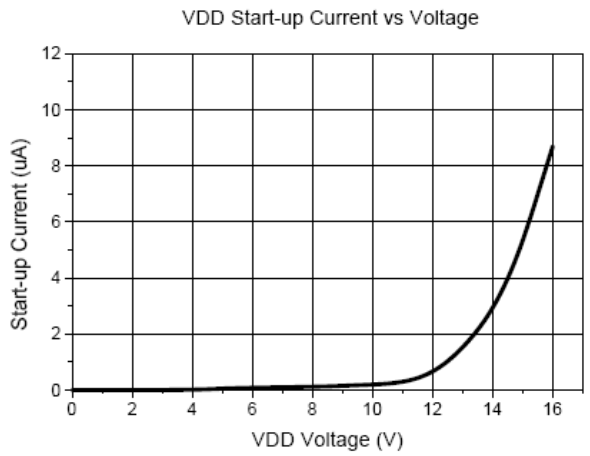
Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Supply Voltage (VDD)						
I_VDD_Startup	VDD Start up Current	VDD =15V, Measure current into VDD		6.5	20	uA
I_VDD_Operation	Operation Current	V_{FB}=3V		2.3		mA
UVLO(Enter)	VDD Under Voltage Lockout Enter		9.5	10.5	11.5	V
UVLO(Exit)	VDD Under Voltage Lockout Exit (Startup)		16	17	18	V
OVP(ON)*Optional	VDD Over Voltage Protection Enter		23.5	25	26.5	V
OVP(OFF)*Optional	VDD Over Voltage Protection Exit (Recovery)		21.5	23.2	24.7	V
OVP_Hys*Optional	OVP Hysteresis	OVP(ON)-OVP(OFF)		2		V
T_D_OVP	VDD OVP Debounce time			80		uSec
V_{DD}_Clamp	V_{DD} Zener Clamp Voltage	I(V_{DD}) = 5mA		36		V
Feedback Input Section(FB Pin)						
A_{VCS}	PWM Input Gain	$\Delta V_{FB}/\Delta V_{cs}$		2.6		V/V
V_{FB}_Open	V_{FB} Open Voltage			6		V
I_{FB}_Short	FB pin short circuit current	Short FB pin to GND, measure current		0.80		mA
V_{TH}_0D	Zero Duty Cycle FB Threshold Voltage				0.95	V
V_{TH}_BM	Burst Mode FB Threshold Voltage			1.7		V
V_{TH}_PL	Power Limiting FB Threshold Voltage			4.4		V
T_D_PL	Power limiting Debounce Time			80		mSec
Z_{FB}_IN	Input Impedance			7.5		Kohm

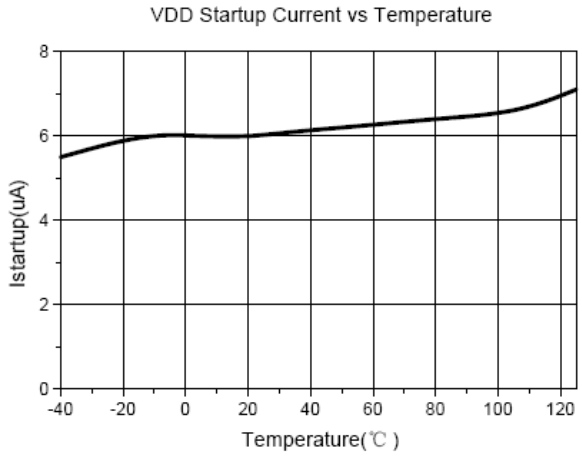
Current Sense Input(Sense Pin)						
T_blanking	Sense Input Leading Edge Blanking Time			300		nS
Z_{SENSE}_IN	Sense Input			39		Kohm
	Impedance					
T_D_OC	Over Current Detection and Control Delay	CL=1nf at GATE,		120		nSec
V_{TH}_OC_0	Current Limiting Threshold at No Compensation	I(VIN) = 0uA	0.85	0.90	0.95	V
V_{TH}_OC_1	Current Limiting Threshold at Compensation	I(VIN) = 150uA		0.81		V
Oscillator						
F_{OSC}	Normal Oscillation Frequency		60	65	70	KHZ
∆f_Temp	Frequency Temperature Stability	-20°C to 100°C		2		%
∆f_VDD	Frequency Voltage Stability	VDD = 12-25V		2		%
RI_range	Operating RI Range		12	24	60	Kohm
V_RI_open	RI open voltage			2.0		V
F_BM	Burst Mode Base Frequency			22		KHZ
DC_max	Maxmum Duty Cycle		75	80	85	%
DC_min	Minimum Duty Cycle		-	-	0	%
Gate Drive Output						
VOL	Output Low Level	Io = -20 mA			0.3	V
VOH	Output High Level	Io = +20 mA	11			V
VG_Clamp	Output Clamp Voltage Level	VDD=20V		18		V
T_r	Output Rising Time	CL = 1nf		120		nSec
T_f	Output Falling Time	CL = 1nf		50		nSec
Over Temperature Protection						

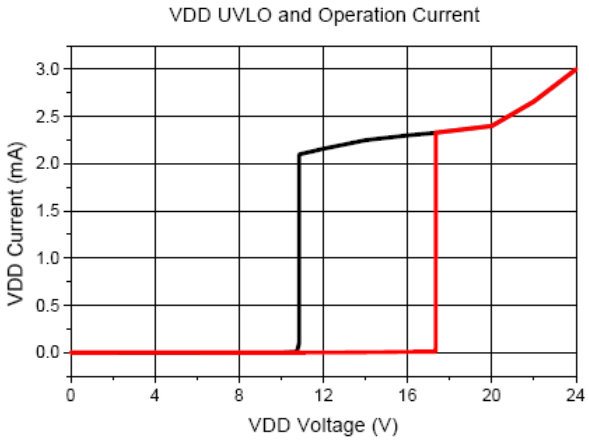
I_RT	Output Current of RT pin			70		uA
V_{TH}_OTP	OTP Threshold Voltage		1.0	1.065	1.13	V
V_{TH}_OTP_off	OTP Recovery Threshold Voltage			1.165		V
T_D_OTP	OTP De-bounce Time			100		uSec
V_RT_Open	RT Pin Open Voltage			3.5		V
Frequency Shuffling						
Δf_OSC	Frequency Modulation range /Base frequency		-3		3	%
Freq_Shuffling	Shuffling Frequency	RI = 24Kohm		32		HZ

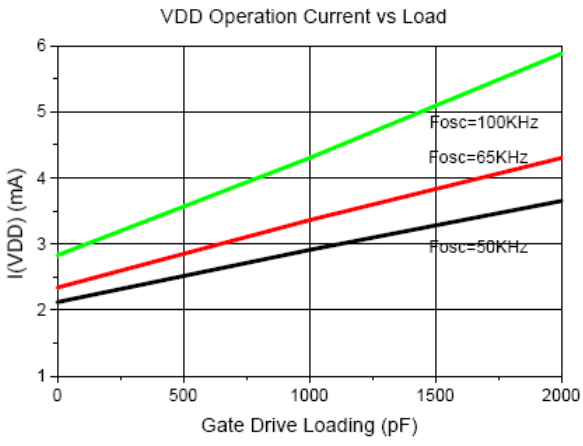
CHARACTERIZATION PLOTS

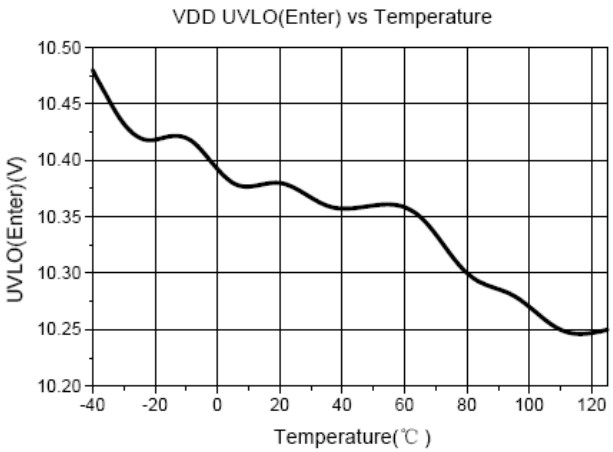
(T_A = 25°C, VDD=16V, RI=24Kohm if not otherwise noted)

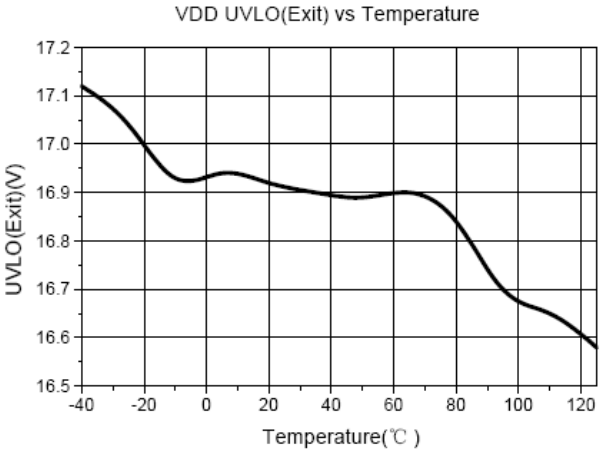


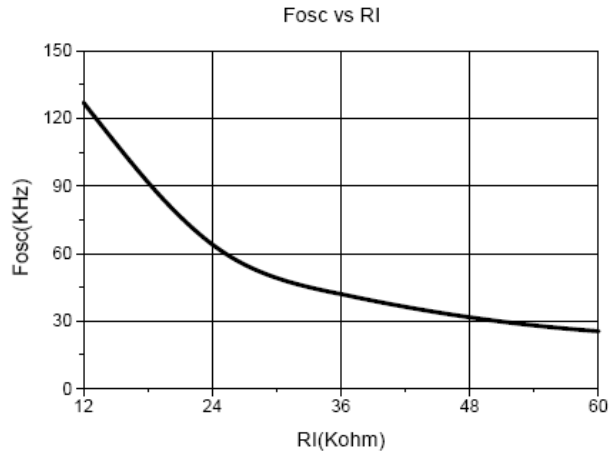


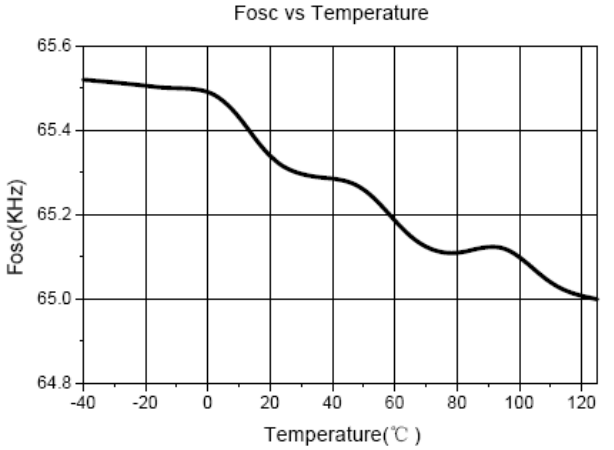


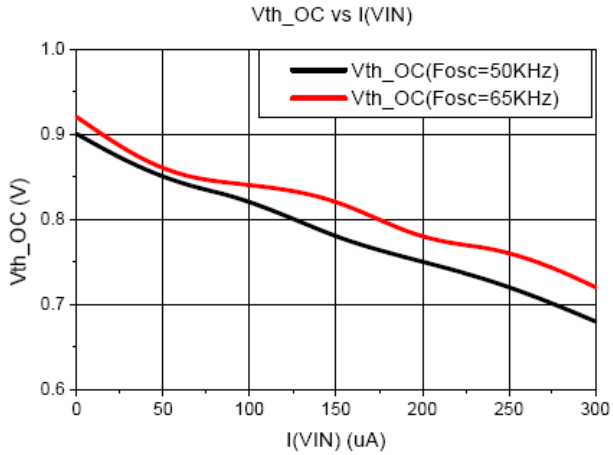


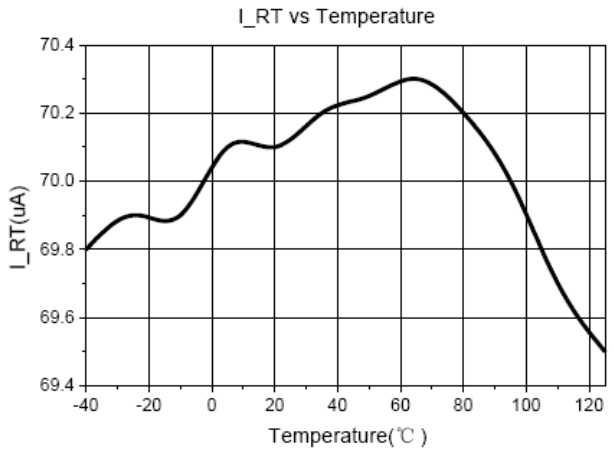

VDD UVLO(Enter) vs Temperature
UVLO(Enter)(V)
10.50
10.45
10.40
10.35
10.30
10.25
10.20
-40 -20 0 20 40 60 80 100 120
Temperature(℃)


VDD UVLO(Exit) vs Temperature
UVLO(Exit)(V)
17.2
17.1
17.0
16.9
16.8
16.7
16.6
16.5
-40 -20 0 20 40 60 80 100 120
Temperature(℃)


Fosc vs RI
Fosc(KHz)
150
120
90
60
30
0
12 24 36 48 60
RI(Kohm)


Fosc vs Temperature
Fosc(KHz)
65.6
65.4
65.2
65.0
64.8
-40 -20 0 20 40 60 80 100 120
Temperature(℃)


Vth_OC vs I(VIN)
Vth_OC(Fosc=50KHz)
Vth_OC(Fosc=65KHz)
Vth_OC (V)
1.0
0.9
0.8
0.7
0.6
0 50 100 150 200 250 300
I(VIN) (uA)


I_RT vs Temperature
I_RT(uA)
70.4
70.2
70.0
69.8
69.6
69.4
-40 -20 0 20 40 60 80 100 120
Temperature(℃)

OPERATION DESCRIPTION

The HT2269 is a highly integrated PWM controller IC optimized for offline flyback converter applications. The extended burst mode control greatly reduces the standby power consumption and helps the design easily meet the international power conservation requirements.

- **Startup Current and Start up Control**

Startup current of HT2269 is designed to be very low so that VDD could be charged up above UVLO(exit) threshold level and device starts up quickly. A large value startup resistor can herefore be used to minimize the power loss yet reliable startup in application. For a typical AC/DC adaptor with universal input range design, a 2 MΩ, 1/8 W startup resistor could be used together with a VDD capacitor to provide a fast startup and yet low power dissipation design solution.

- **Operating Current**

The Operating current of HT2269 is low at 2.3mA. Good efficiency is achieved with HT2269 low operating current together with extended burst mode control schemes.

- **Frequency shuffling for EMI improvement**

The frequency Shuffling/jittering (switching frequency modulation) is implemented in HT2269. The oscillation frequency is modulated with a internally generated random source so that the tone energy is evenly spread out. The spread spectrum minimizes the conduction band EMI and therefore eases the system design in meeting stringent EMI requirement.

- **Burst Mode Operation**

At zero load or light load condition, most of the power dissipation in a switching mode power supply is from switching loss on the MOSFET transistor, the core loss of the transformer and the loss on the snubber circuit. The magnitude of power loss is in proportion to the number of switching events within a fixed period of time. Reducing switching events leads to the reduction on the power loss and thus conserves the energy.

HT2269 self adjusts the switching mode according to the loading condition. At from no load to light/medium load condition, the FB input drops below burst mode threshold level (1.8V). Device enters Burst Mode control. The Gate drive output switches only when VDD voltage drops below a preset level and FB input is active to output an on state. Otherwise the gate drive remains at off stateto minimize the switching loss thus reduce thestandby power consumption to the greatest extend. The nature of high frequency switching also reduces the audio noise at any loading conditions.

- **Oscillator Operation**

A resistor connected between RI and GND sets the constant current source to

charge/discharge the internal cap and thus the PWM oscillator frequency is determined. The relationship between RI and switching frequency follows the below equation within the specified RI in Kohm range at nominal loading operational condition.

$$F_{osc} = \frac{1560}{RI(Kohm)}(Khz)$$

- **Current Sensing and Leading Edge Blanking**

Cycle-by-Cycle current limiting is offered in HT2269 current mode PWM control. The switch current is detected by a sense resistor into the sense pin. An internal leading edge blanking circuit chops off the sense voltage spike at initial MOSFET on state due to snubber diode reverse recovery so that the external RC filtering on sense input is no longer required. The current limit comparator is disabled and thus cannot turn off the external MOSFET during the blanking period. PWM duty cycle is determined by the current sense input voltage and the FB input voltage.

- **Internal Synchronized Slope Compensation**

Built-in slope compensation circuit adds voltage ramp onto the current sense input voltage for PWM generation. This greatly improves the close loop stability at CCM and prevents the sub-harmonic oscillation and thus reduces the output ripple voltage.

- **Over Temperature Protection**

A NTC resistor in series with a regular resistor should connect between RT and GND for temperature sensing and protection. NTC resistor value becomes lower when the ambient temperature rises. With the fixed internal current IRT flowing through the resistors, the voltage at RT pin becomes lower at high temperature. The internal OTP circuit is triggered and shutdown the MOSFET when the sensed input voltage is lower than VTH_OTP.

- **Gate Drive**

HT2269 Gate is connected to the Gate of an external MOSFET for power switch control. Too weak the gate drive strength results in higher conduction and switch loss of MOSFET while too strong gate drive output compromises the EMI. Good tradeoff is achieved through the built-in totem pole gate drive design with right output strength and dead time control. The low idle loss and good EMI system design is easier to achieve with this dedicated control scheme. An internal 18V clamp is added for MOSFET gate protection at higher than expected VDD input.

- **Protection Controls**

Good system reliability is achieved with HT2269's rich protection features including Cycle-by-Cycle current limiting (OCP), Over Load Protection (OLP), over temperature protection (OTP), on-chip VDD over voltage protection (OVP, optional) and

under voltage lockout (UVLO). The OCP

threshold value is self adjusted lower at higher current into VIN pin. This OCP threshold slope adjustment helps to compensate the increased output power limit at higher AC voltage caused by inherent Over-Current sensing and control delay. A constant output power limit is achieved with recommended OCP compensation scheme on HT2269.

At output overload condition, FB voltage is biased higher. When FB input exceeds power limit threshold value for more than 80mS, control circuit reacts to turnoff the power MOSFET.

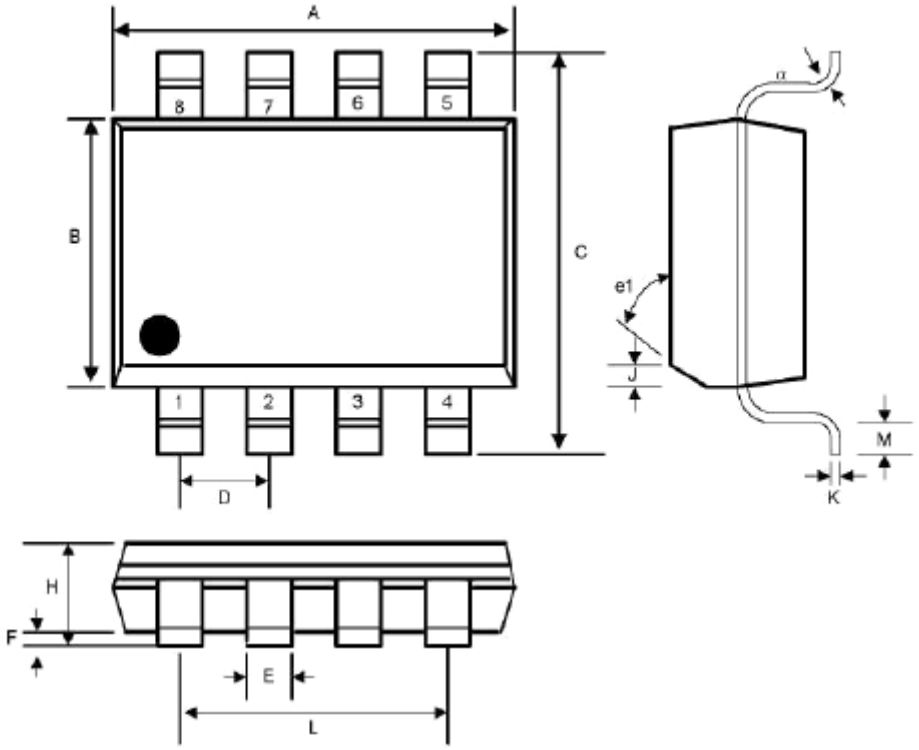
Similarly, control circuit shutdowns the power MOSFET when an Over Temperature condition is detected. HT2269 resumes the operation when temperature drops below the hysteresis value.

VDD is supplied with transformer auxiliary winding output. It is clamped when VDD is higher than 35V. MOSFET is shut down when VDD drops below UVLO(enter) limit and device enters power on startup sequence thereafter.

PACKAGE MECHANICAL DATA

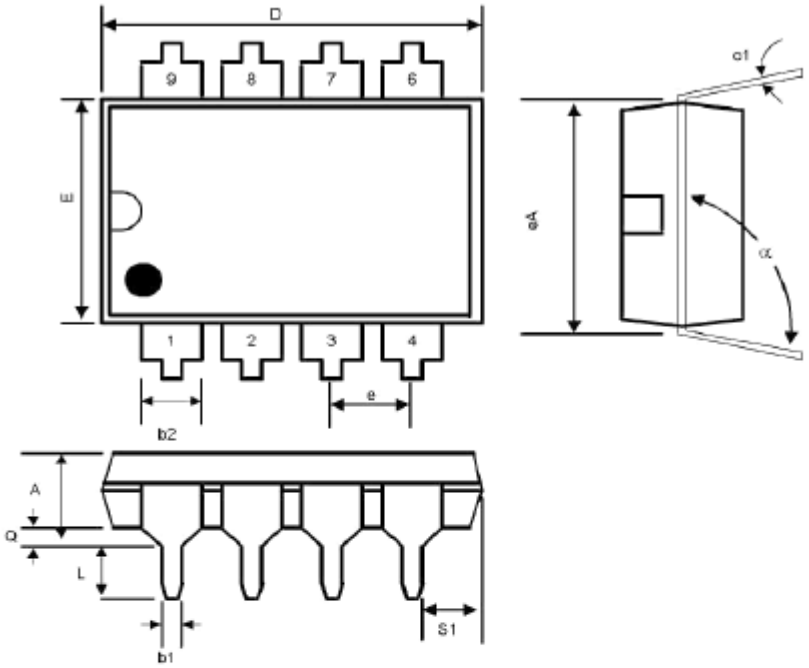
HT2269

SOP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.188	0.197	4.80	5.00	-
B	0.149	0.158	3.80	4.00	-
C	0.228	0.244	5.80	6.20	-
D	0.050 BSC		1.27 BSC		-
E	0.013	0.020	0.33	0.51	-
F	0.004	0.010	0.10	0.25	-
H	0.053	0.069	1.35	1.75	-
J	0.011	0.019	0.28	0.48	
K	0.007	0.010	0.19	0.25	-
M	0.016	0.050	0.40	1.27	
L	0.150 REF		3.81 REF		-
e1	45^0		45^0		-
α	0^0	8^0	0^0	8^0	-

DIP8 PACKAGE OUTLINE DIMENSIONS



SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b1	0.014	0.023	0.36	0.58	-
b2	0.045	0.065	1.14	1.65	-
c1	0.008	0.015	0.20	0.38	-
D	0.355	0.400	9.02	10.16	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	-
s1	0.005	-	0.13	-	-
α	90^0	105^0	90^0	105^0	-