MP7770

2 x 45W Stereo Single-Ended or 90W Mono BTL Class-D Audio Amplifier

The Future of Analog IC Technology

DESCRIPTION

MP7770 is an analog class-D audio amplifier that can drive either stereo speakers in single-ended configuration or a mono speaker in a bridge-tied-load configuration. It is part of MPS's family of fully-integrated audio amplifiers that dramatically reduce footprint size by integrating:

- 100mΩ power MOSFETs
- Startup/Shutdown pop elimination
- Short-circuit protection circuits

The MP7770 is capable of delivering 45W per channel into 4Ω speaker in single-ended output structure, or delivering 90W into 8Ω speaker in bridge-tied-load output structure under 36V VDD. MPS's class D audio amplifiers exhibit the high fidelity of a Class A/B amplifier at higher efficiencies. The circuit is based on the MPS's proprietary variable-frequency topology, which delivers excellent linearity, fast response time and operates from a single power supply.

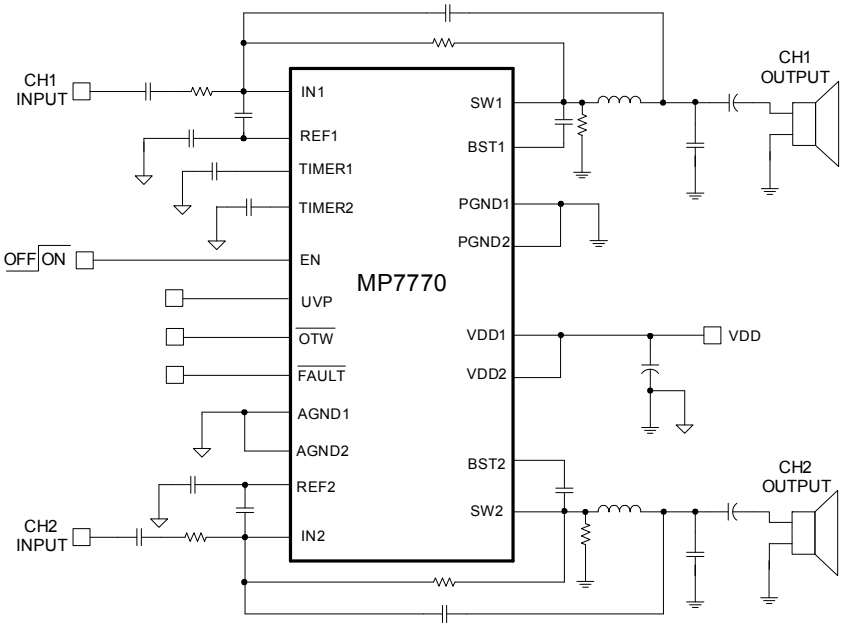
FEATURES

- 9.5V-to-36V Operation from a Single Supply
- ±8.5A Peak Current Output
- Output Power at 36V and 10%THD:
  - Stereo Single-Ended: 2 x 45W into 4Ω Load,
  - Bridge-Tied Load: 90W into 8Ω Load
- THD+N = 0.03% at 1W, 8Ω
- > 90% Efficiency at 10%THD
- Low Noise
- Switching Frequency of up to 1MHz
- Integrated Startup and Shutdown Pop Elimination Circuit
- Programmable UVP
- Thermal and Short-Circuit Protection
- Output Fault Flag and Thermal Warning
- Integrated Power FETs
- TSSOP28-EP Package with Exposed Pad on Bottom
- TSSOP28-EPR Package with Exposed Pad on Top, Please Contact Factory for the Availability

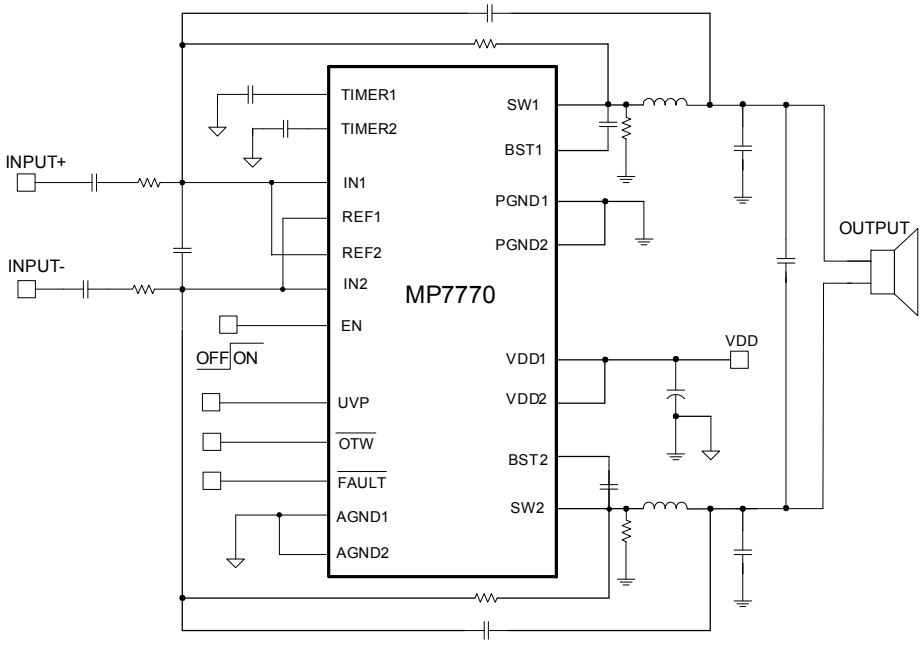
APPLICATIONS

- DVD Receiver
- Mini Combo System
- Home Theater Systems
- Surround Sound Systems
- Audio Docking or High-Power Sound Box

TYPICAL APPLICATIONS



Stereo SE Application Circuit



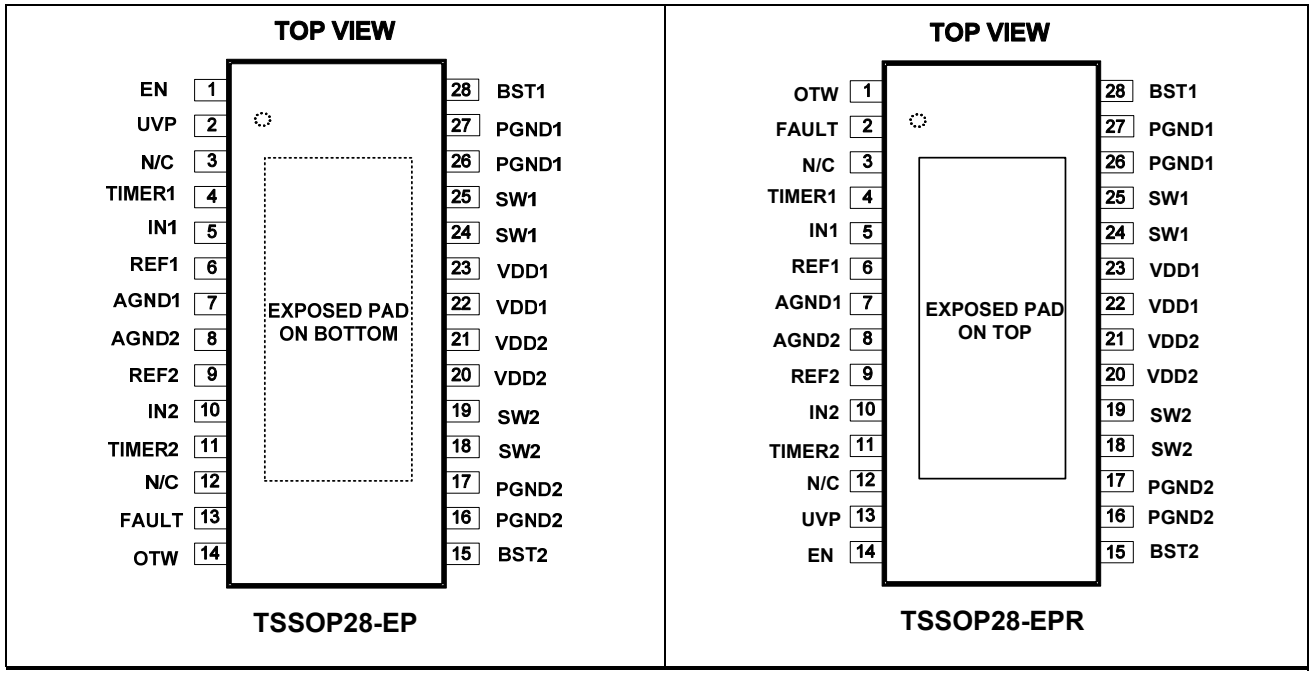
Mono BTL Application Circuit

ORDERING INFORMATION

Part Number*	Package	Top Marking
MP7770GF	TSSOP28-EP	MP7770
**MP7770GFR	TSSOP28-EPR	MP7770R

* For Tape & Reel, add suffix –Z (e.g. MP7770GF–Z);
** Contact Factory for TSSOP28F-EPR Availability

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS (1)

Supply Voltage V_{DD} 40V
BS Voltage ..... (V_{SW} - 0.3V) to (V_{SW} + 6.5V)
V_{OTW}, V_{FAULT}, V_{UVP}, V_{TIMER}, V_{EN} .....–0.3V to +6V
V_{SW} .....–0.3V to (V_{DD} + 1V)
V_{REF}, V_{IN} .....–0.3V to +34V
AGND to PGND .....–0.3V to +0.3V
Continuous Power Dissipation (T_A = 25°C) (2) ..... 3.9 W
Junction Temperature ..... 150°C
Lead Temperature .....260°C
Storage Temperature..... –65°C to +150°C

Recommended Operating Conditions (3)

Supply Voltage V_{DD} ..... 9.5V to 36V
Operating Junction Temp. (T_J). ..... -40°C to +125°C

Thermal Resistance (4) θ_{JA} θ_{JC}

TSSOP28F-EP	32	6 °C/W
TSSOP28F-EPR	..	6 °C/W

The TSSOP28F-EPR is not intended to be used without a heatsink. Therefore, $R_{\theta JA}$ of TSSOP28F-EPR is not specified.

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J (MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by P_D (MAX) = (T_J (MAX)-T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD51-7, 4-layer PCB.

ELECTRICAL CHARACTERISTICS (5, 6)

V_{DD} = 24V, V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Standby Current		V_{EN} = 0V,REF=IN=Float		120	140	μA
Quiescent Current	I_Q	SW=Low		3	4	mA
SW ON Resistance		Sourcing and Sinking		0.1	0.15	Ω
Short-Circuit Current		Sourcing and Sinking	6.2	8.5		A
EN Enable Threshold Voltage		V_{EN} Rising		1.4	2.0	V
		V_{EN} Falling	0.4	1.0		V
EN Enable Input Current		V_{EN} = 5V		5		μA
External Under-Voltage Detection	V_{UVP}		2	2.2	2.4	V
External Under-Voltage Detection Hysteresis Voltage	V_{Hys}			0.3		V
Thermal Shutdown Trip Point (7)		T_J Rising		150		°C
Thermal Shutdown Hysteresis(7)				20		°C
Thermal Warning Trip Point(7)				125		°C
Thermal Warning Hysteresis(7)				10		°C

Notes:

5) The device is not guaranteed to function outside its operating rating.
6) Electrical Characteristics are for the IC only with no external components except bypass capacitors.
7) Not production tested.

OPERATING SPECIFICATIONS (8)

Circuit of Figure 6, Single-Ended Output Configuration; V_{DD} = 34V, Gain=8.2V/V; V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Standby Current		V_{EN} = 0V			120		μA
Quiescent Current		Switching, no load			29		mA
Power Output		f = 1kHz, THD+N = 10%, 4Ω Load			41		W
		f = 1kHz, THD+N = 1%, 4Ω Load			32		W
		f = 1kHz, THD+N = 10%, 8Ω Load			22		W
		f = 1kHz, THD+N = 1%, 8Ω Load			17		W
THD + Noise		P_{OUT} = 1W, f = 1kHz, 4Ω Load			0.05		%
		P_{OUT} = 1W, f = 1kHz, 8Ω Load			0.03		%
Efficiency		f = 1kHz, P_{OUT} = 41W, 4Ω Load			91		%
		f = 1kHz, P_{OUT} = 22W, 8Ω Load			95		%
Maximum Power Bandwidth					20		kHz
Dynamic Range					102		dB
Noise Floor		A-Weighted			90		μV
Power Supply Rejection		V_{RIPPLE}=300mV_{PP} C_R=100μF	f = 1k Hz		-60		dB
			f = 217 Hz		-60		dB

Circuit of Figure 7, BTL Output Configuration; V_{DD} = 34V, Gain=15V/V; V_{EN} = 5V, T_A = 25°C, unless otherwise noted.

Parameters	Symbol	Condition		Min	Typ	Max	Units
Standby Current		V_{EN} = 0V			120		μA
Quiescent Current		Switching, no load			32		mA
Power Output		f = 1kHz, THD+N = 10%, 6Ω Load			108		W
		f = 1kHz, THD+N = 1%,6Ω Load			83		W
THD+ Noise		P_{OUT} = 1W, f = 1kHz, 6Ω Load			0.06		%
		P_{OUT} = 1W, f = 1kHz, 8Ω Load			0.04		%
Efficiency		f = 1kHz, P_{OUT} = 108W, 6Ω Load			91		%
		f = 1kHz, P_{OUT} = 84W, 8Ω Load			95		%
Maximum Power Bandwidth					20		kHz
Dynamic Range					105		dB
Noise Floor		A-Weighted			120		μV
Power Supply Rejection		V_{RIPPLE}=300mV_{PP}	f = 1k Hz		-60		dB
			f = 217 Hz		-60		dB

Note:

8) Operating Specifications are for the IC in Typical Application circuit (Figure 6 and Figure 7).

PIN FUNCTIONS

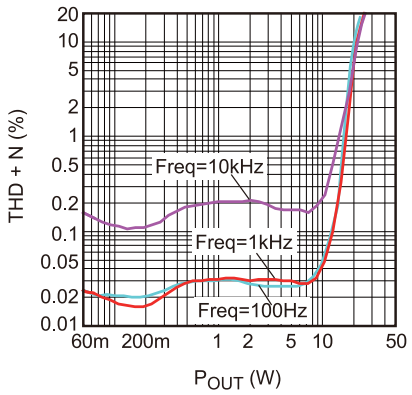
EP on Bottom Pin #	EP on Top Pin #	Name	Description
1	14	OTW	Over Temperature Warning. A low output at OTWB indicates that the die temperature rises above 125°C. This output is open drain.
2	13	FAULT	Fault Output. A low output at FAULT indicates that the IC has detected an over-temperature or over-current condition. This output is open drain.
3, 12	3, 12	N/C	Not Connected.
4	4	TIMER1	Internal Timer Input for Amplifier 1. A capacitor from TIMER1 to AGND sets the internal timer which is used for start-up pop elimination.
5	5	IN1	Inverting Input for Amplifier 1 .
6	6	REF1	Internal Analog Reference (VDD/2) for Amplifier 1. For SE configuration, connect a bypass capacitor from REF1 to AGND (10μF).
7	7	AGND1	Analog Ground for Amplifier 1. Connect AGND1 to AGND2. Connect PGND to AGND at a single point.
8	8	AGND2	Analog Ground for Amplifier 2. Connect AGND2 to AGND1.
9	9	REF2	Internal Analog Reference (VDD/2) for Amplifier 2. For BTL configuration, connect a bypass capacitor from REF2 to AGND (10μF).
10	10	IN2	Inverting Input for Amplifier 2.
11	11	TIMER2	Internal Timer Input for Amplifier 2. Use a capacitor from TIMER2 to AGND to set the internal timer for start-up pop elimination.
13	2	UVP	Under-Voltage Protection Reference Input.
14	1	EN	Enable Input for Amplifier 1. Drive EN1 high to turn on the Amplifier 1, low to turn it off.
15	15	BST2	High-Side MOSFET Bootstrap Input for Amplifier 2. Connect a capacitor from BST2 to SW2 to supplies the gate drive to the internal High-Side MOSFET.
16, 17	16, 17	PGND2	Power Ground for Amplifier 2. Connect PGND2 to PGND1.
18, 19	18, 19	SW2	Switched Power Output for Amplifier 2.
20, 21	20, 21	VDD2	Power Supply Input for Amplifier 2. Bypass VDD2 to PGND2 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the VDD2 and PGND2 pins.
22, 23	22, 23	VDD1	Power Supply Input for Amplifier 1. Bypass VDD1 to PGND1 with a 1μF X7R capacitor (in addition to the main bulk capacitor), placed close to the VDD1 and PGND1 pins.
24, 25	24, 25	SW1	Switched Power Output for Amplifier 1.
26,27	26,27	PGND1	Power Ground for Amplifier 1. Connect PGND1 to PGND2. Connect PGND to AGND at a single point.
28	28	BST1	High-Side MOSFET Bootstrap Input for Amplifier 1. A capacitor from BST1 to SW1 supplies the gate drive current to the internal High-Side MOSFET.

TYPICAL PERFORMANCE CURVES

Circuit of Figure 6, single-ended output configuration, V_{DD}=34V, V_{EN}=5V, A_V=8.2V/V, T_A = +25°C, unless otherwise noted.

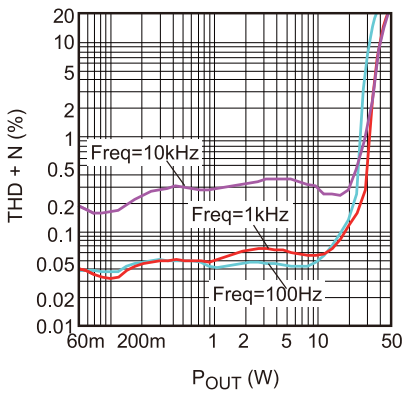
THD+N vs. Pout

V_{DD}=.34V, R_{LOAD}=8Ω (SE)



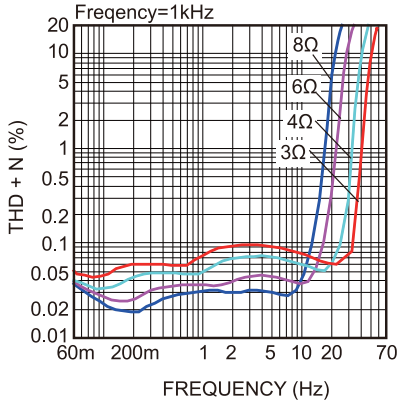
THD+N vs. Pout

V_{DD}=34V, R_{LOAD}=4Ω (SE)



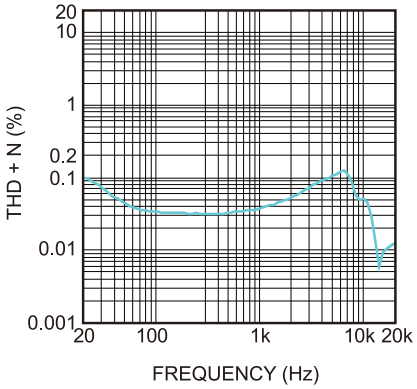
THD+N vs. Pout

V_{DD}=34V, R_{LOAD}=3Ω, 4Ω, 6Ω, 8Ω (SE)
Freqency=1kHz



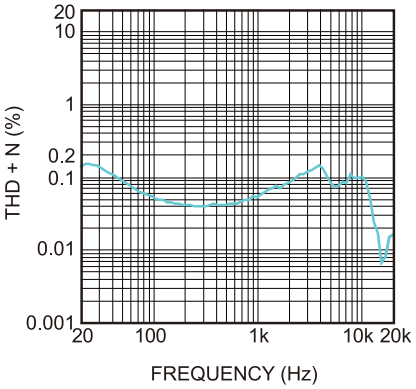
THD+N vs. Frequency

V_{DD}=34V, R_{LOAD}=8Ω (SE), P_{OUT}=1W



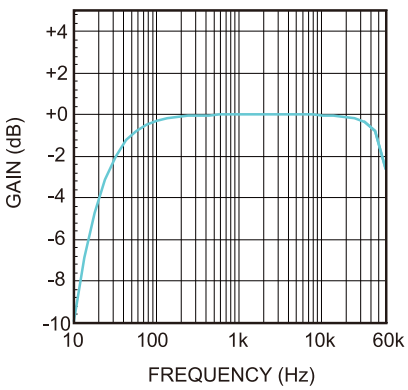
THD+N vs. Frequency

V_{DD}=34V, R_{LOAD}=4Ω (SE), P_{OUT}=1W



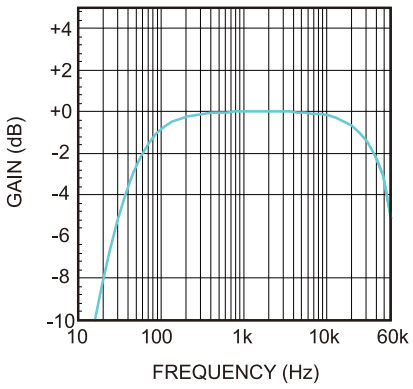
Frequency Response

V_{DD}=34V, R_{LOAD}=8Ω (SE), P_{OUT}=1W



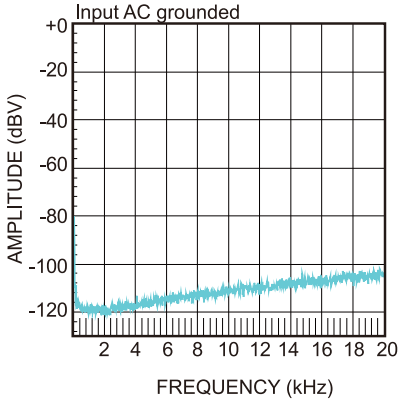
Frequency Response

V_{DD}=34V, R_{LOAD}=4Ω (SE), P_{OUT}=1W



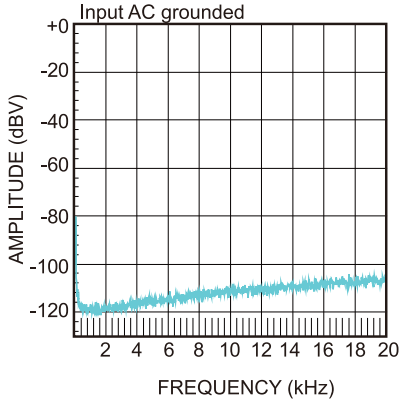
FFT Noise Floor

V_{DD}=34V, R_{LOAD}=8Ω (SE),
Input AC grounded



FFT Noise Floor

V_{DD}=34V, R_{LOAD}=8Ω (SE),
Input AC grounded

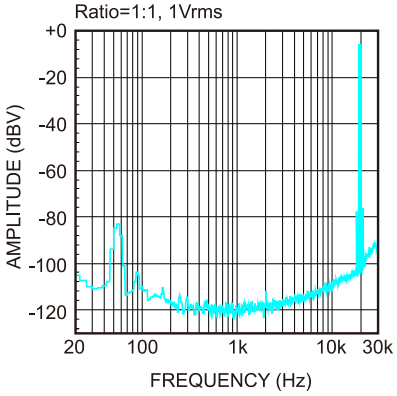


TYPICAL PERFORMANCE CURVES *(continued)*

Circuit of Figure 6, single-ended output configuration, V_{DD}=34V, V_{EN}=5V, A_V=8.2V/V, T_A = +25°C, unless otherwise noted.

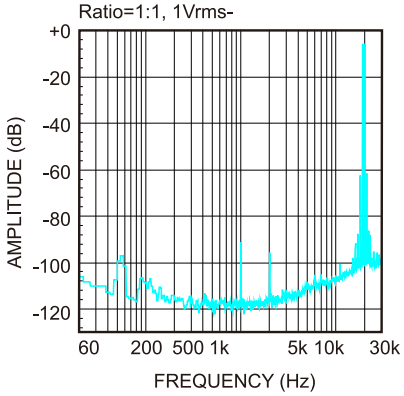
IMD Test

V_{DD} = 34V, R_{LOAD} =8Ω (SE),
Test Tones: 19kHz and 20kHz
Ratio=1:1, 1Vrms



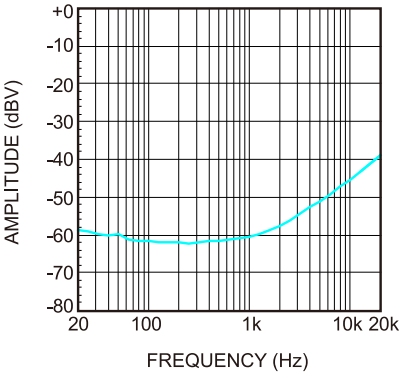
IMD Test

V_{DD} = 34V, R_{LOAD} =4Ω (SE),
Test Tones: 19kHz and 20kHz
Ratio=1:1, 1Vrms-



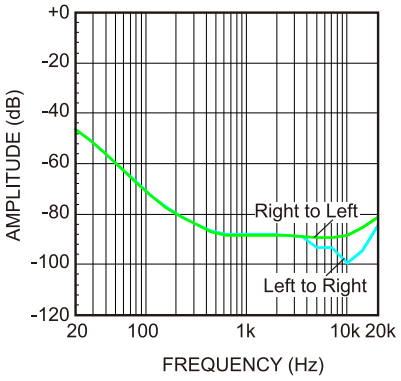
Power Supply Rejection Ratio

V_{DD}=34V, Av=8.2, R_{LOAD}=8Ω (SE),
V_{RIPPLE}=0.3V_{PP},SE, C_R=100µF,
Input AC grounded



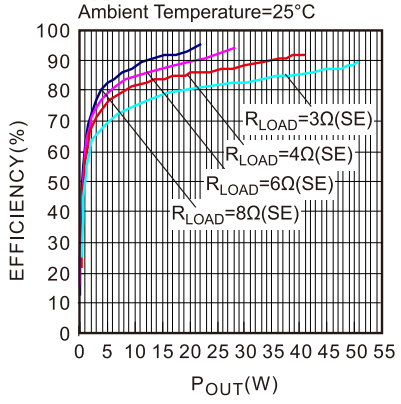
Cross Talk

V_{DD}=34V, R_{LOAD}=8Ω (SE), P_{OUT}=5W



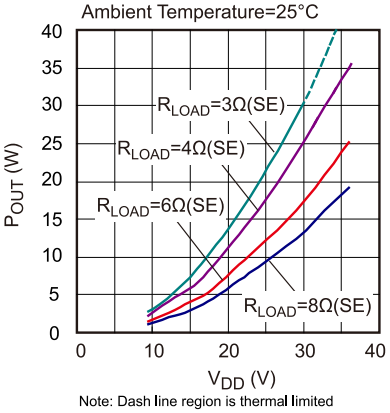
P_{OUT} vs. Efficiency

V_{DD} = 34V, 1kHz,
Ambient Temperature=25°C



P_{OUT} vs. V_{DD}

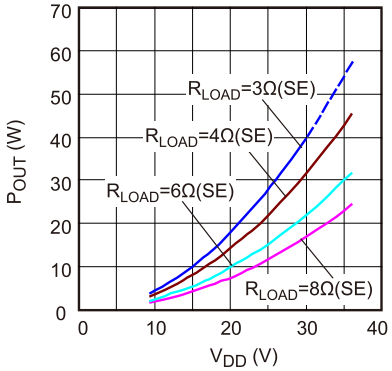
1kHz, THD=1%,
Ambient Temperature=25°C



Note: Dash line region is thermal limited

P_{OUT} vs. V_{DD}

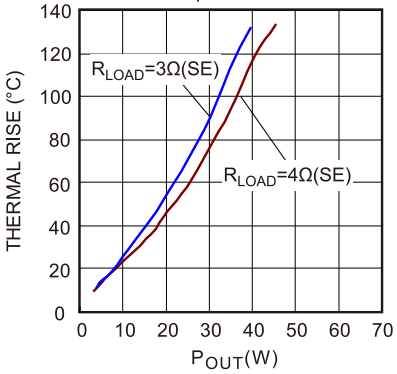
1kHz, THD=10%,
Ambient Temperature=25°C



Note: Dash line region is thermal limited

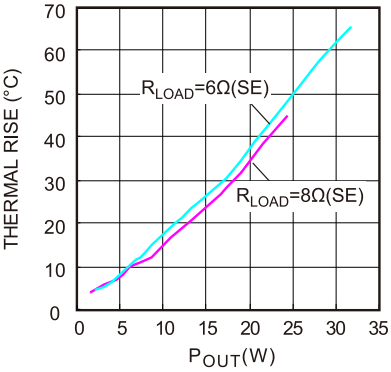
P_{OUT} vs. Thermal Rise

1kHz, THD=10%,
Ambient Temperature=25°C



P_{OUT} vs. Thermal Rise

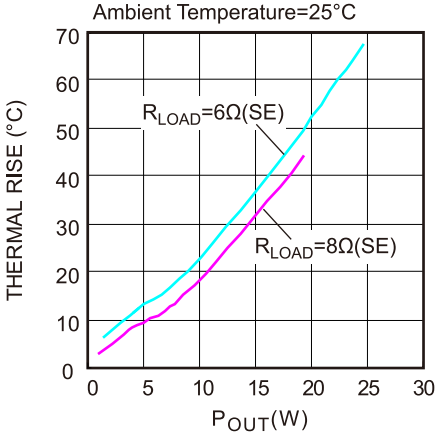
1kHz, THD=10%,
Ambient Temperature=25°C



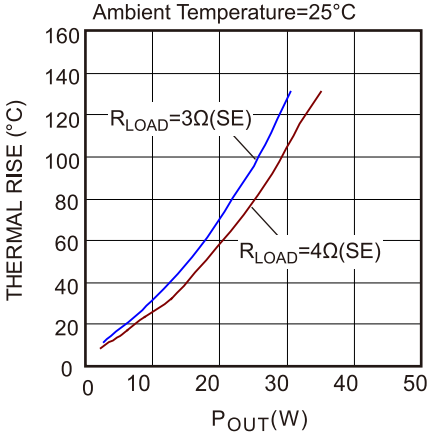
TYPICAL PERFORMANCE CURVES *(continued)*

Circuit of Figure 6, single-ended output configuration, V_{DD}=34V, V_{EN}=5V, A_V=8.2V/V, T_A = +25°C, unless otherwise noted.

P_{OUT} vs. Thermal Rise
1kHz, THD=1%,
Ambient Temperature=25°C



P_{OUT} vs. Thermal Rise
1kHz, THD=1%,
Ambient Temperature=25°C

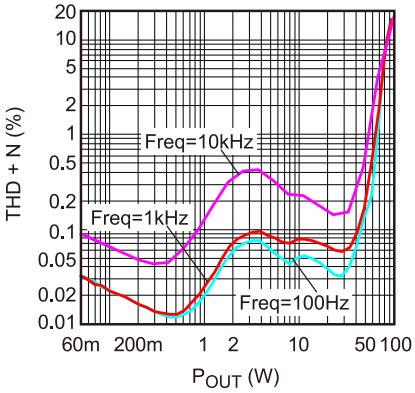


TYPICAL PERFORMANCE CURVES *(continued)*

Circuit of Figure 7, bridge-tied-load output configuration, V_{DD}=34V, V_{EN}=5V, A_V=15V/V, T_A = +25°C, unless otherwise noted.

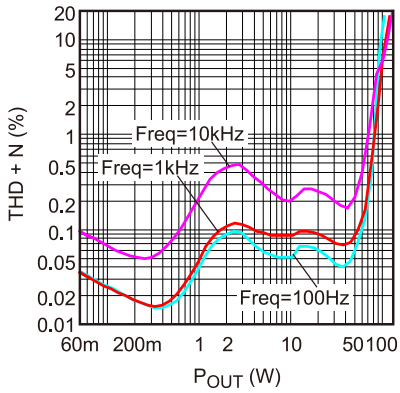
THD+N vs. Pout

V_{DD}=.34V, R_{LOAD}=8Ω (BTL)



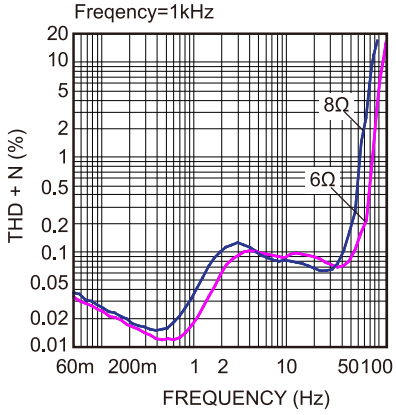
THD+N vs. Pout

V_{DD}=34V, R_{LOAD}=6Ω (BTL)



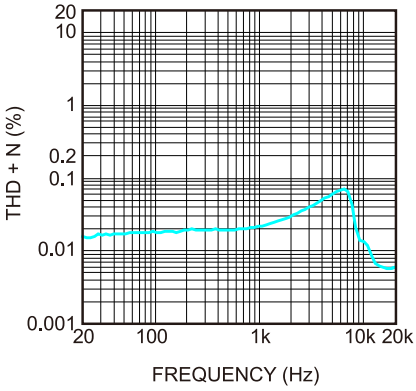
THD+N vs. Pout

V_{DD}=34V, R_{LOAD}=6Ω, 8Ω (BTL)
Freqency=1kHz



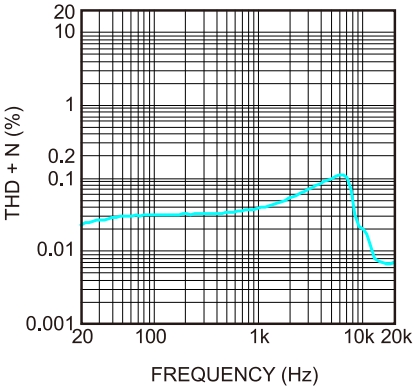
THD+N vs. Frequency

V_{DD}=34V, R_{LOAD}=8Ω (BTL), P_{OUT}=1W



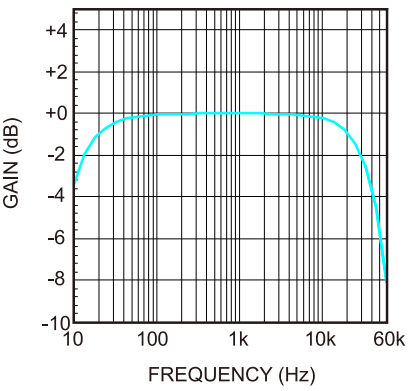
THD+N vs. Frequency

V_{DD}=34V, R_{LOAD}=6Ω (BTL), P_{OUT}=1W



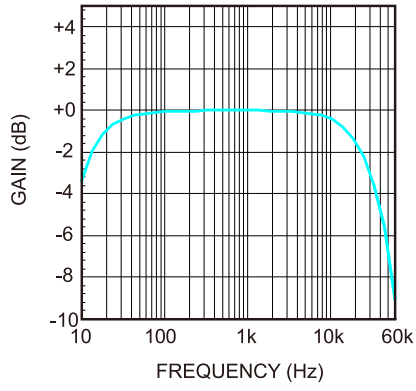
Frequency Response

V_{DD}=34V, R_{LOAD}=8Ω (BTL), P_{OUT}=1W



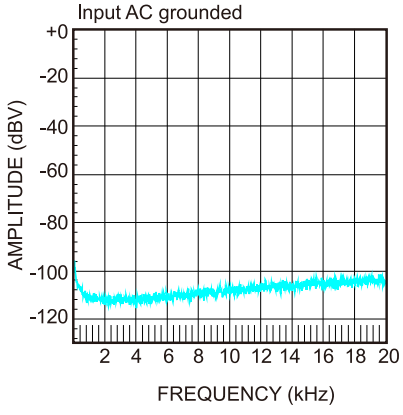
Frequency Response

V_{DD}=34V, R_{LOAD}=6Ω (BTL), P_{OUT}=1W



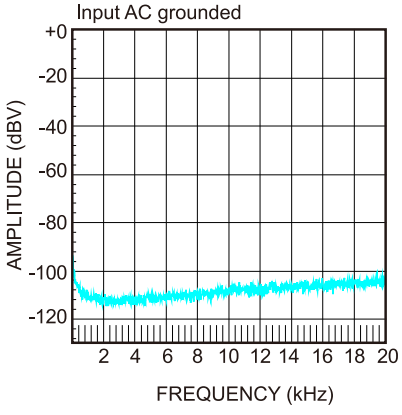
FFT Noise Floor

V_{DD}=34V, R_{LOAD}=8Ω (BTL),
Input AC grounded



FFT Noise Floor

V_{DD}=34V, R_{LOAD}=6Ω (BTL),
Input AC grounded

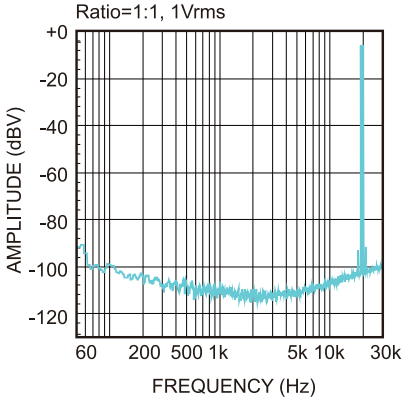


TYPICAL PERFORMANCE CURVES *(continued)*

Circuit of Figure 7, bridge-tied-load output configuration, V_{DD}=34V, V_{EN}=5V, A_V=15V/V, T_A = +25°C, unless otherwise noted.

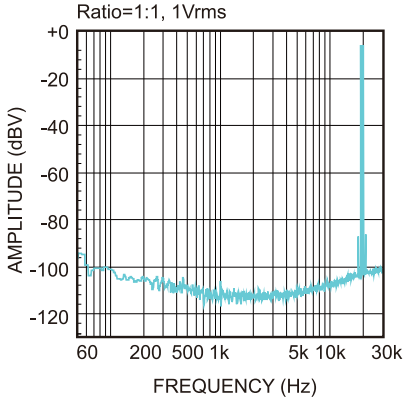
IMD Test

V_{DD} = 34V, R_{LOAD} =8Ω (BTL),
Test Tones: 19kHz and 20kHz
Ratio=1:1, 1Vrms



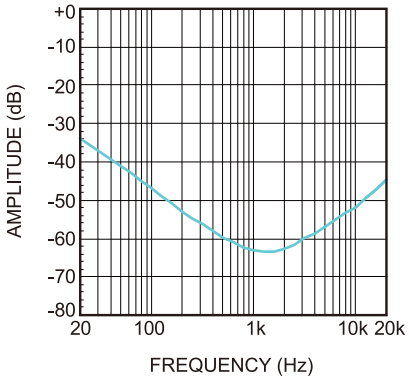
IMD Test

V_{DD} = 34V, R_{LOAD} =6Ω (BTL),
Test Tones: 19kHz and 20kHz
Ratio=1:1, 1Vrms



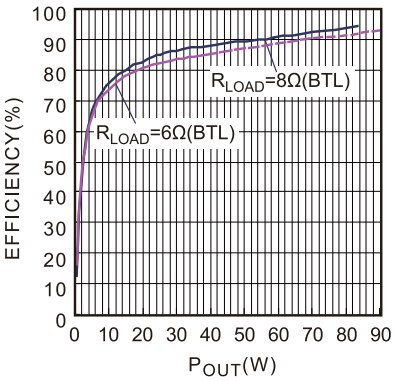
Power Supply Rejection Ratio

V_{DD}=34V, Av=15, R_{LOAD}=8Ω (BTL),
V_{RIPPLE}=0.3V_{PP},SE, C_R=100µF,
Input AC grounded



P_{OUT} vs. Efficiency

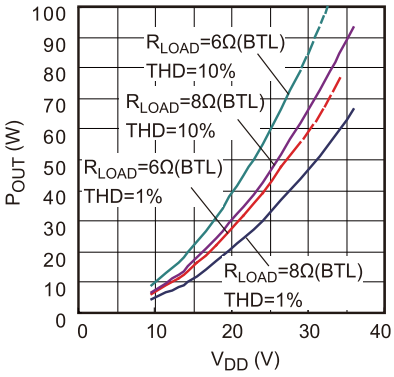
V_{DD} = 34V,
Input Signal Frequency=1kHz



Note: Dash line region is thermal limited

P_{OUT} vs. V_{DD}

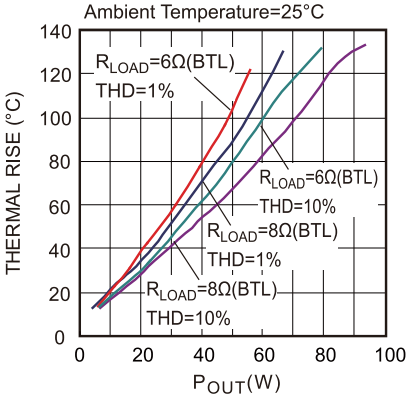
1kHz,
Ambient Temperature=25°C



Note: Dash line region is thermal limited

P_{OUT} vs. Thermal Rise

1kHz,
Ambient Temperature=25°C



FUNCTIONAL BLOCK DIAGRAM

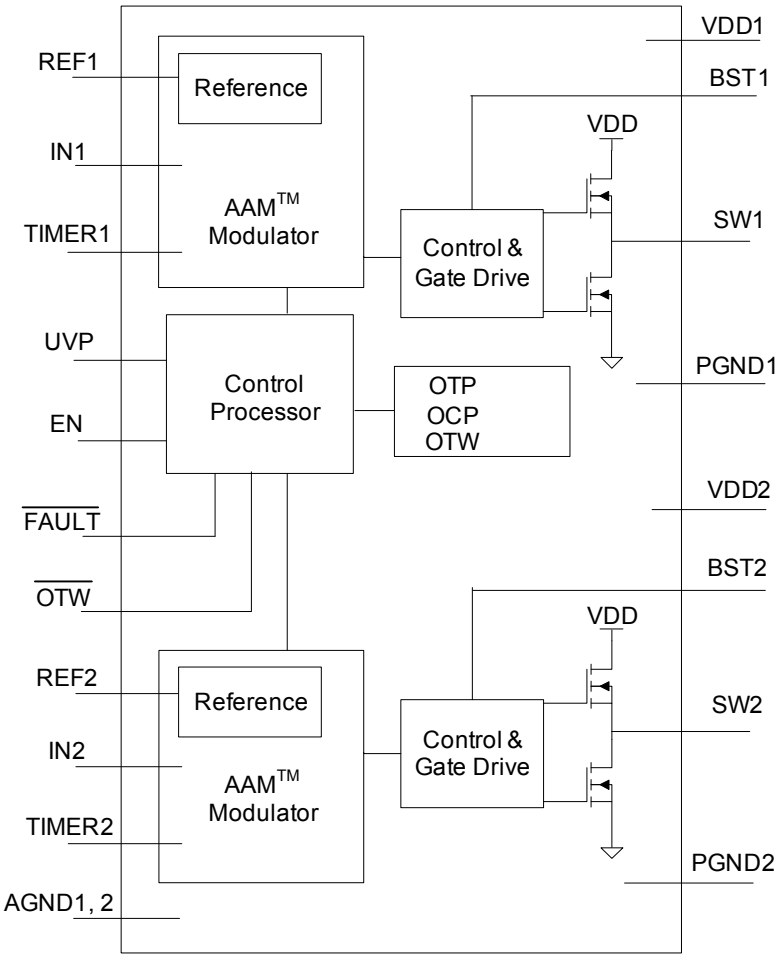


Figure 1: Functional Block Diagram

OPERATION

The MP7770 is a Class D Audio Amplifier that drives stereo speakers in single-ended configuration or a mono speaker in bridge-tied-load configuration. It uses MPS's patented Analog Adaptive Modulation™ technology to convert the audio input signal into pulses. These pulses drive an internal high-current output stage and—when filtered through an external inductor-capacitor filter—reproduce the input signal across the load. Because of the switching Class D output stage, power dissipation in the amplifier is drastically reduced when compared against Class A, B or A/B amplifiers, and maintains high fidelity with low distortion.

REF1 and REF2 are the positive inputs of the two amplifiers. They are set to half the DC power supply input voltage (V_{DD}/2) by the internal circuit. The input capacitor C_{IN} decouples the AC signal at the input.

The input resister R_{IN} and the feedback resistor R_{FB} set the amplifier voltage gain as calculated by the equation:

$$AV = \frac{-R_{FB}}{R_{IN}}$$

Where:

- Channel 1: R_{FB}=R_{FB1} and R_{IN}=R_{IN1}
- Channel 2: R_{FB}=R_{FB2} and R_{IN}=R_{IN2}.

The MP7770 includes four high-power MOSFETs; For each channel, the output driver stage uses two 100mΩ N-channel MOSFETs to deliver pulses to the LC output filter to drive the load. To enhance the high-side MOSFET (HS-FET), the gate is driven to a voltage higher than the source by the bootstrap capacitor between SW and BS. When the output is low, the bootstrap capacitor is charged from V_{DD} through an internal circuit on the MP7770. The gate of the HS-FET is driven high by the BST voltage, forcing the MOSFET gate to a voltage higher than V_{DD}, thus allowing the MOSFET to turn on and reducing amplifier power loss.

Pop Elimination

When used in a single-ended output configuration, the capacitors C_{OUT1} and C_{OUT2} block the DC signal and pass the AC signals to the load. To insure that the amplifier only passes low-frequency signals, the time constant of C_{OUT}*R_{LOAD} is large. However, when EN goes high, the capacitor charges over a long period and can result in turn-on/turn-off "pop" In typical amplifiers.

The MP7770 integrates a source-current function to charge the DC block capacitors C_{OUT1} and C_{OUT2} and C_{IN1} and C_{IN2} at start-up. Two internally-generated currents flow to the SW pin ($I_{initialization\_SW}$) and the IN pin ($I_{initialization\_IN}$) during start-up, which helps to eliminate turn-on pop. The rising/falling slew rate of the SW node start-up current ($I_{initialization\_SW}$) is out of audio band (means rise and falling gradually), can be adjusted from the timer capacitor C_{TIMER} and the voltage of SW node; The larger the C_{TIMER} capacitance, the smaller the slew rate of the $I_{initialization\_SW}$.

After driving the EN pin low, the output SW immediately switches to high impedance to eliminate turn-off pop.

Short Circuit/Overload Protection and Monitoring

The MP7770 is fully-protected against over-current and thermal overload conditions as explained below and \shown in Figure2.

Short Circuit/Overload Protection

The MP7770 has internal overload and short-circuit protection. The currents in both the high-side and low-side MOSFETs (LS-FETs) are measured and if the current exceeds the short circuit current limit (typically 8A), both MOSFETs will be turned off for a fixed duration (around 1ms) before resuming normal operation. After the fixed duration and the short circuit condition is removed, the MP7770 will restart with the start-up sequence that is used for normal starting to prevent a pop from occurring.

Over-Temperature Shutdown

Thermal monitoring is also integrated into the MP7770. If the die temperature rises above 150°C, all switches turn off. The temperature must fall below 130°C before normal operation resumes, with the same power-up sequence used to prevent popping noise.

Over-Temperature Warning Output

The MP7770 includes an open drain, active low fault indicator output to act as an over-temperature warning (OTW). The OTW pin is asserted when the die temperature reaches 125°C and goes low until the temperature drops below 115°C.

Do not apply more than 6V to the OTW pin.

Fault Output

The MP7770 includes an open drain, active low fault indicator output on the FAULTB pin. A fault triggers if either the current limit or thermal shutdown is tripped.

A fault on any channel will cause the FAULTB pin to pull low. A fault on either channel will cause the all outputs to go into high impedance. When the fault goes away, the MP7770 will resume normal operation.

Do not apply more than 6V to the FAULTB pin.

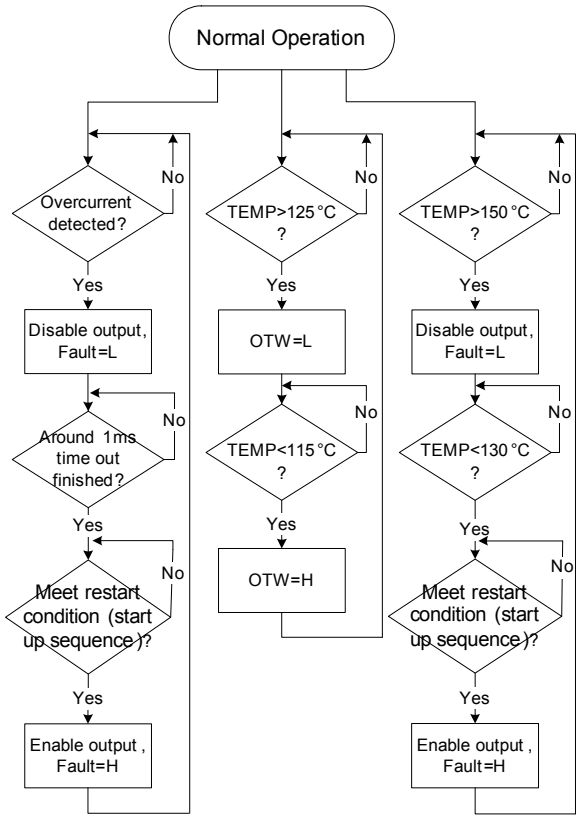


Figure 2: Fault Timing Chart

Enable Function

The MP7770 EN input is an active-high–enable control. To enable the MP7770, drive EN with a voltage 2.0V or higher; to disable the amplifier, drive it below 0.4V. While the MP7770 is disabled, the VDD operating current is around 250μA and the output driver MOSFETs are turned off.

Programmable UVP

MP7770 integrate programmable UVP function, which can be used to shutdown the MP7770 to escape the pop, by controlling the UVP node voltage. The VDD shutdown voltage can be flexibly adjusted by the external resistor, as shown in the figure 3.

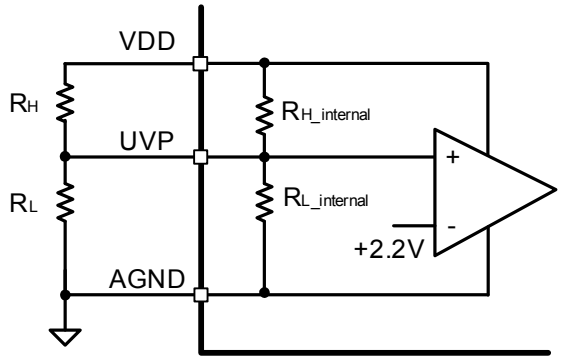


Figure 3: UVP Block Diagram

If external resistor R_H and R_L is low enough (e.g. R_H, R_L < 50kΩ) compared with internal resistor, the VDD shutdown voltage (rising threshold) can be calculated by the equation:

$$V_{VDD\_shutdown} \approx 2.2 * \frac{(R_H + R_L)}{R_L}$$

If the UVP pin is NC, the default VDD shutdown voltage (rising threshold) is 8.4V since there is internal voltage divided circuit.

For example, please see the table 1 for recommended UVP setting for reduce the power off pop.

Table 1

VDD (V)	VDD_shutdown (V)	R_H	R_L
12	8.6	15k	5.1k
24	19	39k	5.1k
36	26	56k	5.1k

Thermal Information

The MP7770 is available in a thermally-enhanced TSSOP28 package. The user can choose between two package options, with the exposed pad on top or bottom.

The thermally-augmented TSSOP-EPR package with the exposed pad on top is designed to interface directly with heat sinks using a thermal interface compound. The heat sink then absorbs heat from the ICs and couples it to the local air. If louvers or fans are used, this process can reach equilibrium and heat can be continually removed from the ICs. Because of the efficiency of the MP7770, heat sinks can be smaller than those required for linear amplifiers.

The TSSOP28-EPR is not intended for use without a heatsink. For cases without a heatsink, please use the TSSOP28-EP with the exposed pad on the bottom.

APPLICATION INFORMATION

Component Selection

The MP7770 uses a minimal number of external components to complete a stereo SE or mono BTL Class D audio amplifier. The circuit in Figure 6 (stereo SE application circuit) and Figure 7 (mono BLT application circuit) are optimized for a 24V power supply. This circuit should be suitable for most applications. Use the following sections to design custom circuits.

Setting the Voltage Gain

The maximum output-voltage swing is limited by the power supply. To achieve the maximum output power, set the gain such that the maximum input signal results in the maximum output voltage swing.

For a single-ended (SE) output configuration, the maximum output voltage $V_{OUT(PK)}$ is $V_{DD}/2$. For a bridge-tied-load (BTL) output configuration, the maximum output voltage $V_{OUT(PK)}$ is V_{DD}. For a given input signal voltage, where $V_{IN(PK)}$ is the peak input voltage, the maximum voltage gain is:

$$A_V(MAX) = \frac{V_{OUT(PK)}}{V_{IN(PK)}}$$

This voltage-gain setting results in the peak output voltage approaching its maximum for the maximum input signal. In some cases the amplifier is allowed to overdrive slightly, allowing the THD to increase at high power levels, and so a higher gain than A_V (max) is required.

Setting the Switching Frequency

The idle switching frequency (the switching frequency when no audio input is present) is a function of several variables: The supply voltage V_{DD}, the integral capacitor C_{INT} and the feedback resistor R_{FB}. Lower switching frequencies result in greater inductor ripple, causing more quiescent output voltage ripple, and increasing the output noise and distortion. Higher switching frequencies result in greater power loss. The optimum quiescent switching frequency is approximately 600kHz. When used to drive stereo speakers in single-ended configuration, set right channel to an idle switching frequency greater than 50kHz plus the left channel's switching frequency by using a different timing capacitor C_{INT}. For details, refer to the Table 2 for recommended SE output configuration design, and Table 3 for recommended BTL output configuration design.

Table 2: Switching Frequency Setting For SE Output Configuration

V_{DD} (V)	Gain (V/V)	R_{FB} (kΩ)	R_{IN} (kΩ)	Left channel		Right channel	
				C_{INT1} (nF)	F_{SW1} (kHz)	C_{INT2} (nF)	F_{SW2} (kHz)
12	10	100	10	2.2	635	1.8	705
12	20	100	4.99	2.2	635	1.8	705
24	10	75	7.5	5.6	700	4.7	740
24	20	150	7.5	2.2	780	2.7	665
30	10	51	5.1	8.2	780	10	680
30	20	150	7.5	3.3	710	2.7	780
30	30	150	4.99	3.3	710	2.7	780
34	10	51	5.1	10	785	12	610
34	20	100	4.99	4.7	780	5.6	740
34	30	150	4.99	3.9	700	3.3	775

Table 3: Switching Frequency Setting for BTL Output Configuration

V_{DD} (V)	Gain (V/V)	R_{FB} (kΩ)	R_{IN} (kΩ)	C_{INT1} (nF)	F_{SW1} (kHz)
12	10	100	10	2.2	435
12	20	100	4.99	2.2	435
12	30	150	4.99	1.0	440
24	10	100	10	3.3	490
24	20	100	4.99	2.2	570
24	30	150	4.99	1.5	480
30	10	100	10	2.2	465
30	20	100	4.99	3.3	535
30	30	150	4.99	2.2	450
34	10	100	10	3.3	560
34	20	100	4.99	3.3	560
34	30	150	4.99	2.2	470

Choosing the Output LC Filter

The inductor-capacitor (LC) filter converts the pulses at SW to the output voltage that drives the speaker. There are two kinds of LC filter structure depending on the output configuration.

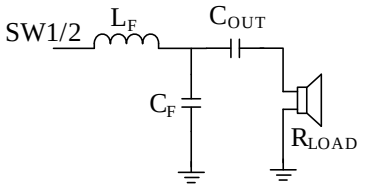


Figure 4: SE Filter Configuration

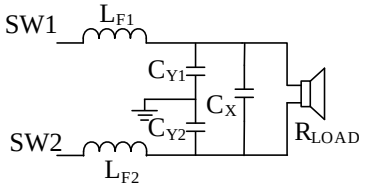


Figure 5: BTL Filter Configuration

Where:

$$L_F = L_{F1} + L_{F2},$$

$$C_F = C_X + \frac{C_{Y1} \times C_{Y2}}{C_{Y1} + C_{Y2}},$$

$$L_{F1} = L_{F2};$$

$$C_{Y1} = C_{Y2}$$

The characteristic frequency of the LC filter needs to be high enough to allow high frequency audio to the output, yet needs to be low enough to filter out high frequency products of the pulses from the SW pin. The characteristic frequency of the LC filter is:

$$f_0 = \frac{1}{2 \times \pi \times \sqrt{L_F \times C_F}}$$

The quality factor (Q) of the LC filter is important: If this is too low, output noise will increase; if this is too high, then peaking may occur at high frequencies and reduce the passband flatness. The circuit Q is set by the load resistance (speaker resistance, typically 4Ω or 8Ω). Q is calculated as:

$$Q = \frac{R_{LOAD}}{\omega_0 \times L_F} = \frac{R_{LOAD}}{2\pi \times f_0 \times L_F}$$

ω_0 is the characteristic frequency in radians/second and f_0 is in Hz. Use an LC filter with Q between 0.7 and 1.

The type of inductor and capacitor used in the LC filter.greatly affects the output ripple and noise. Use a film capacitor and an inductor with sufficient power rating to supply the output current to the load. The inductor must exhibit soft saturation characteristics: If the inductor exhibits hard saturation, it should operate well below the saturation current. Use toroidal cores made of gapped ferrite, MPP, powdered iron, or similar materials. If using either an open or shielded bobbin ferrite core for multi-channel designs, make sure that the start windings of each inductor align (all starting toward the SW pin, or all starting toward the output) to prevent crosstalk or other channel-to-channel interference.

Output Coupling Capacitor for SE Output

The output AC coupling capacitor—C_{OUT}—serves to pass only the amplified AC signal from the LC filter to the load and to block DC signals. The combination of the coupling capacitor, C_{OUT} and the load resistance results in a first-order high-pass filter. Select C_{OUT} so that the required minimum frequency passes. The output corner frequency (-3dB point), f_{OUT}, can be calculated as:

$$f_{OUT} = \frac{1}{2 \times \pi \times R_{LOAD} \times C_{OUT}}$$

Set the output corner frequency (f_{OUT}) at or below the minimum required frequency.

The output coupling capacitor carries the full load current, so chose a capacitor such that its ripple current rating is greater than the maximum load current. Use low-ESR aluminum electrolytic capacitors for best results.

Input Coupling Capacitor

The input coupling capacitors C_{IN1} and C_{IN2} pass only the AC signal at the input. For a typical system application, the source input signal centers around the circuit ground, while the MP7770 input is at half the power supply voltage (V_{DD}/2). The input coupling capacitor transmits the AC signal from the source

to the MP7770 while blocking the DC voltage. Choose an input coupling capacitor such that the corner frequency (f_{IN}) is less than the passband frequency. The corner frequency is calculated as:

$$f_{IN} = \frac{1}{2 \times \pi \times R_{IN} \times C_{IN}}$$

Timer capacitor

The start-up source current slew rate is adjusted from the timing capacitor, C_{TIMER}: The larger the C_{TIMER} capacitance is, the smaller the start-up current slew rate is. Select a C_{TIMER} value larger than 312nF, so the start-up current slew rate would be smaller than 20mA/50ms which helps eliminate the turn-on pop. The recommended 2.2μF capacitor C_{TIMER} results in a start-up current slew rate of approximately 20mA/350ms.

Power Source

For maximum output power, the amplifier circuit requires a regulated external power source. A high power-supply voltage can deliver more power to a given load resistance, but a power-source voltage exceeding the maximum voltage of 36V can damage the MP7770. The MP7770's power supply rejection is excellent, though power-supply noise can pass to the output, so care must be taken to minimize power supply noise within the pass-band frequencies. Bypass the power supply with a large capacitor (typically aluminum electrolytic) along with a smaller 1μF ceramic capacitor at the MP7770 V_{DD} supply pins.

PCB Layout

Circuit layout is critical for optimal performance, low output distortion, and noise. Duplicate the EVB layout for best results. For layout changes, follow these guidelines and use Figure 8 as SE layout references, use Figure 9 as BTL layout reference.

1) Place the following components as close to the MP7770 as possible:

Bootstrap Capacitors
C_{BS1} and C_{BS2} supply the gate drive current to the internal HS-FET. Place C_{BS1} as close to BST1/2 pin and SW1/2 pin as possible. Likewise, place C_{BS2} as close to BST2 pin and SW2 pins as possible.

Power Supply Bypass Capacitors
C_{BYP1} and C_{BYP2} carry the transient current for the switching power stage. To avoid overstressing the MP7770 and excessive output noise, place C_{BYP1} as close to the VDD1 pins and PGND1 pins as possible, and place C_{BYP2} as close to the VDD2 pins and PGND2 pins as possible.

Integral Capacitors
C_{INT} sets the amplifier switching frequencies and are typically on the order of a few nF. Place the integral capacitor C_{INT} as close to the corresponding input as possible to reduce distortion and noise. For example, place C_{INT1} as close to pins 2 and 3 as possible at SE output configuration.

Reference Bypass Capacitors for SE Output
When used with SE output, CR1 and CR2 filter the ½ VDD reference voltages. Place C_{R1} and C_{R2} as close to the IC as possible to improve power supply rejection and reduce distortion and noise at the output.

2) The Inductor-Capacitor (LC) filter converts the pulse train at SW to the output voltage that drives the speaker. Please keep the filter capacitor close to the inductor.

3) Keep the sensitive feedback signal trace on the input side and shield the trace with the AGND plane. Make sure that any traces carrying the switch node (SW) voltages are routed far from any input signal traces. If the trace must run near the SW trace near the input, shield the input with a ground plane between the traces. Physically separate each channel to

prevent crosstalk. Make sure that all inductors used on a single circuit board have the same orientation.

Route each power supply from the source to each channel individually, not serially. This prevents channel-to-channel coupling through the power supply input.

Electro-Magnetic Interference (EMI) Considerations

Due to the switching nature of Class D amplifiers, care must be taken to minimize the effects of electromagnetic interference from the amplifier. However, proper component selection and careful attention to circuit layout can minimize the effects of the EMI due to the amplifier switching.

The power inductors are a potential source of radiated emissions. For the best EMI performance, use toroidal inductors, since the magnetic field is well-contained inside the core. However toroidal inductors can be expensive to wind. For a more economical solution, use shielded-gapped–ferrite or shielded-ferrite-bobbin-core inductors. These inductors typically do not contain the EM field as well toroidal inductors, but can achieve a better balance between good EMI performance with low cost.

The size of high-current loops that carry rapidly changing currents must be minimized: Make sure that the V_{DD} bypass capacitors are as close to the MP7770 as possible.

Nodes that carry rapidly changing voltage, such as SW, need to be made as small as possible. If sensitive traces run near a trace connected to SW, place a ground shield between the traces.

TYPICAL APPLICATION CIRCUITS

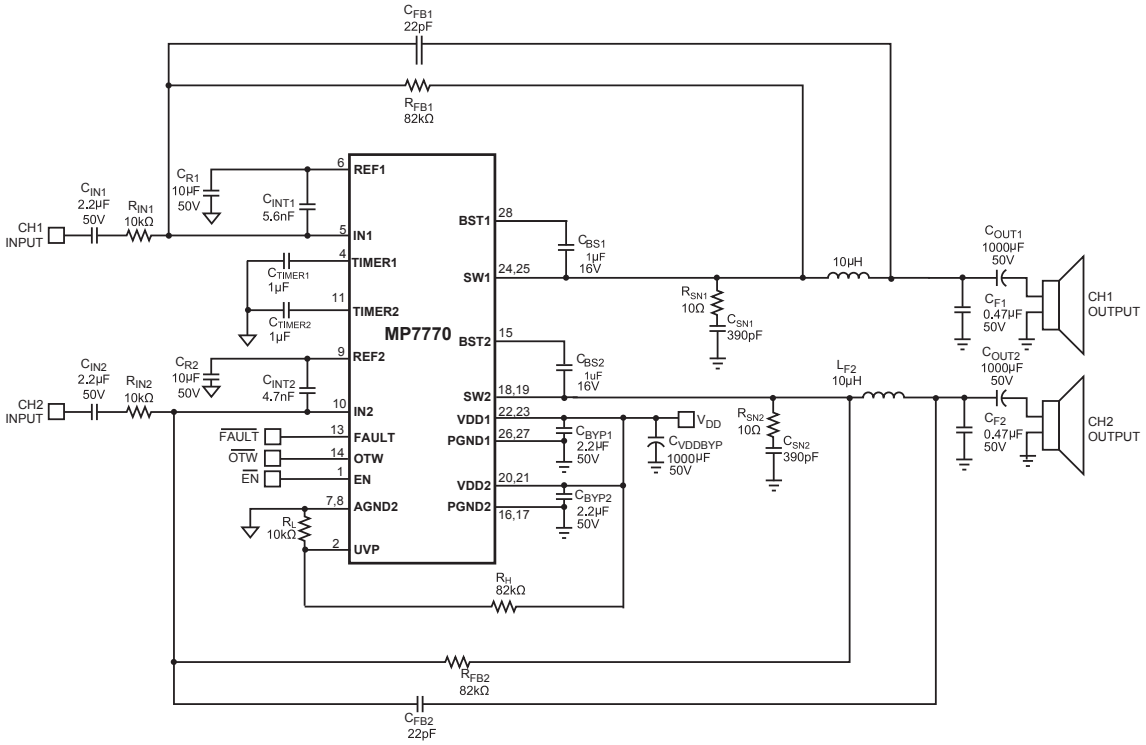


Figure 6: 24V VDD Stereo SE Typical Application Circuit

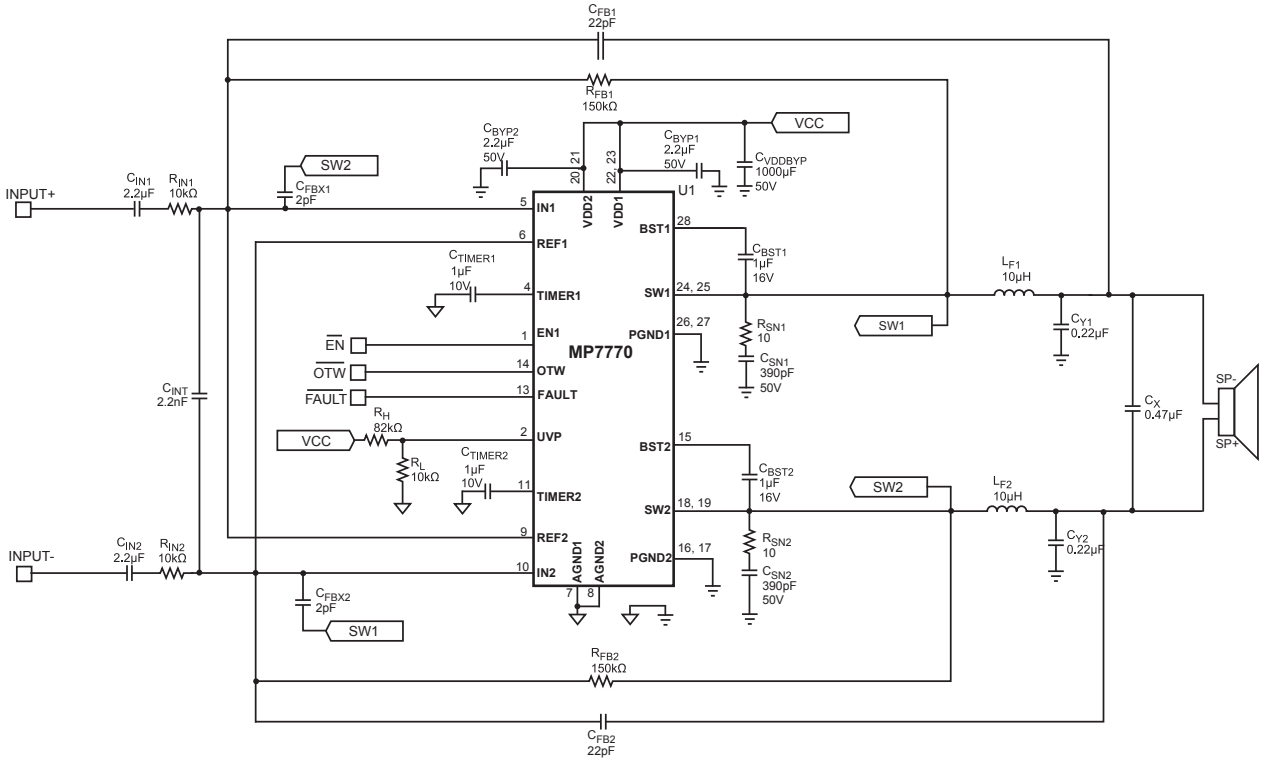
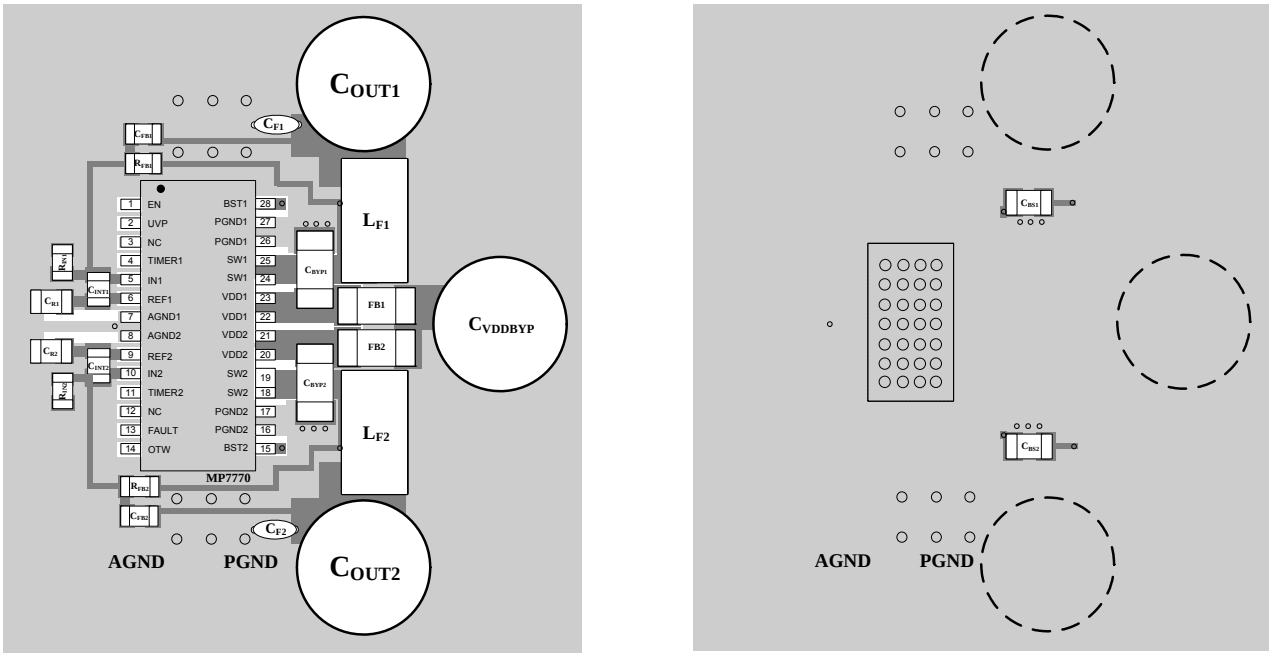
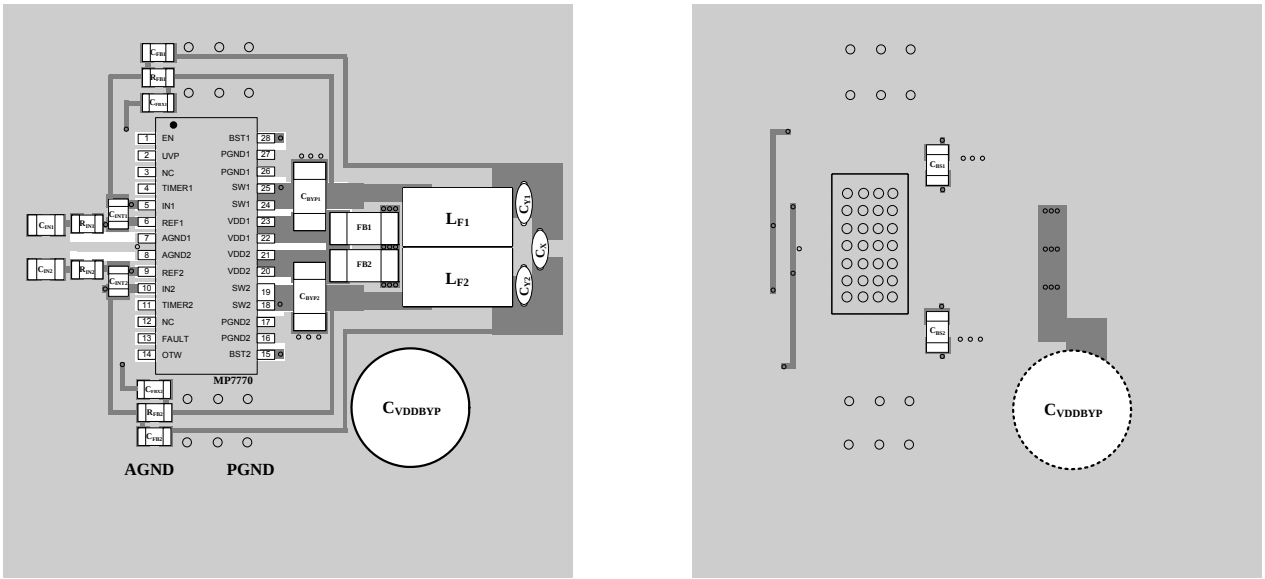


Figure 7: 24V VDD Mono BTL Typical Application Circuit



Top Bottom

Figure 8: Stereo SE Reference PCB Layout



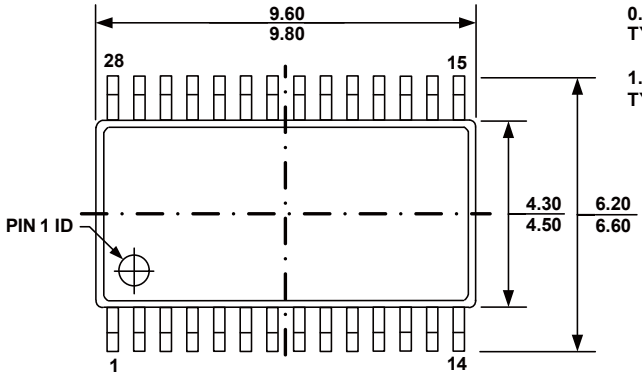
Top Bottom

Figure 9: Mono BTL Reference PCB Layout

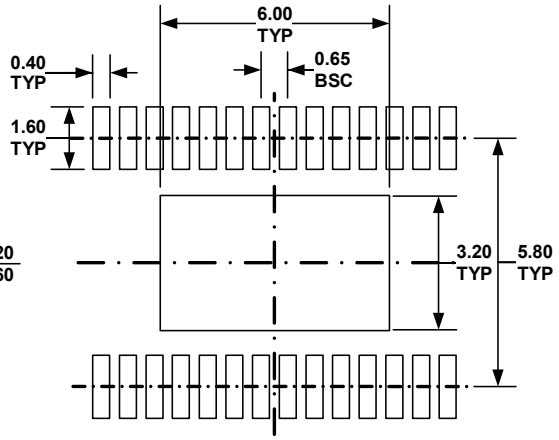
PACKAGE INFORMATION

TSSOP28-EP

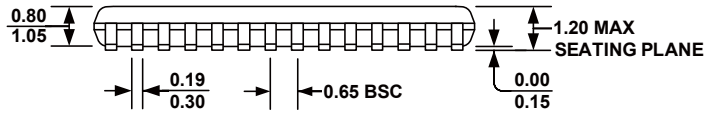
PACKAGE OUTLINE DRAWING FOR 28-TSSOP w/ EXPOSED PADDLE
MF-PO-D-0055 revision 2.0



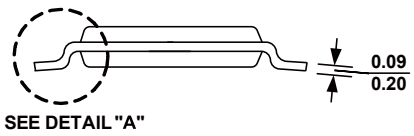
TOP VIEW



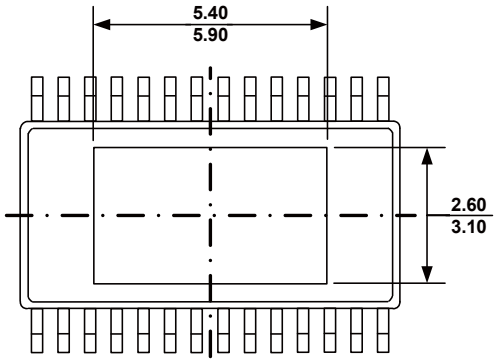
RECOMMENDED LAND PATTERN



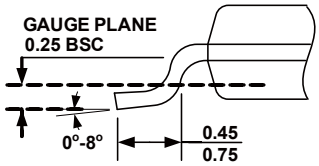
FRONT VIEW



SIDE VIEW



BOTTOM VIEW



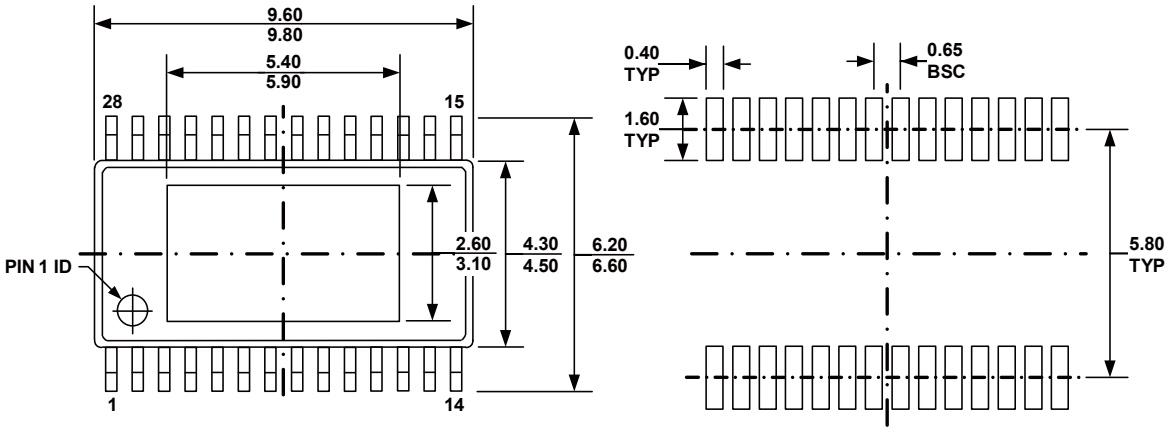
DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
5) DRAWING CONFORMS TO JEDEC MO-153, VARIATION AET.
6) DRAWING IS NOT TO SCALE

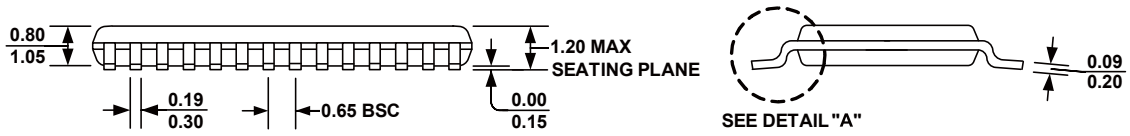
TSSOP28-EPR

PACKAGE OUTLINE DRAWING FOR 28-TSSOP w/ REVERSE EXPOSED PADDLE
MF-PO-D-0XXX preliminary



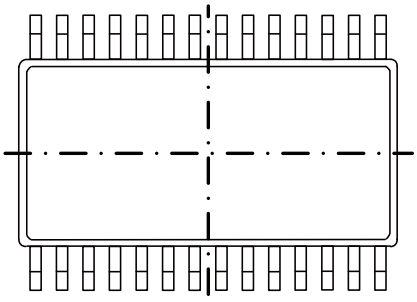
TOP VIEW

RECOMMENDED LAND PATTERN

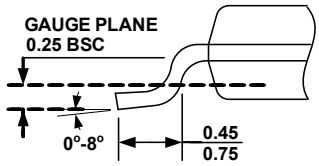


FRONT VIEW

SIDE VIEW



BOTTOM VIEW



DETAIL "A"

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) PACKAGE LENGTH DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURR
3) PACKAGE WIDTH DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION.
4) LEAD COPLANARITY(BOTTOM OF LEADS AFTER FORMING) SHALL BE 0.10 MILLIMETERS MAX
5) JEDEC REFERENCE IS MO-153.
6) DRAWING IS NOT TO SCALE