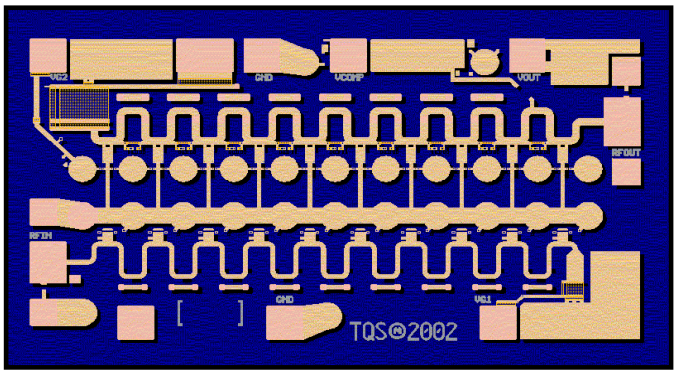
TriQuint SEMICONDUCTOR

TGA4832

DC - 35 GHz Wideband Amplifier



Key Features and Performance

- Frequency Range: DC to 35GHz Linear
- 40Gb/s Optical Modulator Driver
- 12dB Small Signal Gain
- 17 dBm Typical Output Power (4Vpp)
- 3dB Gain Adjustment
- < 15ps Edge Rates
- 4Vpp 40Gb/s NRZ PRBS Linear
- 0.15um pHEMT Technology
- Bias: Vd = 5V, Id = 135 mA
- Chip Size: 1.79 x 1.00 x 0.1 mm (0.70 x 0.39 x 0.004 in)

Product Description

The TriQuint TGA4832 is a medium power wideband AGC amplifier which operates from DC to 35 GHz. Typical small signal gain is 12dB with 3dB AGC range. Typical input and output return losses are >10dB. The TGA4832 provides 18 dBm of output power at 1 dB gain compression.

Drain bias may be applied through the output port for best efficiency or through the on-chip drain termination. Two stages in cascade demonstrate 3.8Vpp output voltage swing with 350mV at the input when stimulated with 40Gb/s 2^31-1prbs NRZ data. RF ports are DC coupled enabling the user to customize system corner frequencies. The TGA4832 requires off-chip decoupling and blocking components.

The TGA4832 is suitable for a variety of wideband electronic warfare systems such as radar warning receivers, electronic counter measures, decoys, and jammers. It is also an excellent choice for 40Gb/s NRZ applications. The TGA4832 is capable of driving an Electro-Absorptive optical Modulator (EAM) with electrical Non-Return to Zero (NRZ) data. In addition, the TGA4832 may also be used as a predriver or a receive gain block.

Bond pad and backside metallization is gold plated for compatibility with eutectic alloy attachment methods as well as the thermocompression and thermosonic wire bonding processes. Each device is 100% DC and RF tested on-wafer to ensure performance compliance. The device is available in die form.

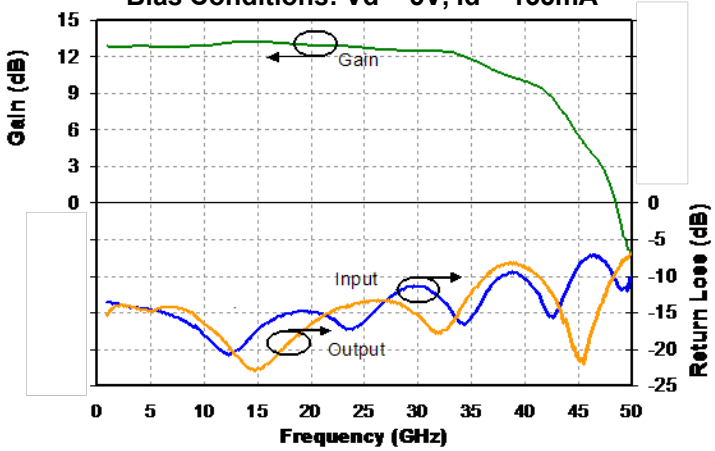
Lead Free & RoHS Compliant.

Primary Applications

- Test Equipment
- Ultra Wideband
- 40Gb/s NRZ EAM Driver
- 40Gb/s NRZ Predriver or Gain Block

Measured Performance

Bias Conditions: Vd = 5V, Id = 135mA



Datasheet subject to change without notice

TABLE I
MAXIMUM RATINGS 1/

SYMBOL	PARAMETER	V+	Vd	NOTES
	POSITIVE SUPPLY VOLTAGE			
	Biased thru On-chip Drain Termination	10.4 V	-	2/, 3/
	Biased thru the RF Output Port using a Bias Tee	-	6 V	
	POSITIVE SUPPLY CURRENT			
	Biased thru On-chip Drain Termination	135 mA	-	3/
	Biased thru the RF Output Port using a Bias Tee	-	150 mA	
	POWER DISSIPATION			
	Biased thru On-chip Drain Termination	1.4 W	-	3/, 4/
	Biased thru the RF Output Port using a Bias Tee	-	0.9 W	
	NEGATIVE GATE			
Vg	Voltage Range	+1V to –3 V		
| Ig |	Gate Current	10 mA		
	CONTROL GATE			
Vctrl	Voltage Range	Vd/2 to –3V		5/
| Ictl |	Gate Current	10 mA		
	RF INPUT			
P_{IN}	Sinusoidal Continuous Wave Power	21 dBm		
Vin	40 Gb/s PRBS Input Voltage Peak to Peak	TBD		
T_{CH}	OPERATING CHANNEL TEMPERATURE	200 °C		6/
	MOUNTING TEMPERATURE (30 SECONDS)	320 °C		
T_{STG}	STORAGE TEMPERATURE	-65 to 150 °C		

Notes:

1/ These ratings represent the maximum operable values for the device.
2/ Assure Vd - Vctrl $\leq$ 8 V. Compute Vd as follows, Vd = V^+ - Id*40
3/ Combinations of supply voltage, supply current, input power, and output power shall not exceed P_D.
4/ When operated at this power dissipation with a base plate temperature of 70 °C, the median life is 3.8E5 hours.
5/ Assure Vctrl never exceeds Vd during bias up and down sequences. Also, assure Vctrl never exceeds 5V during normal operation.
6/ Junction operating temperature will directly affect the device median time to failure (Tm). For maximum life, it is recommended that junction temperatures be maintained at the lowest possible levels.

TABLE II
RF SPECIFICATIONS
(T_A = 25°C Nominal)

NOTE	TEST	MEASUREMENT CONDITIONS	VALUE			UNITS
			MIN	TYP	MAX	
	SMALL SIGNAL BW			35		GHz
1/, 2/	SMALL-SIGNAL GAIN MAGNITUDE	100KHz thru 30GHz		12		dB
1/, 2/	GAIN FLATNESS	100KHz thru 30GHz		+/-1		dB
3/,4/	SMALL SIGNAL AGC RANGE	100KHz thru 30GHz		3		dB
1/, 2/	INPUT RETURN LOSS MAGNITUDE	100KHz thru 30GHz		10		dB
1/, 2/	OUTPUT RETURN LOSS MAGNITUDE	100KHz thru 30GHz		10		dB
	OUTPUT POWER AT P1dB	100KHz thru 30GHz		18		dBm
3/, 4/	AMPLITUDE	40Gb/s NRZ		4		Vpp

Notes:

1/ Verified at die level on-wafer probe (future requirement, data is not currently available).
2/ Small Signal S-Parameter RF Probe Bias: V+ = 5 V, Vctrl=float, adjust Vg to achieve Id=100mA
3/ Verified by design, MMIC assembled onto evaluation platform detailed on page 8.
4/ Vin=1V, V+=8V, VCTRL=Float, and VG adjusted for ID=100mA.

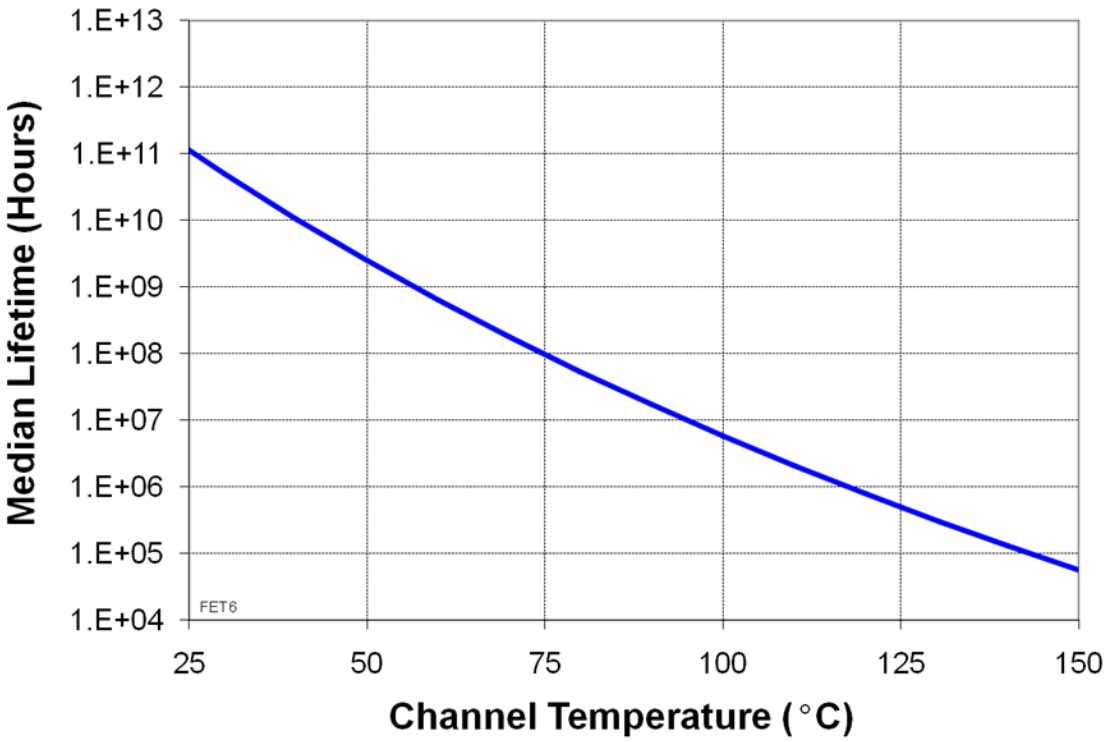
TABLE III
THERMAL INFORMATION

PARAMETER	TEST CONDITIONS	T_{CH} (°C)	θ_{JC} (°C/W)	T_m (HRS)
θ_{JC} Thermal Resistance (channel to backside of carrier)	Vds = 2.5 V* I_D = 135 mA Pdiss = 0.34 W	92	64	1.5 E+7

* Vds = 2.5V across common gate or common source FET in cascode pair.

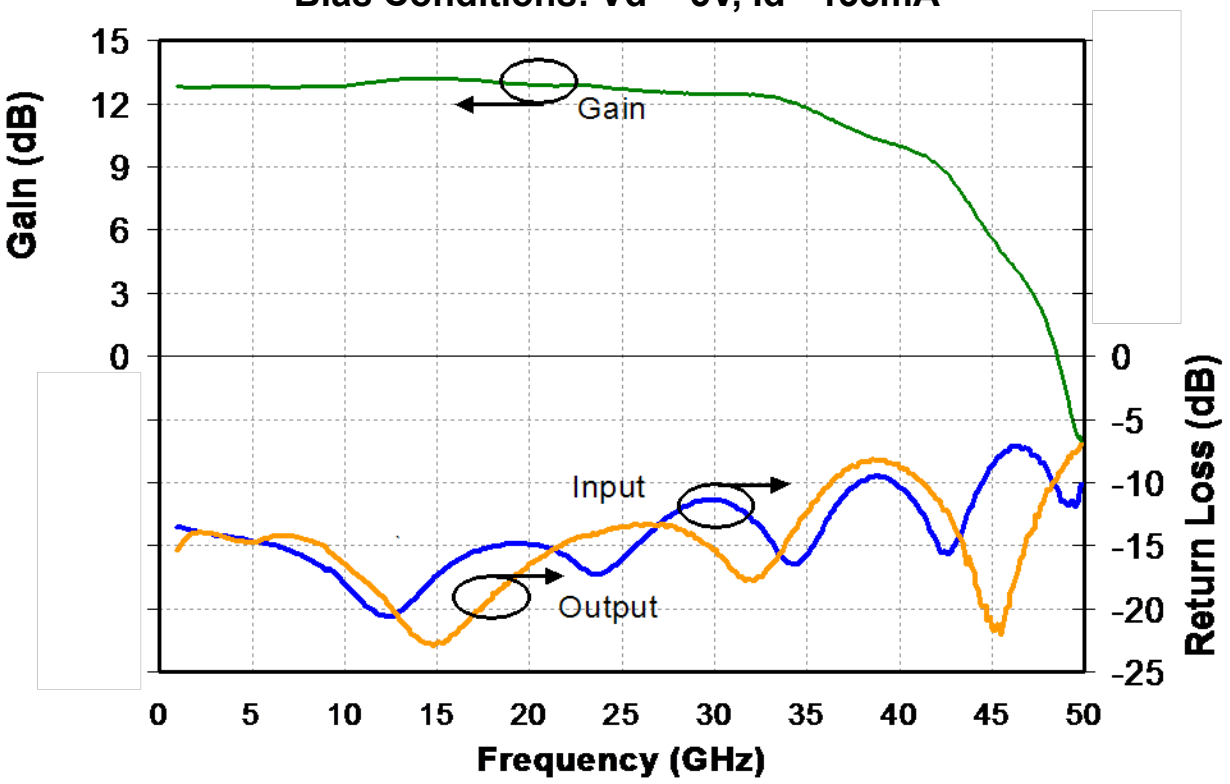
Note: Assumes eutectic attach using 1.5 mil 80/20 AuSn mounted to a 20 mil CuMo Carrier at 70°C baseplate temperature. Worst case condition with no RF applied, 100% of DC power is dissipated. Thermal transfer is conducted thru the bottom of the TGA4832 into the mounting carrier. Design the mounting interface to assure adequate thermal transfer to the base plate.

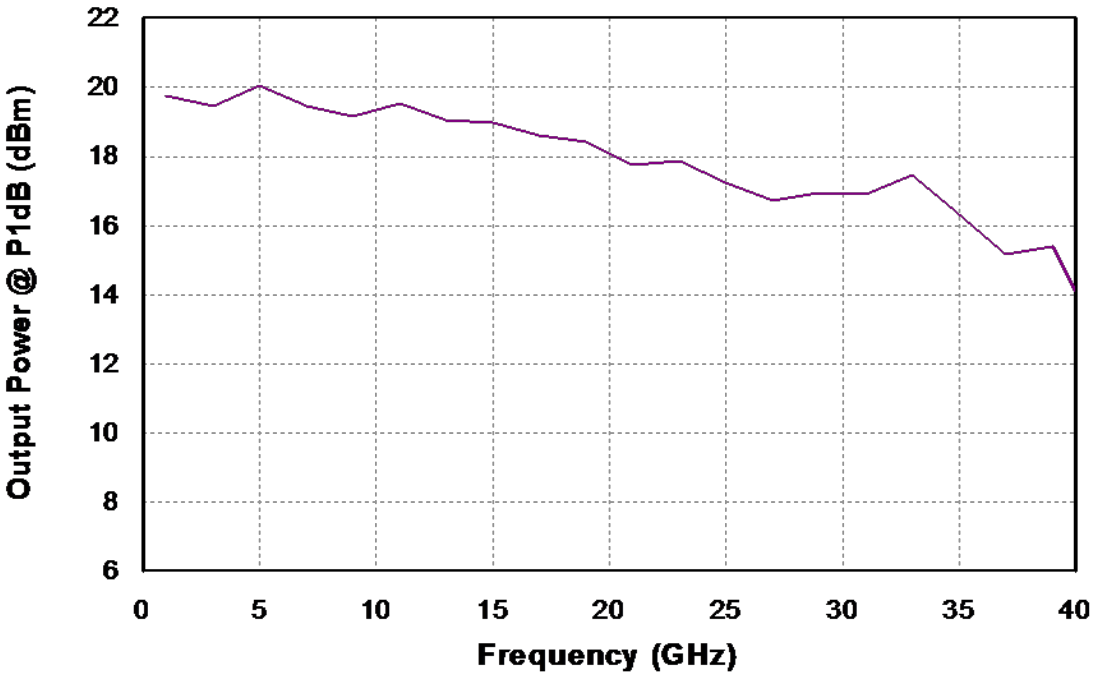
Median Lifetime (Tm) vs. Channel Temperature



Measured Fixtured Data

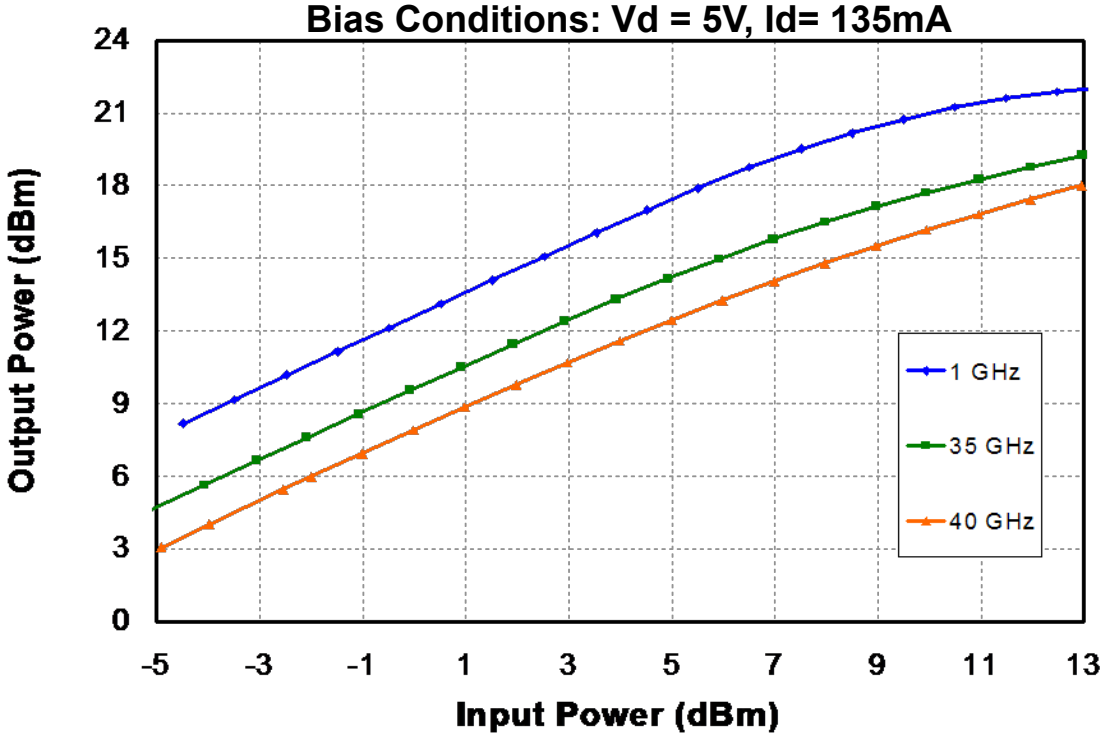
Bias Conditions: Vd = 5V, Id= 135mA



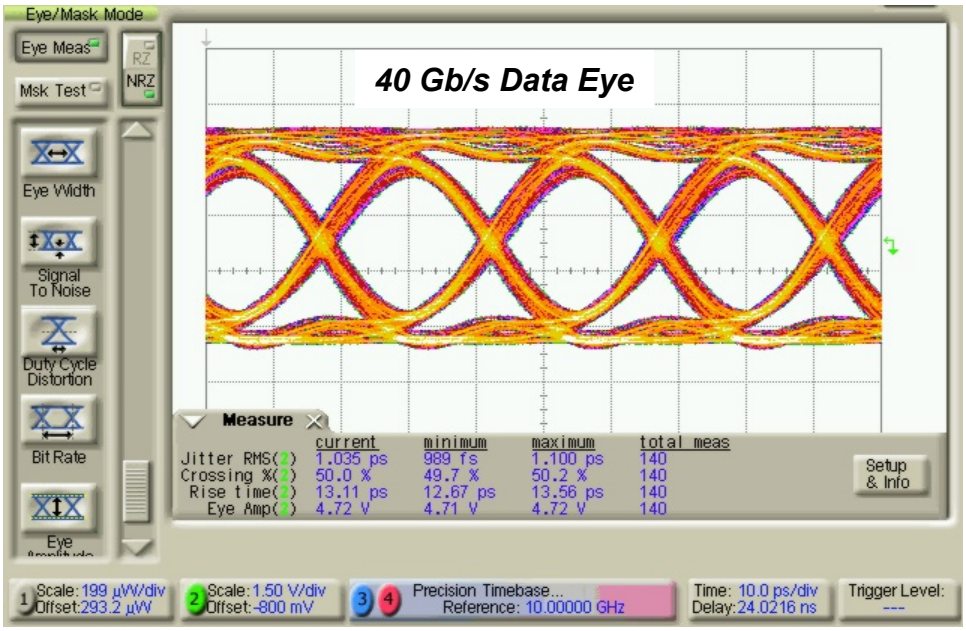


Measured Fixtured Data

Bias Conditions: Vd = 5V, Id= 135mA



40Gb/s NRZ 2^31-1 PRBS Vin=1.8Vpp.



Bias Procedure for V+ = 10.4 V Operation
Fiber Optic Applications

Bias ON

1. Disable the PPG
2. Set Vg=-1V
3. Set Vctrl = 2.2V (if appliable)
4. Increase V+ to 7V observing Id.
   - Assure Id increased to between 10 and 100mA
5. Raise V+ to 10.4V
   - Id should still be between 10 and 100mA
6. Make Vg more positive until **Id=135mA**.
   - Typical value for **Vg is -0.3V**
7. Enable the PPG

Bias OFF

1. Disable the output of the PPG
2. Set Vctrl = 0V (if appliable)
3. Set V+=0V
4. Set Vg=0V

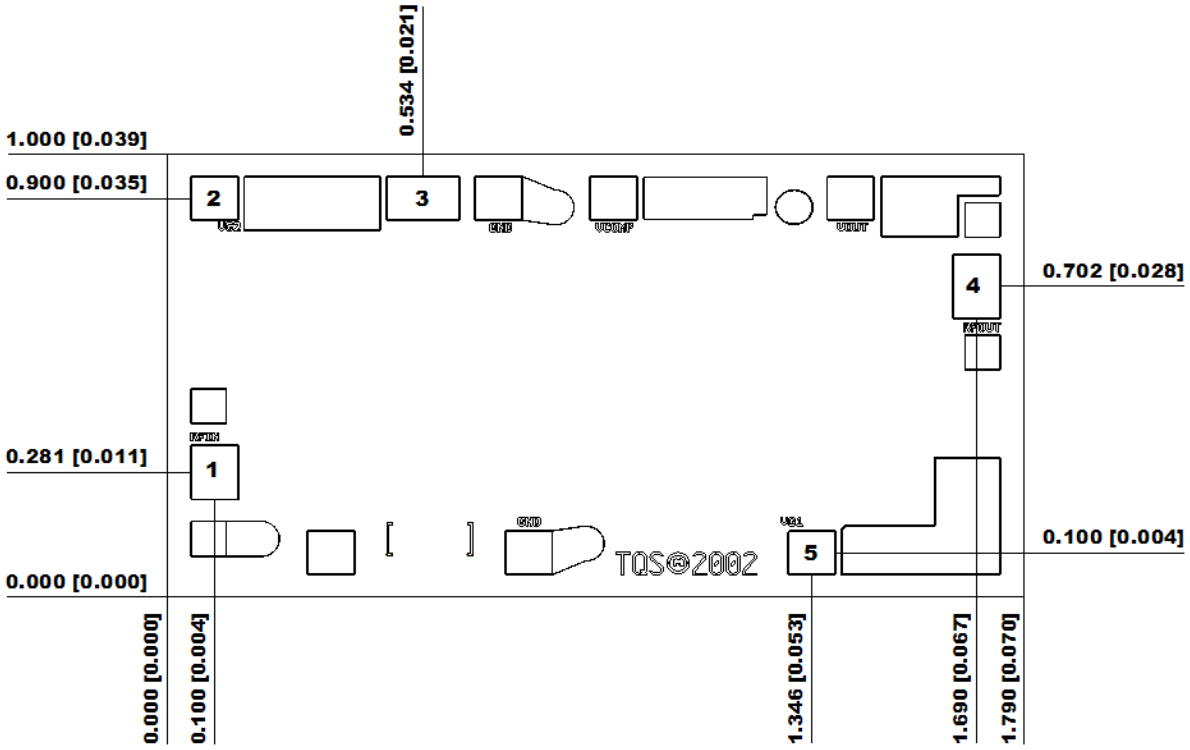
Note: Assure Vctrl never exceeds Vd during Bias ON and Bias OFF sequences and during normal operation.

Bias Procedure @ Vd = 5V Operation

1. Bias Conditions: Vd = 5.0 V, Id = 135 mA
2. Adjust Vg for Id = 135 mA
3. Adjust Vctrl for Gain and Eye crossing control. Vctrl bias is optional
4. Positive or negative gate bias may be required to achieve recommended operating point:- 0.5 V < Vg < + 0.5 V

   Note: +5V Bias operation requires a bias tee

Mechanical Drawing

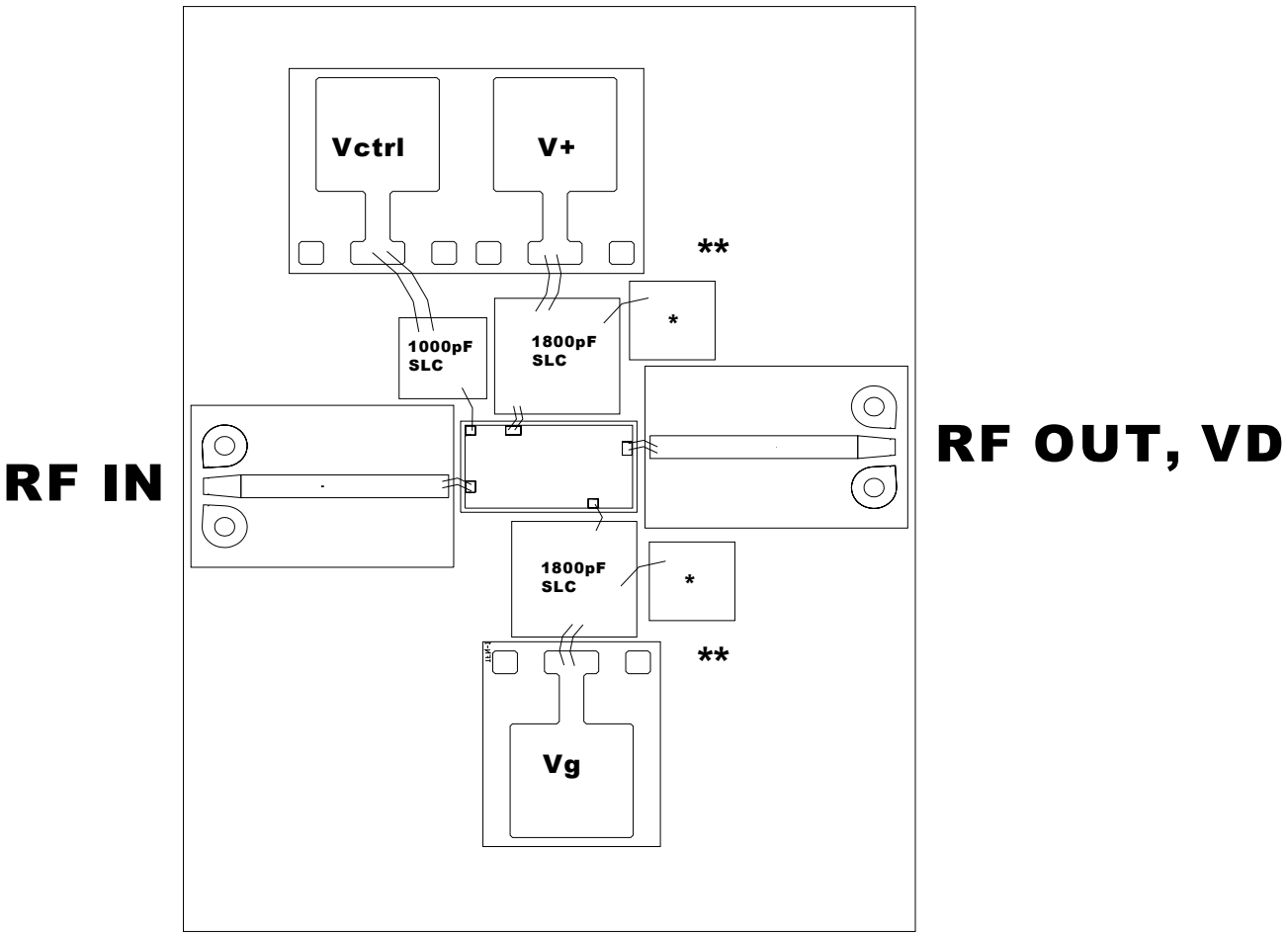


Units: millimeters (inches)
Thickness: 0.100 (0.004) (reference only)
Chip edge to bond pad dimensions are shown to center of pad
Chip size tolerance: +/- 0.051 (0.002)

GND IS BACKSIDE OF MMIC

Bond Pad #1:	**RF In**	**0.100 x 0.125 [0.0039 x 0.0049]**
Bond Pad #2:	**Vctrl**	**0.100 x 0.100 [0.0039 x 0.0039]**
Bond Pad #3:	**V+**	**0.100 x 0.156 [0.0039 x 0.0061]**
Bond Pad #4:	**RF Out/Vd (RF Out)**	**0.100 x 0.145 [0.0039 x 0.0057]**
Bond Pad #5:	**Vg**	**0.100 x 0.100 [0.0039 x 0.0039]**

Recommended Assembly Diagram



Note: Input and Output ports are DC coupled.

Recommended Components:

* CAPACITOR VALUE	BYPASSING EFFECTIVE TO:
None	20 MHz
0.01 uF	4 MHz
0.1 uF	250 KHz

** 1800pF & 0.1uF capacitors can be substituted with the following integrated capacitors:

Part Number	Manufacturer
GZ0SYC104KJ8182MAW	AVX
VB4080X7R105Z16VHX182	Presidio

Evaluation Platform Assembly Notes

Assembly Notes:

Reflow Attachment:

- Use AuSn (80/20) solder with limited exposure to temperatures at or above 300□C
- Use alloy station or conveyor furnace with reducing atmosphere
- No fluxes should be utilized
- Coefficient of thermal expansion matching is critical for long-term reliability
- Storage in dry nitrogen atmosphere

Adhesive Attachment:

- Organic attachment can be used in low-power applications
- Curing should be done in a convection oven; proper exhaust is a safety concern
- Microwave or radiant curing should not be used because of differential heating
- Coefficient of thermal expansion matching is critical

Component Pickup and Placement:

- Vacuum pencil and/or vacuum collet preferred method of pick up
- Avoidance of air bridges during placement
- Force impact critical during auto placement

Interconnect:

- Thermosonic ball bonding is the preferred interconnect technique
- Force, time, and ultrasonics are critical parameters
- Aluminum wire should not be used
- Discrete FET devices with small pad sizes should be bonded with 0.0007-inch wire
- Maximum stage temperature: 200□C