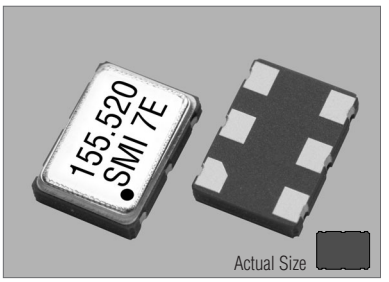
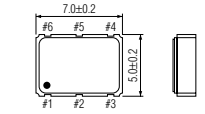
Low Voltage Positive Emitter Coupled Logic Oscillators

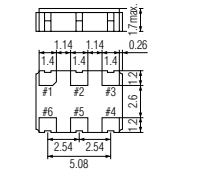
57SMO (+2.5V or +3.3V FIXED LVPECL MODELS) — STANDARD SMD CLOCK OSCILLATORS

57SMO



57SMO



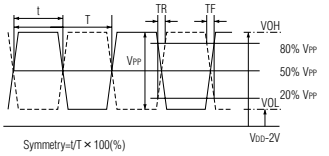


PIN	CONNECTION	
1	"L"	OPEN or "H"
2	N.C.	
3	GND	
4	Z	OUTPUT
5	Z	C-OUTPUT
6	V_{DD}	

Z : high impedance

OUTPUT WAVEFORM(1)

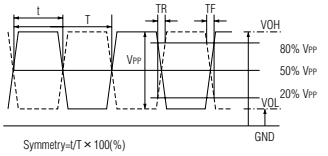
Termination : 50Ω impedance matching



Symmetry=t/T × 100(%)

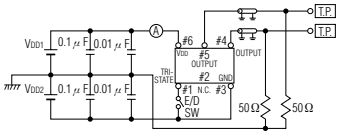
OUTPUT WAVEFORM(2)

Termination : high impedance probes



Symmetry=t/T × 100(%)

TEST CIRCUIT(1)



Termination : 50Ω impedance matching

V_{DD}	V_{DD1}	V_{DD2}
+3.3V	+2.0V	-1.3V
+2.5V	+2.0V	-0.5V

STANDARD SPECIFICATIONS

LVPECL

Item	Specifications	
Generic part number	57SMO※1	
Frequency range	40.000 MHz to 300.000 MHz	
Frequency stability (0°C to +70°C) over all conditions	57SMO(A) : ±100 ppm 57SMO(B) : ±50 ppm 57SMO(C) : ±30 ppm 57SMO(D) : ±25 ppm	
Operating Conditions		
Operating temperature	0°C to +70°C(Standard) −40°C to +85°C (W)	
Input voltage (V_{DD})	+2.5V DC ±5%	+3.3V DC ±5%
Stand-by control voltage (Pin#1)	V_{IH} : 70%V_{DD} min. V_{IL} : 30%V_{DD} max.※2	
Absolute Max. Ratings		
Supply voltage	−0.5V to +5.0V DC	
Storage temperature	−50°C to +125°C	
Input current (Pin #1 = Open or V_{IH})	90 mA max.	
Stand−by current※2 (Pin #1 = V_{IL})	30 μA max.	
Output (0°C to +70°C)		
Symmetry (at crossing point)	40% to 60%	45% to 55%
Rise and fall times	1 ns max. (20% to 80% of amplitude)	
"0" level	V_{OL} : +1.195V max.	V_{OL} : +1.745V max.
"1" level	V_{OH} : +1.415V min.	V_{OH} : +2.215V min.
Load	50Ω into V_{DD} −2V	
Disable delay time	200 ns max.	
Enable delay time	10 ms max.	
Startup time	10 ms max.	
RMS jitter (12 kHz to 20 MHz band)	1 ps max.	
Aging	±5 ppm max. at +25°C ±3°C for first year	
Reflow condition	+250°C ±10°C for 10 seconds +170°C ±10°C for 1 to 2 minutes (preheating)	

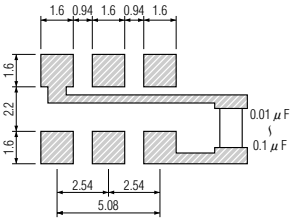
(※1) Final exact part number to be determined with frequency, frequency stability, operating temperature and input voltage.
e.g. 57SMO(3.3VB)W 155.520 MHz.

(※2) Internal crystal oscillation to be halted (Pin #1=V_{IL}).

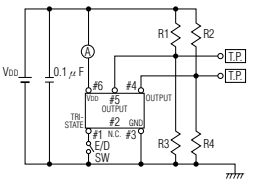
PACKAGE DATA

Item \ Package	57SMO
Lid	Metal
Base	Ceramic
Sealing	Seam
Terminal	Tungsten (metalized)
Terminal plating	Gold / Nickel (surface) / (under)
RoHS	Compliant (Pb-free)

SOLDERING PATTERN



TEST CIRCUIT(2)

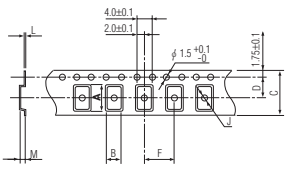


Termination : high impedance probes

V_{DD}	R_1	R_2	R_3	R_4
+3.3V	130Ω	130Ω	82Ω	82Ω
+2.5V	270Ω	270Ω	62Ω	62Ω

Note : R_3 & R_4 to change for the use of low impedance probes

TAPE SPECIFICATIONS



A	B	C	D	F	J	L	M	Reel Dia.	Qty/Reel
7.5	5.5	16.0	7.5	8.0	2.0	0.3	2.2	245	1000pcs