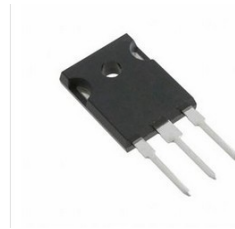# IRFP054N

KERSEMI ELECTRONIC CO.,LTD.
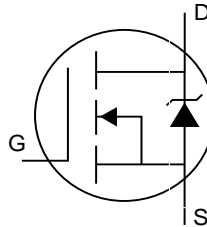
- Advanced Process Technology
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated

TO-247AC

Description

The TO-247 package is preferred for commercial-industrial applications where higher power levels preclude the use of TO-220 devices. The TO-247 is similar but superior to the earlier TO-218 package because of its isolated mounting hole.

$V_{DSS} = 55V$

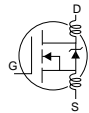$R_{DS(on)} = 0.012\Omega$

$I_D = 81A⑥$

Absolute Maximum Ratings

	Parameter	Max.	Units
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	81⑥	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	57	
I_{DM}	Pulsed Drain Current ①⑤	290	
P_D @T_C = 25°C	Power Dissipation	170	W
	Linear Derating Factor	1.1	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
E_{AS}	Single Pulse Avalanche Energy②⑤	360	mJ
I_{AR}	Avalanche Current①	43	A
E_{AR}	Repetitive Avalanche Energy①	17	mJ
dv/dt	Peak Diode Recovery dv/dt ③⑤	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	
T_{STG}	Storage Temperature Range		°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 srew	10 lbf•in (1.1N•m)	

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	——	0.90	
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	0.24	——	°C/W
$R_{\theta JA}$	Junction-to-Ambient	——	40	

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	55	——	——	V	V_{GS} = 0V, I_D = 250µA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.06	——	V/°C	Reference to 25°C, I_D = 1mA⑤
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	——	0.012	Ω	V_{GS} = 10V, I_D = 43A ④
$V_{GS(th)}$	Gate Threshold Voltage	2.0	——	4.0	V	V_{DS} = V_{GS}, I_D = 250µA
g_{fs}	Forward Transconductance	30	——	——	S	V_{DS} = 25V, I_D = 43A⑤
I_{DSS}	Drain-to-Source Leakage Current	——	——	25	µA	V_{DS} = 55V, V_{GS} = 0V
		——	——	250		V_{DS} = 44V, V_{GS} = 0V, T_J = 150°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	100	nA	V_{GS} = 20V
	Gate-to-Source Reverse Leakage	——	——	-100		V_{GS} = -20V
Q_g	Total Gate Charge	——	——	130	nC	I_D = 43A
Q_{gs}	Gate-to-Source Charge	——	——	23		V_{DS} = 44V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	——	53		V_{GS} = 10V, See Fig. 6 and 13 ④⑤
$t_{d(on)}$	Turn-On Delay Time	——	11	——	ns	V_{DD} = 28V
t_r	Rise Time	——	66	——		I_D = 43A
$t_{d(off)}$	Turn-Off Delay Time	——	40	——		R_G = 3.6Ω
t_f	Fall Time	——	46	——		R_D = 0.62Ω, See Fig. 10④⑤
L_D	Internal Drain Inductance	——	5.0	——	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L_S	Internal Source Inductance	——	13	——		
C_{iss}	Input Capacitance	——	2900	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	880	——		V_{DS} = 25V
C_{rss}	Reverse Transfer Capacitance	——	330	——		f = 1.0MHz, See Fig. 5⑤

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	81⑥	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	290		
V_{SD}	Diode Forward Voltage	——	——	1.3	V	T_J = 25°C, I_S = 43A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	——	81	120	ns	T_J = 25°C, I_F = 43A
Q_{rr}	Reverse Recovery Charge	——	240	370	nC	di/dt = 100A/µs ④⑤

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② V_{DD} = 25V, starting T_J = 25°C, L = 390µH R_G = 25Ω, I_{AS} = 43A. (See Figure 12)

③ I_{SD} ≤ 43A, di/dt ≤ 260A/µs, V_{DD} ≤ $V_{(BR)DSS}$, T_J ≤ 175°C

④ Pulse width ≤ 300µs; duty cycle ≤ 2%.

⑤ Uses IRF1010N data and test conditions

⑥ Caculated continuous current based on maximum allowable junction temperature;for recommended current-handling of the package refer to Design Tip # 93-4
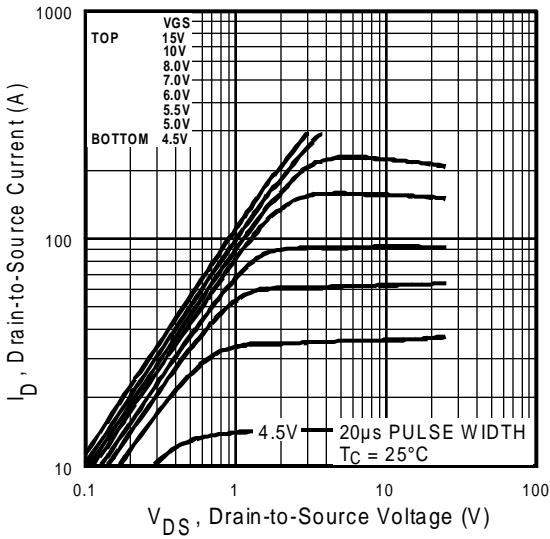
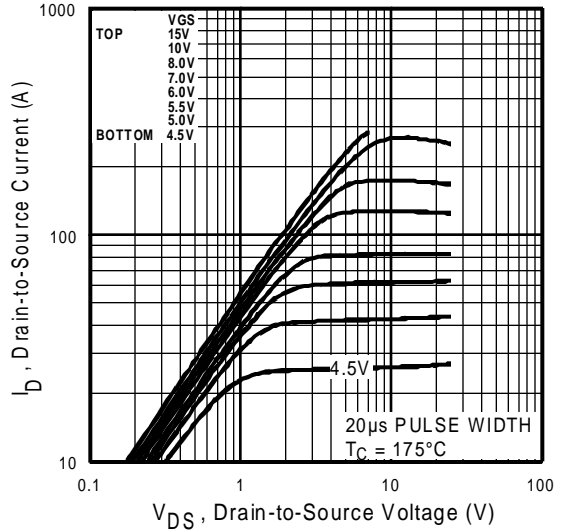**Fig 1.** Typical Output Characteristics
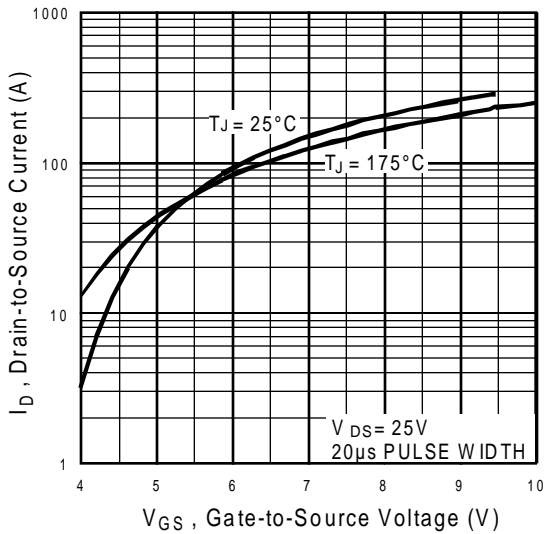

Fig 2. Typical Output Characteristics

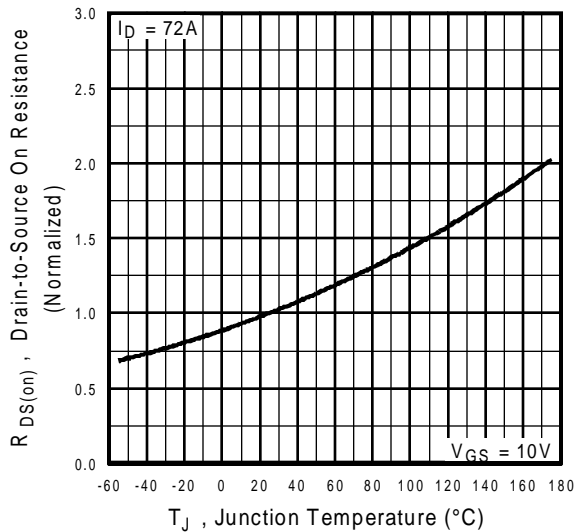**Fig 3.** Typical Transfer Characteristics

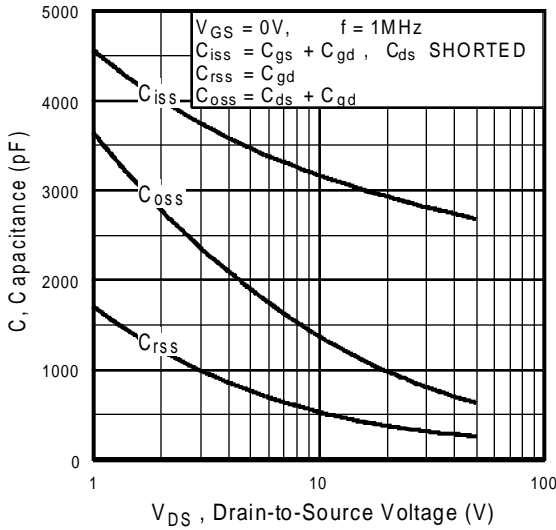**Fig 4.** Normalized On-Resistance Vs. Temperature

Fig 5. Typical Capacitance Vs.
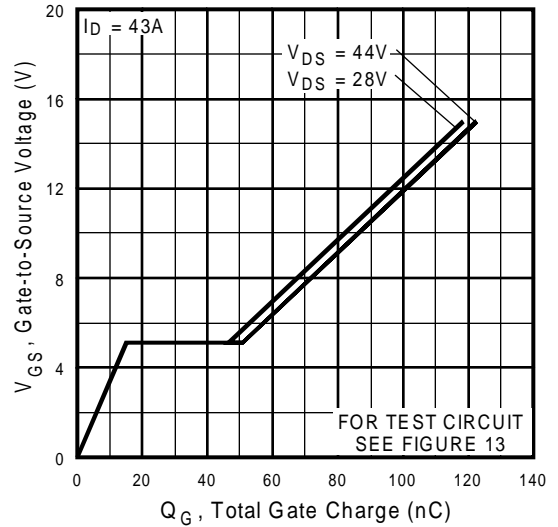Drain-to-Source Voltage
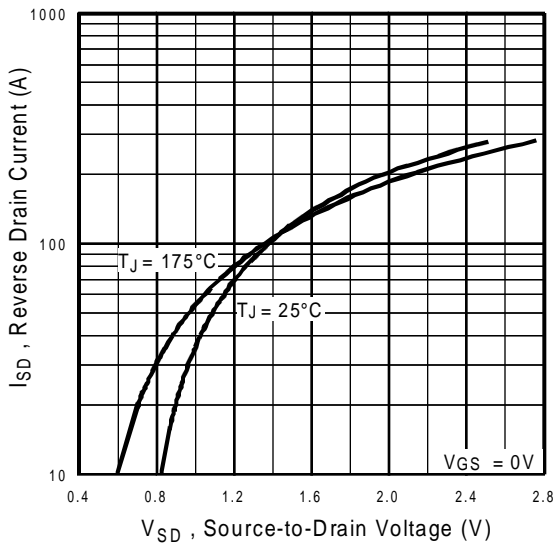
Fig 6. Typical Gate Charge Vs.
Gate-to-Source Voltage

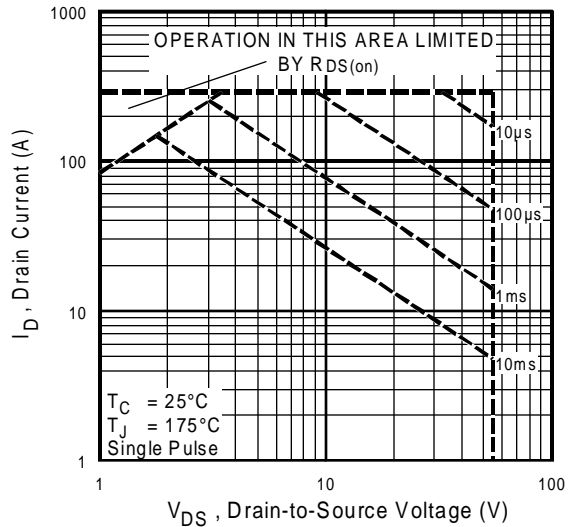**Fig 7.** Typical Source-Drain Diode
Forward Voltage
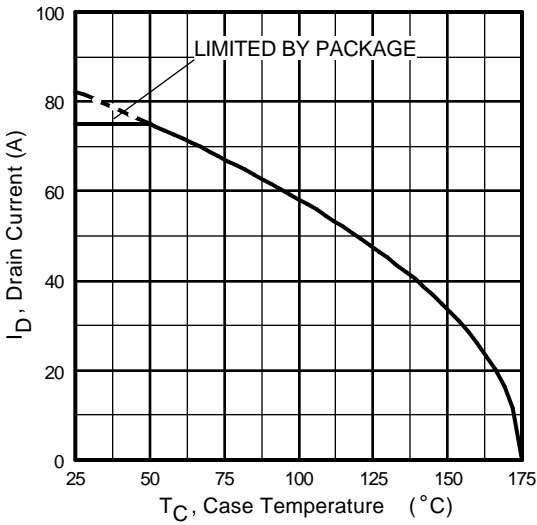
Fig 8. Maximum Safe Operating Area

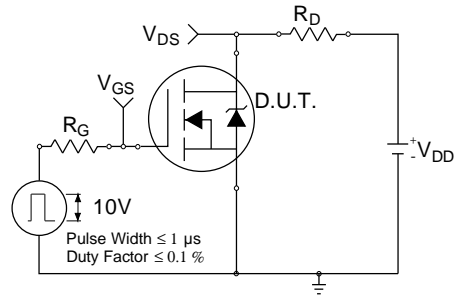**Fig 9.** Maximum Drain Current Vs.
Case Temperature

Fig 10a. Switching Time Test Circuit
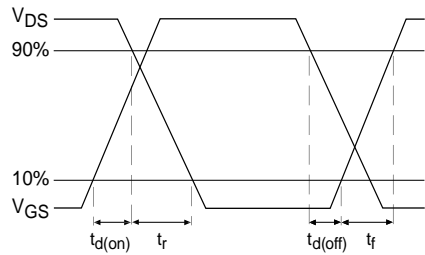

Fig 10b. Switching Time Waveforms
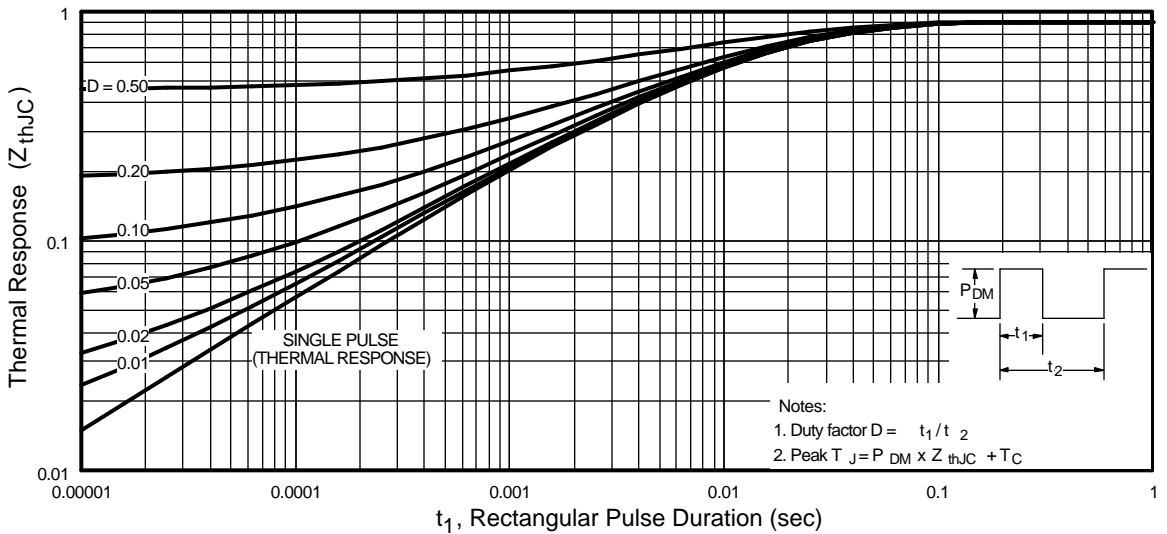

Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case
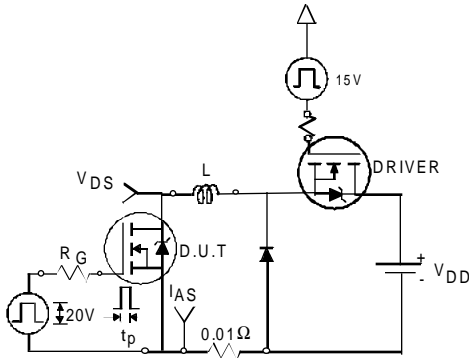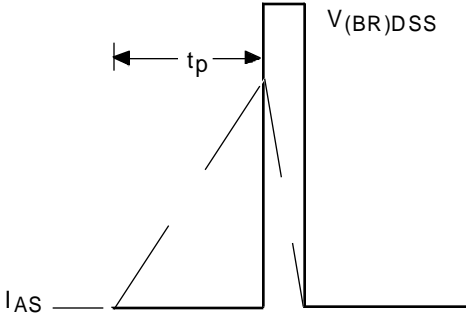
Fig 12a. Unclamped Inductive Test Circuit

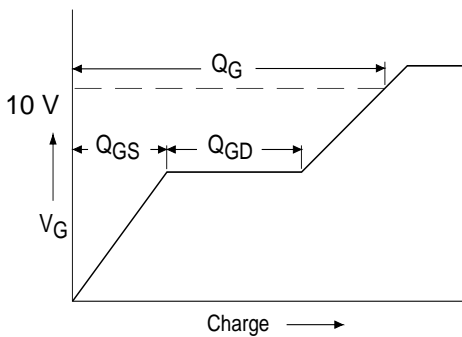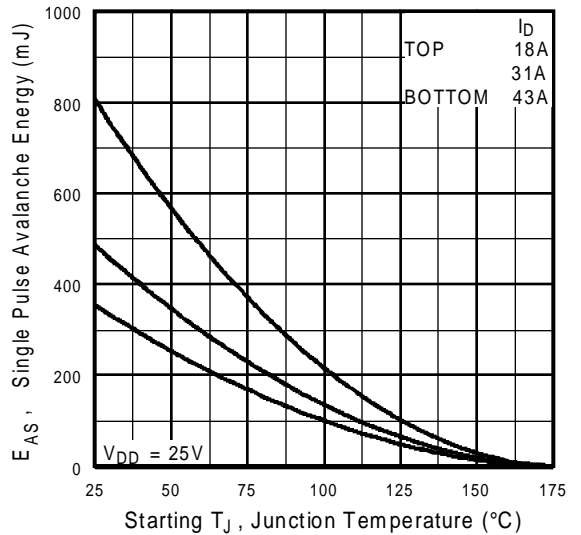

Fig 12b. Unclamped Inductive Waveforms

Fig 12c. Maximum Avalanche Energy Vs. Drain Current

Fig 13a. Basic Gate Charge Waveform

Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit

D.U.T

Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance
  Current Transformer

③

②

④

①

R_G

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

V_{DD}

① Driver Gate Drive

P.W.

Period

$D = \dfrac{P.W.}{Period}$

$V_{GS}=10V$ *

② D.U.T. I_{SD} Waveform

Reverse
Recovery
Current

Body Diode Forward
Current

di/dt

③ D.U.T. V_{DS} Waveform

Diode Recovery
dv/dt

V_{DD}

Re-Applied
Voltage

Body Diode Forward Drop

④ Inductor Curent

Ripple ≤ 5%

I_{SD}

* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFETS

Package Outline

TO-247AC Outline

Dimensions are shown in millimeters (inches)

NOTES:

1 DIMENSIONING & TOLERANCING
PER ANSI Y14.5M, 1982.
2 CONTROLLING DIMENSION : INCH.
3 CONFORMS TO JEDEC OUTLINE
TO-247-AC.

LEAD ASSIGNMENTS

1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

Part Marking Information

TO-247AC

EXAMPLE : THIS IS AN IRFPE30
WITH ASSEMBLY
LOT CODE 3A1Q

INTERNATIONAL
RECTIFIER
LOGO

IRFPE30

3A1Q 9302

PART NUMBER

ASSEMBLY
LOT CODE

DATE CODE
(YYWW)
YY = YEAR
WW WEEK