TO-252   TO-251

Features

- 9.3A, 80V, $R_{DS(on)} = 0.21\Omega$ @$V_{GS} = 10$ V
- Low gate charge (typical 5.9 nC)
- Low Crss (typical 13 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability

General Description

These N-Channel enhancement mode power field effect transistors are produced using Kersemi proprietary, planar stripe, DMOS technology.

This advanced technology is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand a high energy pulse in the avalanche and commutation modes. These devices are well suited for low voltage applications such as automotive, high efficiency switching for DC/DC converters, and DC motor control.
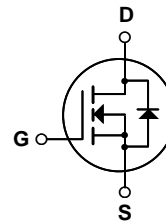
Absolute Maximum Ratings $T_C = 25°C$ unless otherwise noted

Symbol	Parameter		KSMD9N08 / KSMU9N08	Units
V_{DSS}	Drain-Source Voltage		80	V
I_D	Drain Current - Continuous ($T_C = 25°C$)		7.4	A
	- Continuous ($T_C = 100°C$)		4.68	A
I_{DM}	Drain Current - Pulsed	(Note 1)	29.6	A
V_{GSS}	Gate-Source Voltage		± 25	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	55	mJ
I_{AR}	Avalanche Current	(Note 1)	7.4	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	2.5	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	6.5	V/ns
P_D	Power Dissipation ($T_A = 25°C$) *		2.5	W
	Power Dissipation ($T_C = 25°C$)		25	W
	- Derate above 25°C		0.2	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	5.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

c

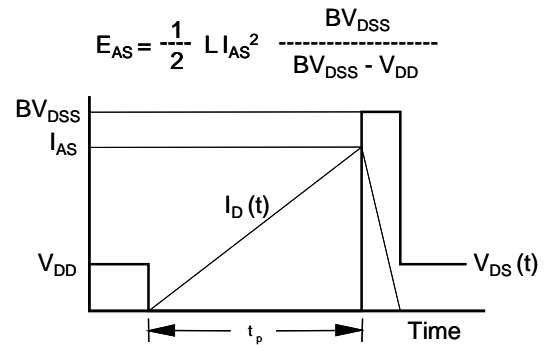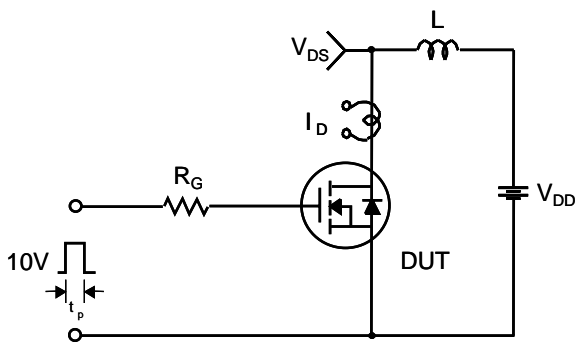| Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0$ V, $I_D = 250$ µA	80	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	$I_D = 250$ µA, Referenced to 25°C	--	0.08	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80$ V, $V_{GS} = 0$ V	--	--	1	µA
		$V_{DS} = 64$ V, $T_C = 125$°C	--	--	10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 25$ V, $V_{DS} = 0$ V	--	--	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -25$ V, $V_{DS} = 0$ V	--	--	-100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}$, $I_D = 250$ µA	2.0	--	4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10$ V, $I_D = 3.7$ A	--	0.16	0.21	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 30$ V, $I_D = 3.7$ A (Note 4)	--	3.5	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	$V_{DS} = 25$ V, $V_{GS} = 0$ V, f = 1.0 MHz	--	190	250	pF
C_{oss}	Output Capacitance		--	70	90	pF
C_{rss}	Reverse Transfer Capacitance		--	13	17	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40$ V, $I_D = 9.3$ A, $R_G = 25$ Ω	--	2.8	15pp	ns
t_r	Turn-On Rise Time		--	28	65	ns
$t_{d(off)}$	Turn-Off Delay Time		--	9	28	ns
t_f	Turn-Off Fall Time	(Note 4, 5)	--	17	45	ns
Q_g	Total Gate Charge	$V_{DS} = 64$ V, $I_D = 9.3$ A, $V_{GS} = 10$ V	--	5.9	7.7	nC
Q_{gs}	Gate-Source Charge		--	1.5	--	nC
Q_{gd}	Gate-Drain Charge	(Note 4, 5)	--	2.6	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	7.4	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	29.6	A
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0$ V, $I_S = 7.4$ A	--	--	1.5	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0$ V, $I_S = 9.3$ A,	--	50	--	ns
Q_{rr}	Reverse Recovery Charge	dI_F / dt = 100 A/µs (Note 4)	--	70	--	nC

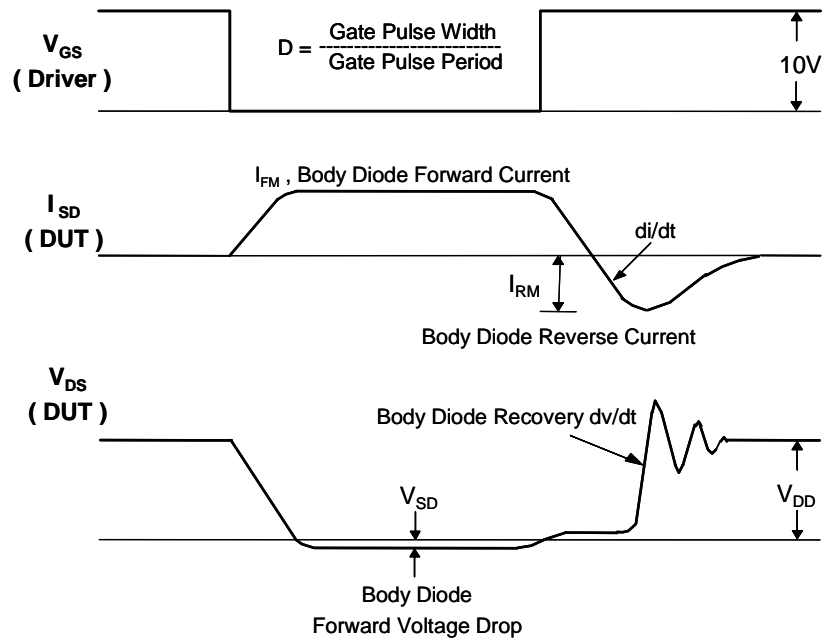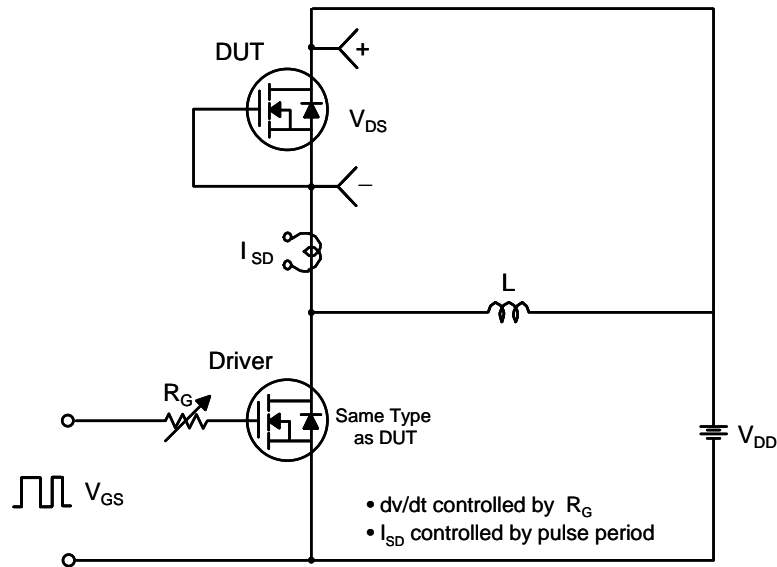**Notes:**
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 1.38mH, $I_{AS} = 7.4$A, $V_{DD} = 25$V, $R_G = 25$ Ω, Starting $T_J = 25$°C
3. $I_{SD} \leq 9.3$A, di/dt ≤ 300A/µs, $V_{DD} \leq BV_{DSS}$, Starting $T_J = 25$°C
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics
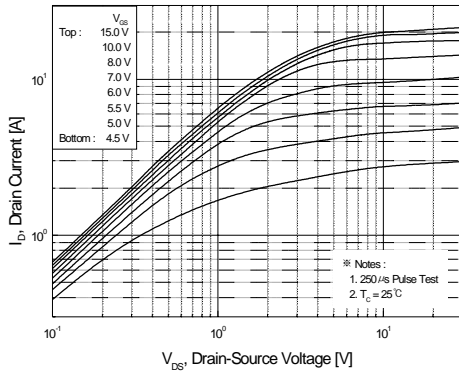
Figure 1. On-Region Characteristics
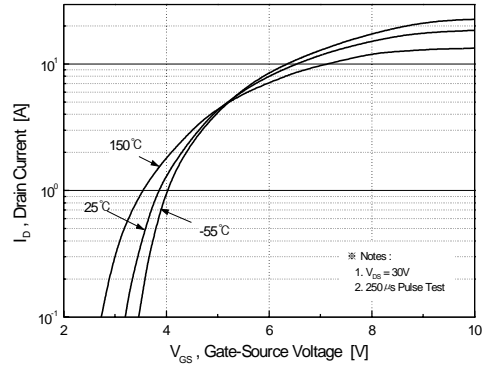
Figure 2. Transfer Characteristics
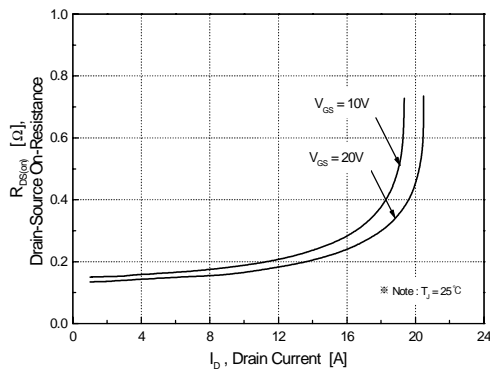
Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage
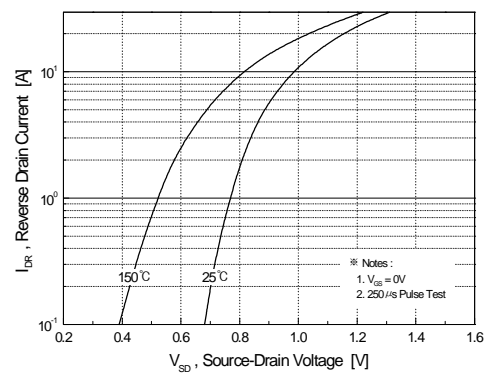
Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature
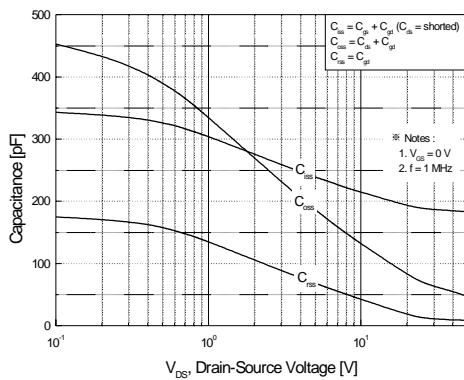
Figure 5. Capacitance Characteristics
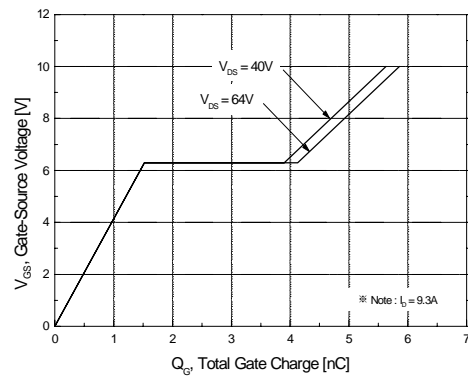
Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)
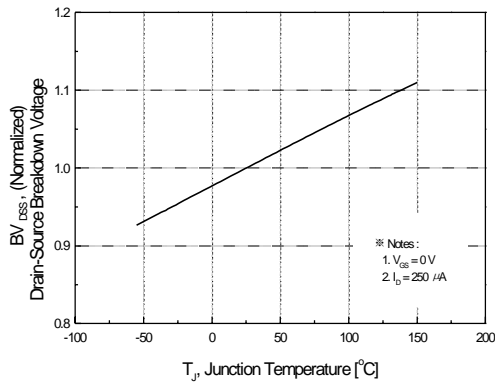
Figure 7. Breakdown Voltage Variation vs. Temperature
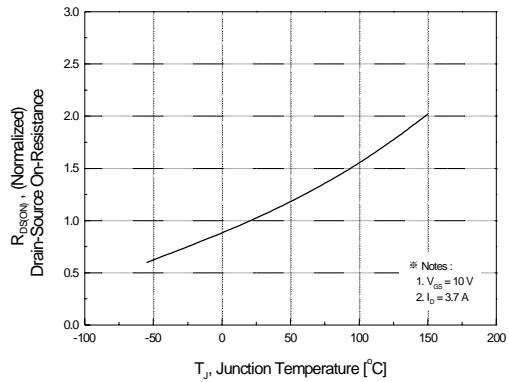
Figure 8. On-Resistance Variation vs. Temperature
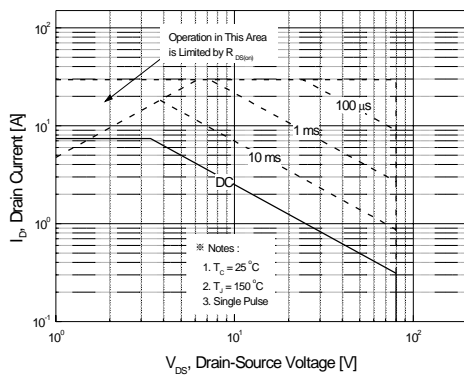
Figure 9. Maximum Safe Operating Area
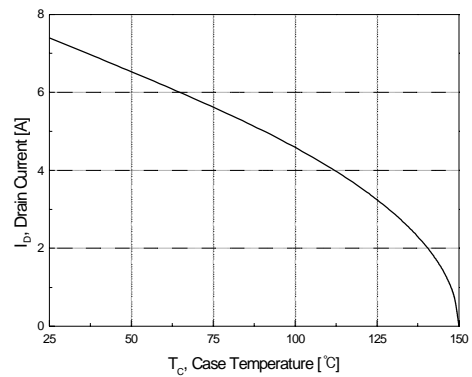
Figure 10. Maximum Drain Current vs. Case Temperature
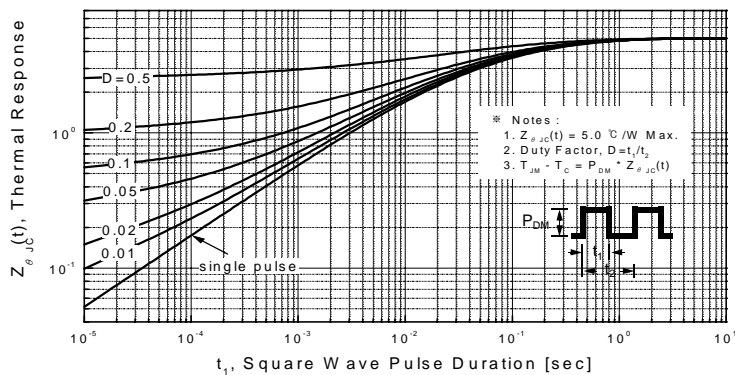
Figure 11. Transient Thermal Response Curve

Gate Charge Test Circuit & Waveform
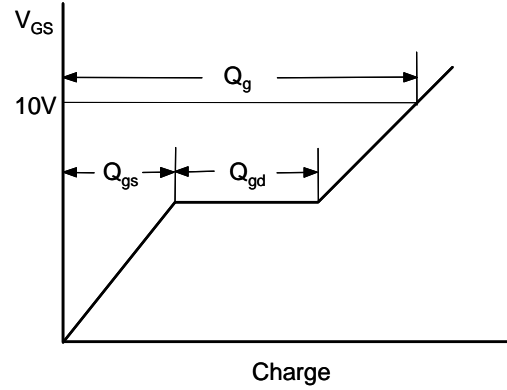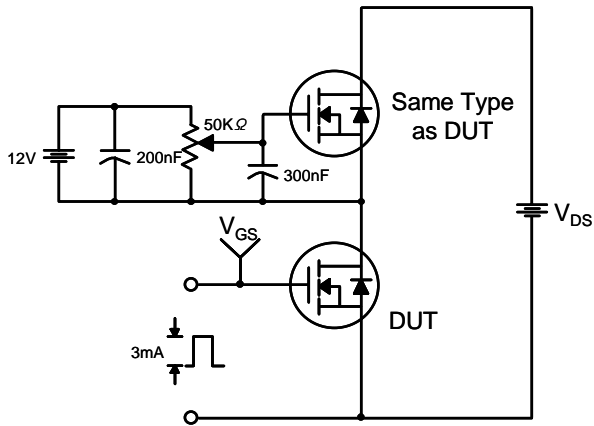
Resistive Switching Test Circuit & Waveforms
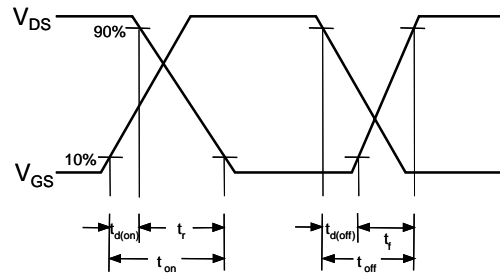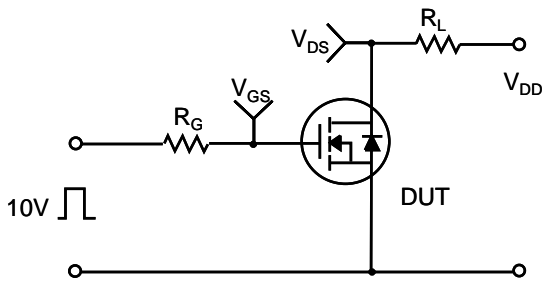
Unclamped Inductive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2 \frac{BV_{DSS}}{BV_{DSS} - V_{DD}}$$

Peak Diode Recovery dv/dt Test Circuit & Waveforms

DUT

V_{DS}

I_{SD}

L

Driver

R_G

Same Type
as DUT

V_{DD}

V_{GS}

• dv/dt controlled by R_G
• I_{SD} controlled by pulse period

V_{GS}
(Driver)

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$

10V

I_{SD}
(DUT)

I_{FM} , Body Diode Forward Current

di/dt

I_{RM}

Body Diode Reverse Current

V_{DS}
(DUT)

Body Diode Recovery dv/dt

V_{SD}

V_{DD}

Body Diode
Forward Voltage Drop

Package Dimensions

DPAK
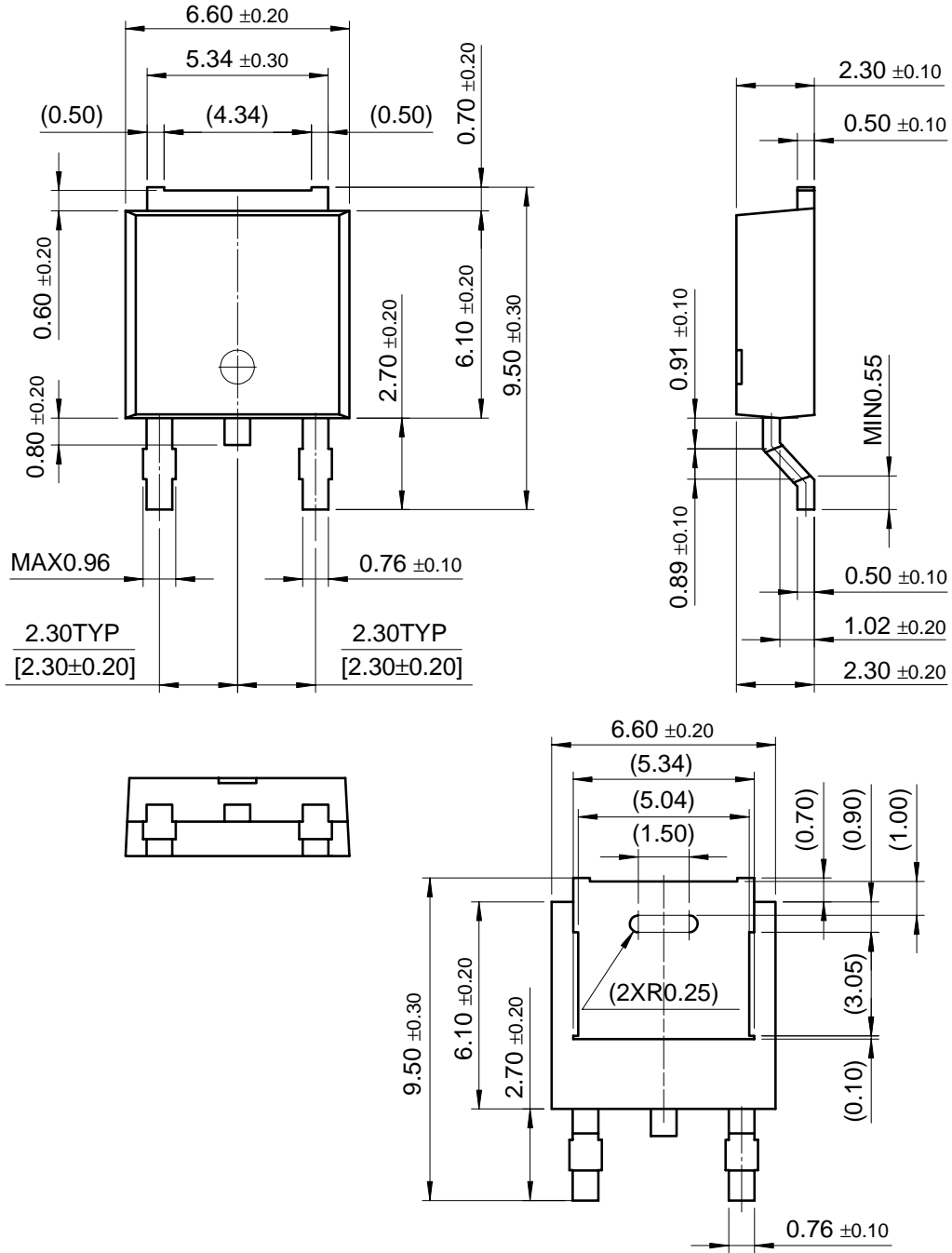
Package Dimensions (Continued)

IPAK