MN158412

Features

- ROM capacity: 4,096 × 8 bits
- RAM capacity:256×4bits+ 1,024×4bits (direct access)(access via port)
- \bullet Machine cycle:2.23 $\mu s (4.5 \text{ to } 5.5 \text{ V})$

17.9 μ s(2.5 to 5.5 V)

●Interrupt:External interrupt

Timer interrupt

Serial interrupt

- Timer/counter: Timer and event count functions provided by 8-bit programmable timer with 7-bit prescaler
- Serial interface: 8-bit synchronous type
- DTMF circuit incorporated: DTMF output, 1 channel
- Clock selector circuit incorporated:

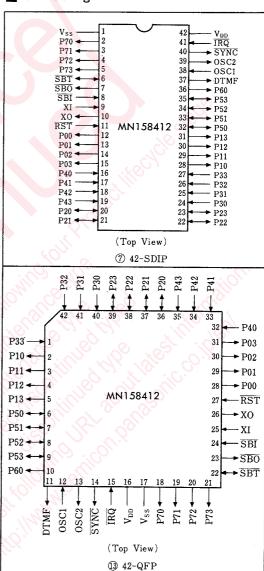
Programmable selection of system clocks enabled. Clock sources are OSC1, OSC2 or XI, XO.

- Backup mode: STOP/HALT mode
- Operating voltage range: 2.5 to 5.5 V

for general purpose I/O	8	• I/O Pins:
for general purpose input	8	
for general purpose output	8	
for high-voltage N-channel	5	
open drain output		
for serial data input	1	
for serial data output	1	
for serial clock I/O	1	
for DTMF output	1	

- Process: Silicon gate CMOS
- Package: 42-SDIP/QFP
- Piggyback: EP158412

■ Pin Configuration



■ Pin Functions

Pin No.		C 1 1	D. M	I/O	Description
42-SDIP	42-QFP	Symbol	Pin Name	1/0	Description
42 1	16 17	$V_{ exttt{DD}}$ $V_{ exttt{SS}}$	Power supply	I	Connect +2.5-5.5 V to V _{DD} , and 0 V to V _{ss} .
38 39	12 13	OSC1 OSC2	Clock input Clock output	I O	Oscillation terminals to connect ceramic oscillator or crystal oscillator. A feedback resistor is incorporated between OSC/and OSC2.
9 10	25 26	XI XO	Clock input Clock output	I O	Even counter clock, source terminals to connect a crystal oscillator. A feedback resistor is incoroprated between XI and XO. They serve as an operating clock source when XI/XO is specified by clock selection.
11	27	RST	Reset input	I	Reset is applied if the "L" level is inputted over 1 machine cycle. A pull-up resistor can be specified with a mask option.
40	14	SYNC	Sync.signal output	0	An internal timing signal is outputted every machinale cycle.
41	15	ĪRQ	External inter- rupt	I	External interrupt terminal which receives an interrupt at negative edge. A pull-up resistor can be specified with a mask option.
6	22	SBT	Serial interface clock output	I/O	Serial interface send/receive clock I/O terminal. It serves as an output terminal in the internal clock mode, and as an input terminal in the external clock mode. A pull-up resistor can be specified with a mask option.
7	23	SBO	Serial interface data output	0	Serial interface send data output terminal. It outputs 8-bit serial data in the send mode. A pull-up resistor can be specified with a mask option.
8	24	SBI	Serial interface data input	iiige.	Serial interface receive data input terminal. It inputs 8-bit serial data in the receive mode. A pull-up resister can be specified with a mask option.
37	11	DTMF	DTMF signal output ter- minal	8	It outputs a DTMF signal.
20~23 32~35	36~39 6~9	P20~P23 P50~P53	Parallel data I/O	I/O /I /O	4-bit parallel data I/O ports. Input, output or I/O can be selected with a mask option.
24~27 16~19	1 32~35	P30~P33 P40~P43	Parallel data input	IQ	4-bit parallel data input ports. A pull-up resistor can be specified with a mask option.
36 2~5	10 18~21	P60 P70~P73	Parallel data output	0	4-bit parallel data output ports. 12 V N-channel open drain output. High impedance at reset time.
12~15 28~31	28~31 2~5	P00~P03 P10~P13	Parallel data output	0	4-bit parallel data output ports. "H" level at reset time.

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