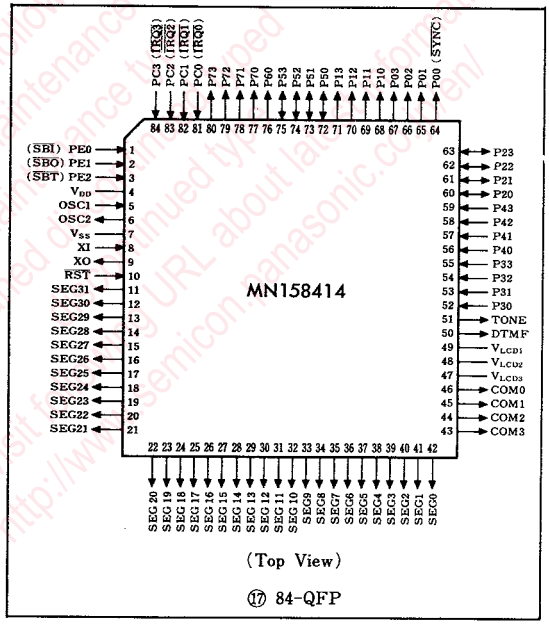
MN158414

■ Features

- ROM capacity: 4,096 × 8 bits
- RAM capacity: 256×4bits +1,024×4bits (direct access)(access via port)
- Machine cycle: 2.0 μs(4.5 to 5.5 V)
  (2.23 μs at 3.58 MHz when DTMF is used)
  8.0 μs(2.5 to 5.5 V)
- Interrupt: External interrupt 4
  Timer interrupt 1
  Serial interrupt 1
  2 Hz-cycle interrupt 1
- Timer/counter: Timer and event counter functions provided by 8-bit programmable timer with 7-bit prescaler
- Serial interface: 8-bit synchronous type
- DTMF circuit incorporated: DTMF output, 1 channel
- TONE circuit incorporated: Programmable setting of frequency enabled
- LCD driver circuit incorporated: 4 commons, 32 segments
- Time base interrupt generator circuit incorporated: 2 Hz cycle
- Clock selector circuit incorporated:
  Programmable selection of system clock sources enabled. Clock sources are OSC1, OSC2 or XI, XO.
- Backup mode: STOP/HALT mode
- Supply voltage: 2.5 V to 5.5 V
- I/O pins:
  - 8 for general purpose I/O
  - 15 for general purpose input
  - 8 for general purpose output
  - 5 for high breakdown voltage N-channel open drain output
  - 1 for serial data input
  - 1 for serial data output
  - 1 for serial clock I/O
  - 4 for LCD drive common output
  - 32 for LCD drive segment output
  - 1 for DTMF output
  - 1 for TONE output
- Process: Silicon gate CMOS
- Package: 84-QFP
- Piggyback: EP158414

■ Pin Configuration



(Top View)

⑰ 84-QFP

■ Pin Descriptions

Pin	Symbol	Pin name	I/O	Description
4 7	V_{DD} V_{SS}	Power supply	I	Connect +2.5-5.5 V to V_{DD}, and 0 V to V_{SS}
5 6	OSC1 OSC2	Clock input Clock output	I O	Oscillator terminals to connect f_{osc} ceramic oscillator or crystal oscillator. A feedback resistor is incorporated between OSC1 and OSC2.
8 9	XI XO	Clock input Clock output	I O	Event counter clock source terminals to connect a crystal oscillator. A feedback resistor is incorporated berween XI and XO. They serve as an operating clock source when XI/XO is specified by clock selection.
10	$\overline{RST}$	Reset input	I	Reset is applied if the "L" level is inputted over 1 machine cycle. A pull-up resistor is incorporated.
64	$\overline{SYNC}$ (P00)	Sync. signal output /output	O	An internal timing signal is outputted every machine cycle at reset time. Available as a normal output port after reset is cancelled.
81 82 83 84	$\overline{LRQ0}$ $\overline{IRQ1}$ $\overline{IRQ2}$ $\overline{IRQ3}$ (PC0 ~PC3)	External interrupt/input	I	External interrupt terminals which receives an interrupt at a negative edge. Also available as as a normal input port.
1	$\overline{SBI}$ (PE0)	Serial interface data input/input		Serial interface receive data input terminal which inputs 8-bit serial data. Also available as a normal input port.
2	$\overline{SBO}$ (PE1)	Serial interface data output/input	O /I	Serial interface send data output terminal which outputs 8-bit serial data. Can be set to high impedance when no data is outputted. Also available as a normal input port.
3	$\overline{SBT}$ (PE1)		I/O /I	Clock I/O terminal for sending or receiving of Serial Interface. In internal clock mode, it is output terminal and in external clock mode, it is input terminal.
50	DTMF	DTMF signal output	O	A DTMF signal is outputted. When DTMF is used, source oscillation of 3.58 MHz is used.
49 48 47	$V_{LCD}1$ $V_{LCD}2$ $V_{LCD}3$	LCD power suppy	I	LCD drive power supply terminals $V_{LCD1}=V_{DD}-(1/3)V_{LCD}$, $V_{LCD2}=V_{DD}-(2/3)V_{LCD}$, $V_{LCD3}=V_{DD}-V_{LCD}$ (V_{LCD} : LCD drive voltage)
43~46	COM0~ COM3	LCD common output	O	LCD Common signal output terminals
11~42	SEG0~ SEG31	LCD segment output	O	LCD segment signal output terminals
51	TONE	TONE output	O	Enables programmable setting of pulse output of 694.8 to 1,639.0 Hz(source oscillation: 3.58 MHz), same as DTMF output. Output can be turned on/off by controlling the port P30.
64~67 68~71	P00~P03 P10~P13	Parallel data output	O	4-bit parallel data output ports. Push-pull output. High impedance at reset time.
60~63 72~75	P20~P23 P50~P53	Parall data I/O	I/O	4-bit parallel data input or output ports. P20-P23 and P50-P53 can be I/O-selected at P32 and P33, respectively. High impedance at reset time.

■ Pin Descriptions(Continued)

Pin	Symbol	Pin name	I/O	Description
52~55 56~59	P30~P33 P40~P43	Parallel data input	I	4-bit parallel data input ports. No pull-up resistor is incor-porated.
76 77~80	P60 P70~P73	Parallel data output	O	4-bit parallel data output ports. 12 V breckdown N-channel open drain output. High impedance at reset time.
81~84	PC0~PC3	Parallel data output	I	4-bit parallel data input ports. These ports are jointly used as $\overline{IRQ0}$, $\overline{IRQ1}$, $\overline{IRQ2}$ and $\overline{IRQ3}$, respectively. No pull-up resistor is incorporated.
1~3	PE0~PE2	Parallel data input	I	3-bit Parallel data input ports. These ports are jointly used as $\overline{SBI}$, $\overline{SBO}$ and $\overline{SBT}$, respectively. No pull-up resistor is incorporated.

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