OP-177

ULTRA-PRECISION OPERATIONAL AMPLIFIER

FEATURES

- **Ultra-Low Offset Voltage**
  - T_A = 25°C ..... 10μV Max
  - −55°C ≤ T_A ≤ 125°C ..... 20μV Max
- **Outstanding Offset Voltage Drift** ..... 0.1μV/°C Max
- **Excellent Open-Loop Gain and Gain Linearity** ..... 12V/μV Typ
- **CMRR** ..... 130dB Min
- **PSRR** ..... 120dB Min
- **Low Supply Current** ..... 2.0 mA Max
- **Fits Industry Standard Precision Op Amp Sockets (OP07/OP77)**

ORDERING INFORMATION †

PACKAGE				OPERATING
CERDIP 8-PIN	PLASTIC 8-PIN	LCC 20-PIN	SO 8-PIN	TEMPERATURE RANGE
OP177AZ*	–	–	–	MIL
OP177BZ*	–	OP177BRC/883	–	MIL
OP177EZ	–	–	–	XIND
OP177FZ	OP177FP	–	–	XIND
OP177GZ	OP177GP	–	OP177GS	XIND

MIL = −55°C to +125°C XIND = −40°C to +85°C

* For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

† Burn-in is available on commercial and industrial temperature range parts in cerDIP, plastic DIP, and TO-can packages. For ordering information, see PMI's Data Book, Section 2.

GENERAL DESCRIPTION

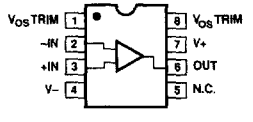
The OP-177 features the highest precision performance of any op amp currently available. Offset voltage of the OP-177 is only 10μV MAX at room temperature and 20μV MAX over the full military temperature range of −55°C to +125°C. The ultra-low V_{OS} of the OP-177, combines with its exceptional offset voltage drift (TCV_{OS}) of 0.1μV/°C MAX, to eliminate the need for external V_{OS} adjustment and increases system accuracy over temperature.

The OP-177's open-loop gain of 12V/μV is maintained over the full ±10V output range. CMRR of 130dB MIN, PSRR of 120dB MIN, and maximum supply current of 2mA are just a few examples of the excellent performance of this operational amplifier. The OP-177's combination of outstanding specifications insure accurate performance in high closed-loop gain applications.

This low noise bipolar input op amp is also a cost effective alternative to chopper-stabilized amplifiers. The OP-177 provides chopper-type performance without the usual problems of high noise, low frequency chopper spikes, large physical size, limited common-mode input voltage range, and bulky external storage capacitors.

Continued

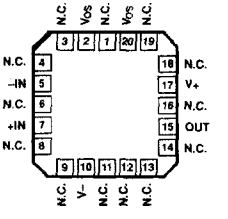
PIN CONNECTIONS



EPOXY MINI-DIP (P-Suffix)

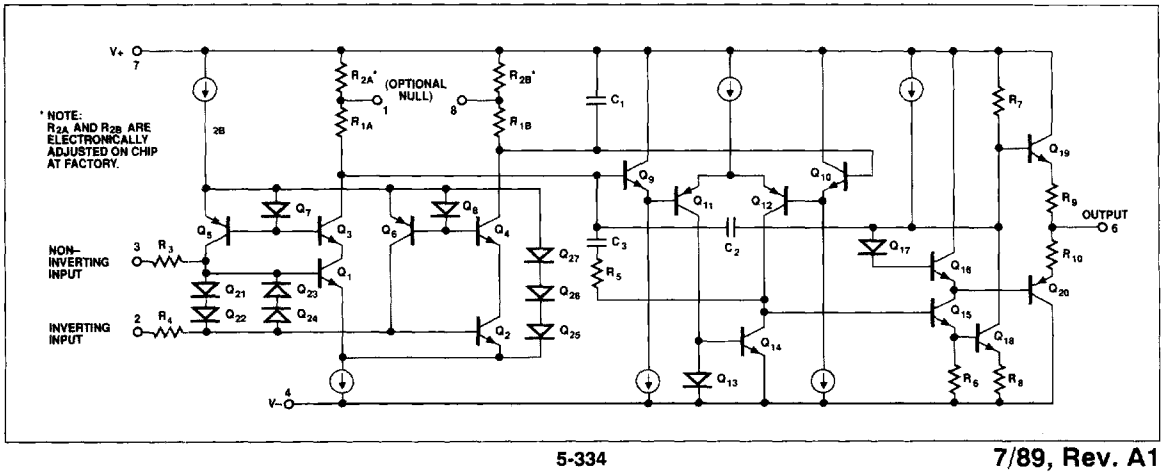
8-PIN HERMETIC DIP (Z-Suffix)

8-PIN SO (S-Suffix)



OP-177BRC/883 LCC (RC-Suffix)

SIMPLIFIED SCHEMATIC



GENERAL DESCRIPTION *Continued*

The OP-177 is offered in both the –55°C to +125°C military, and the –40°C to +85°C extended industrial temperature ranges. This product is available in 8-pin ceramic and epoxy DIPs, as well as the space saving 8-pin Small-Outline (SO) and the Leadless Chip Carrier (LCC) packages.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±22V
Output Short-Circuit Duration ..... Indefinite
Storage Temperature Range
Z and RC Packages ..... –65°C to +150°C
P Package ..... –65°C to +125°C
Operating Temperature Range
OP-177A, OP-177B ..... –55°C to +125°C
OP-177E, OP-177F, OP-177G ..... –40°C to +85°C
Lead Temperature Range (Soldering, 60 sec) ..... 300°C
Junction Temperature (T_j) ..... –65°C to +150°C

PACKAGE TYPE	Θ_{JA} (NOTE 2)	Θ_{JC}	UNITS
8-Pin Hermetic DIP (Z)	148	16	°C/W
8-Pin Plastic DIP (P)	103	43	°C/W
20-Contact LCC (RC)	98	38	°C/W
8-Pin SO (S)	158	43	°C/W

NOTES:
1. For supply voltages less than ±22V, the absolute maximum input voltage is equal to the supply voltage.
2. Θ_{JA} is specified for worst case mounting conditions, i.e., Θ_{JA} is specified for device in socket for CerDIP, P-DIP, and LCC packages; Θ_{JA} is specified for device soldered to printed circuit board for SO package.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177A MIN	OP-177A TYP	OP-177A MAX	OP-177B MIN	OP-177B TYP	OP-177B MAX	UNITS
Input Offset Voltage	V_{OS}		–	4	10	–	10	25	µV
Long-Term Input Offset Voltage Stability	ΔV_{OS}/Time	(Note 1)	–	0.2	–	–	0.2	–	µV/Mo
Input Offset Current	I_{OS}		–	0.3	1.0	–	0.3	1.5	nA
Input Bias Current	I_B		–0.2	–	1.5	–0.2	–	2.0	nA
Input Noise Voltage	e_n	f_o = 1Hz to 100Hz (Note 2)	–	118	150	–	118	150	nV_{RMS}
Input Noise Current	i_n	f_o = 1Hz to 100Hz (Note 2)	–	3	8	–	3	8	pA_{RMS}
Input Resistance Differential-Mode	R_{IN}	(Note 3)	26	45	–	26	45	–	MΩ
Input Resistance Common-Mode	R_{INCM}		–	200	–	–	200	–	GΩ
Input Voltage Range	IVR	(Note 4)	±13	±14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	130	140	–	130	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	115	125	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V (Note 5)	5000	12000	–	5000	12000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ R_L ≥ 2kΩ R_L ≥ 1kΩ	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	±13.5 ±12.5 ±12.0	±14.0 ±13.0 ±12.5	– – –	V
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	–	0.1	0.3	–	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_{O}		–	60	–	–	60	–	Ω
Power Consumption	Pd	V_S = ±15V, No Load V_S = ±3V, No Load	– –	50 3.5	60 4.5	– –	50 3.5	60 4.5	mW
Supply Current	I_{SY}	V_S = ±15V, No Load	–	1.6	2.0	–	1.6	2.0	mA
Offset Adjustment Range		Rp = 20kΩ	–	±3	–	–	±3	–	mV

NOTES:
1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0µV.
2. Sample tested.
3. Guaranteed by design.
4. Guaranteed by CMRR test condition.
5. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at –10V ≤ V_O ≤ 0V, 0V ≤ V_O ≤ +10V, and –10V ≤ V_O ≤ +10V.

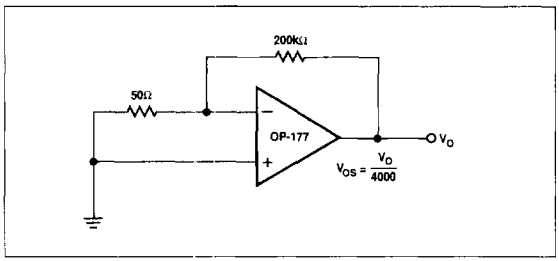
ELECTRICAL CHARACTERISTICS at $V_S = \pm15V$, $-55°C \le T_A \le +125°C$, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177A MIN	OP-177A TYP	OP-177A MAX	OP-177B MIN	OP-177B TYP	OP-177B MAX	UNITS
Input Offset Voltage	V_{OS}		–	10	20	–	25	55	µV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	–	0.03	0.1	–	0.1	0.3	µV/°C
Input Offset Current	I_{OS}		–	0.5	1.5	–	0.5	2.0	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	–	1.5	25	–	1.5	25	pA/°C
Input Bias Current	I_B		–0.2	2.4	4	–0.2	2.4	4	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	–	8	25	–	8	25	pA/°C
Input Voltage Range	IVR	(Note 3)	±13	±13.5	–	±13	±13.5	–	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = \pm13V$	120	140	–	120	140	–	dB
Power Supply Rejection Ratio	PSRR	$V_S = \pm3V$ to $\pm18V$	120	125	–	110	120	–	dB
Large-Signal Voltage Gain	A_{VO}	$R_L \ge 2k\Omega$, $V_O = \pm10V$ (Note 4)	2000	6000	–	2000	6000	–	V/mV
Output Voltage Swing	V_O	$R_L \ge 2k\Omega$	±12	±13.0	–	±12	±13.0	–	V
Power Consumption	P_d	$V_S = \pm15V$, No Load	–	60	75	–	60	75	mW
Supply Current	I_{SY}	$V_S = \pm15V$, No Load	–	2.0	2.5	–	2.0	2.5	mA

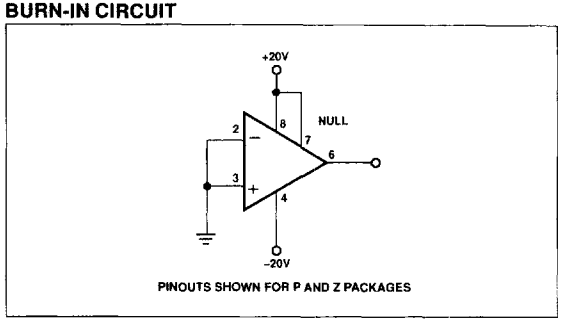
NOTES:

1. TCV_{OS} is 100% tested.
2. Guaranteed by end-point limits.
3. Guaranteed by CMRR test condition.
4. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$.

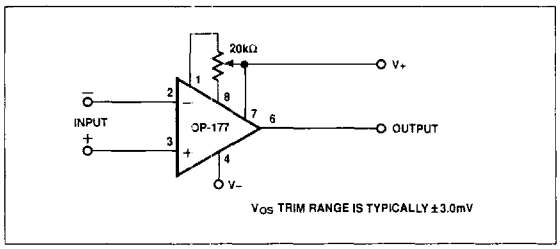
TYPICAL OFFSET VOLTAGE TEST CIRCUIT



BURN-IN CIRCUIT



OPTIONAL OFFSET NULLING CIRCUIT



ELECTRICAL CHARACTERISTICS at V_S = ±15V, T_A = +25°C, unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	OP-177E MIN	OP-177E TYP	OP-177E MAX	OP-177F MIN	OP-177F TYP	OP-177F MAX	OP-177G MIN	OP-177G TYP	OP-177G MAX	UNITS
Input Offset Voltage	V_{OS}		–	4	10	–	10	25	–	20	60	µV
Long-Term V_{OS} Stability	V_{OS}/Time	(Note 1)	–	0.2	–	–	0.3	–	–	0.4	–	µV/Mo
Input Offset Current	I_{OS}		–	0.3	1.0	–	0.3	1.5	–	0.3	2.8	nA
Input Bias Current	I_B		–0.2	1.0	1.5	–0.2	1.2	2.0	–0.2	1.2	2.8	nA
Input Noise Voltage	e_n	f_o = 1Hz to 100Hz (Note 2)	–	118	150	–	118	150	–	118	150	nV_{RMS}
Input Noise Current	i_n	f_o = 1Hz to 100Hz (Note 2)	–	3	8	–	3	8	–	3	8	pA_{RMS}
Input Resistance – Differential-Mode	R_{IN}	(Note 3)	26	45	–	26	45	–	18.5	45	–	MΩ
Input Resistance – Common-Mode	R_{INCM}		–	200	–	–	200	–	–	200	–	GΩ
Input Voltage Range	IVR	(Note 4)	±13	±14	–	±13	±14	–	±13	±14	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	130	140	–	130	140	–	115	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	115	125	–	110	120	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ, V_O = ±10V (Note 5)	5000	12000	–	5000	12000	–	2000	6000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 10kΩ	±13.5	±14.0	–	±13.5	±14.0	–	±13.5	±14.0	–	V
		R_L ≥ 2kΩ	±12.5	±13.0	–	±12.5	±13.0	–	±12.5	±13.0	–	
		R_L ≥ 1kΩ	±12.0	±12.5	–	±12.0	±12.5	–	±12.0	±12.5	–	
Slew Rate	SR	R_L ≥ 2kΩ (Note 2)	0.1	0.3	–	0.1	0.3	–	0.1	0.3	–	V/µs
Closed-Loop Bandwidth	BW	A_{VCL} = +1 (Note 2)	0.4	0.6	–	0.4	0.6	–	0.4	0.6	–	MHz
Open-Loop Output Resistance	R_O		–	60	–	–	60	–	–	60	–	Ω
Power Consumption	P_d	V_S = ±15V, No Load	–	50	60	–	50	60	–	50	60	mW
		V_S = ±3V, No Load	–	3.5	4.5	–	3.5	4.5	–	3.5	4.5	
Supply Current	I_{SY}	V_S = ±15V, No Load	–	1.6	2.0	–	1.6	2.0	–	1.6	2.0	mA
Offset Adjustment Range		R_P = 20kΩ	–	±3	–	–	±3	–	–	±3	–	mV

NOTES:

1. Long-Term Input Offset Voltage Stability refers to the averaged trend line of V_{OS} vs. Time over extended periods after the first 30 days of operation. Excluding the initial hour of operation, changes in V_{OS} during the first 30 operating days are typically less than 2.0µV.
2. Sample tested.
3. Guaranteed by design.
4. Guaranteed by CMRR test condition.
5. To insure high Open-loop gain throughout the ±10V output range, A_{VO} is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$.

ELECTRICAL CHARACTERISTICS at V_S = ±15V, –40°C ≤ T_A ≤ ±85°C, unless otherwise noted.

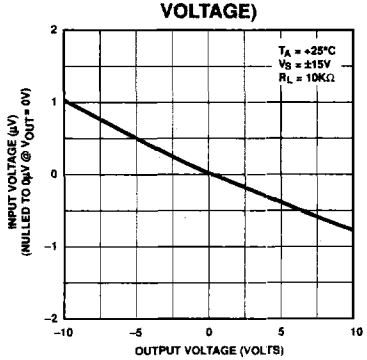
PARAMETER	SYMBOL	CONDITIONS	OP-177E MIN	OP-177E TYP	OP-177E MAX	OP-177F MIN	OP-177F TYP	OP-177F MAX	OP-177G MIN	OP-177G TYP	OP-177G MAX	UNITS
Input Offset Voltage	V_{OS}		–	10	20	–	15	40	–	20	100	µV
Average Input Offset Voltage Drift	TCV_{OS}	(Note 1)	–	0.03	0.1	–	0.1	0.3	–	0.7	1.2	µV/°C
Input Offset Current	I_{OS}		–	0.5	1.5	–	0.5	2.2	–	0.5	4.5	nA
Average Input Offset Current Drift	TCI_{OS}	(Note 2)	–	1.5	25	–	1.5	40	–	1.5	85	pA/°C
Input Bias Current	I_B		–0.2	2.4	4.0	–0.2	2.4	4.0	–	2.4	±6.0	nA
Average Input Bias Current Drift	TCI_B	(Note 2)	–	8	25	–	8	40	–	15	60	pA/°C
Input Voltage Range	IVR	(Note 3)	±13.0	±13.5	–	±13.0	±13.5	–	±13.0	±13.5	–	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = ±13V	120	140	–	120	140	–	110	140	–	dB
Power Supply Rejection Ratio	PSRR	V_S = ±3V to ±18V	120	125	–	110	120	–	106	115	–	dB
Large-Signal Voltage Gain	A_{VO}	R_L ≥ 2kΩ V_O = ±10V	2000	6000	–	2000	6000	–	1000	4000	–	V/mV
Output Voltage Swing	V_O	R_L ≥ 2kΩ	±12.0	±13.0	–	±12.0	±13.0	–	±12.0	±13.0	–	V
Power Consumption	P_d	V_S = ±15V, No Load	–	60	75	–	60	75	–	60	75	mW
Supply Current	I_{SY}	V_S = ±15V, No Load	–	2.0	2.5	–	2.0	2.5	–	2.0	2.5	mA

NOTES:

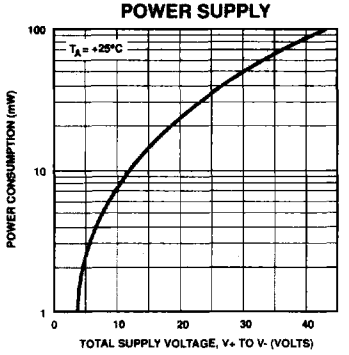
1. OP177E and OP177F: TCV_{OS} is 100% tested.
2. Guaranteed by end-point limits.
3. Guaranteed by CMRR test condition.
4. To insure high open-loop gain throughout the ±10V output range, A_{VO} is tested at $-10V \le V_O \le 0V$, $0V \le V_O \le +10V$, and $-10V \le V_O \le +10V$.

TYPICAL PERFORMANCE CHARACTERISTICS

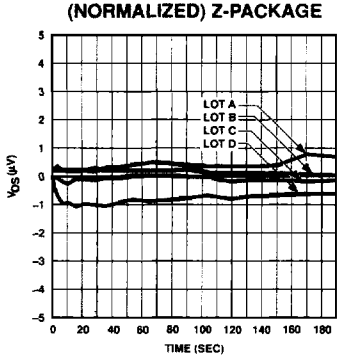
GAIN LINEARITY (INPUT VOLTAGE vs OUTPUT VOLTAGE)



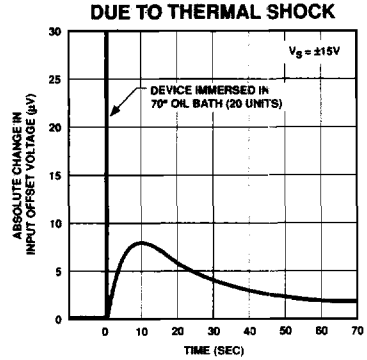
POWER CONSUMPTION vs POWER SUPPLY



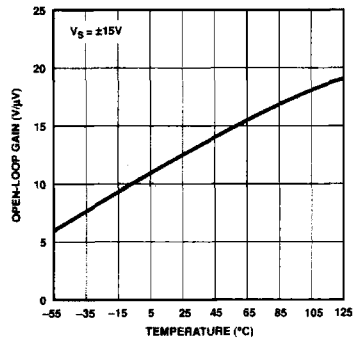
WARM-UP V_{OS} DRIFT (NORMALIZED) Z-PACKAGE



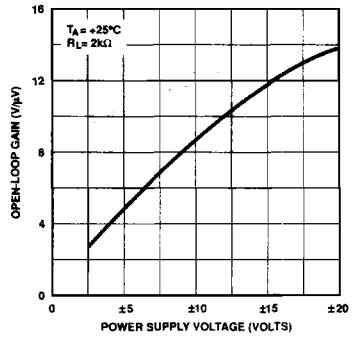
OFFSET VOLTAGE CHANGE DUE TO THERMAL SHOCK



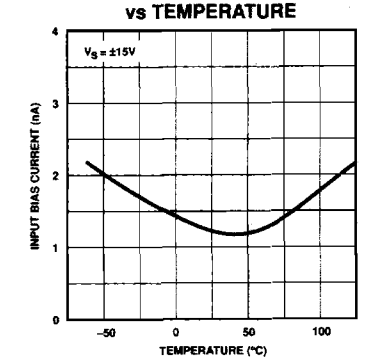
OPEN-LOOP GAIN vs TEMPERATURE



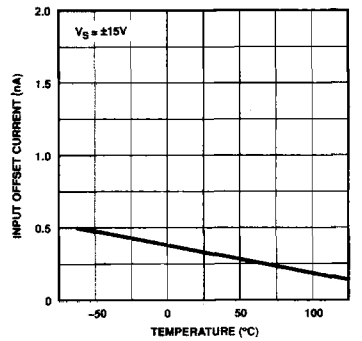
OPEN-LOOP GAIN vs POWER SUPPLY VOLTAGE



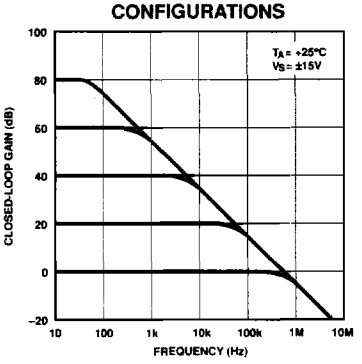
INPUT BIAS CURRENT vs TEMPERATURE



INPUT OFFSET CURRENT vs TEMPERATURE

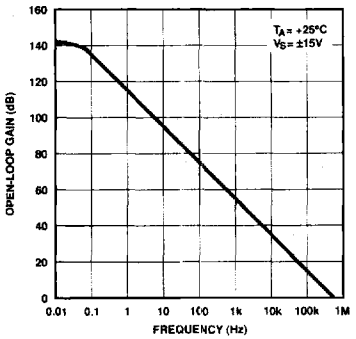


CLOSED-LOOP RESPONSE FOR VARIOUS GAIN CONFIGURATIONS

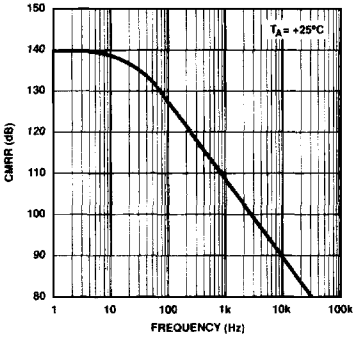


TYPICAL PERFORMANCE CHARACTERISTICS *Continued*

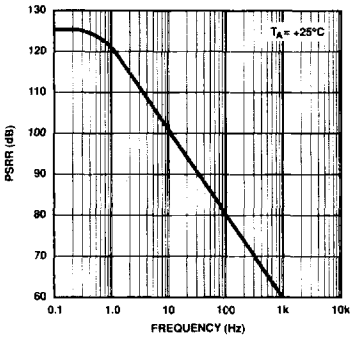
OPEN-LOOP FREQUENCY RESPONSE



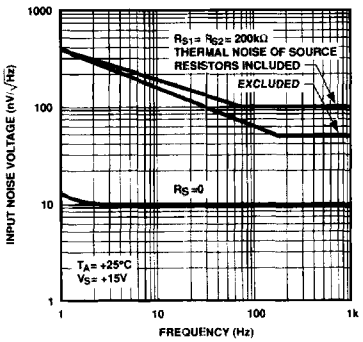
CMRR vs FREQUENCY



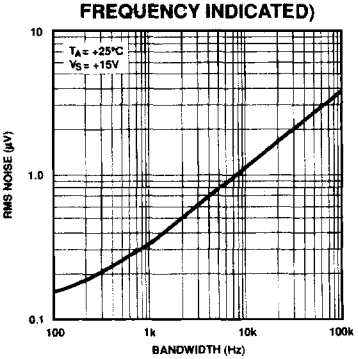
PSRR vs FREQUENCY



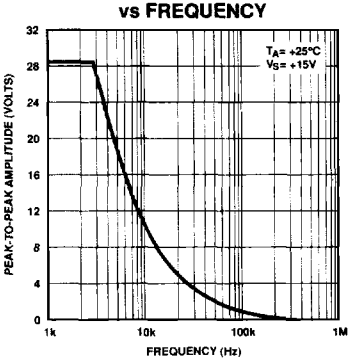
TOTAL INPUT NOISE VOLTAGE vs FREQUENCY



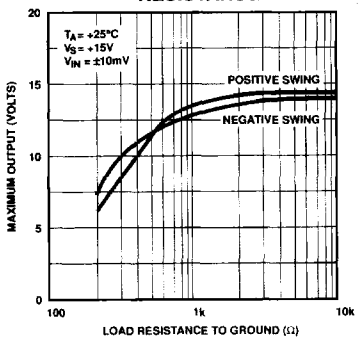
INPUT WIDEBAND NOISE vs BANDWIDTH (0.1 Hz TO FREQUENCY INDICATED)



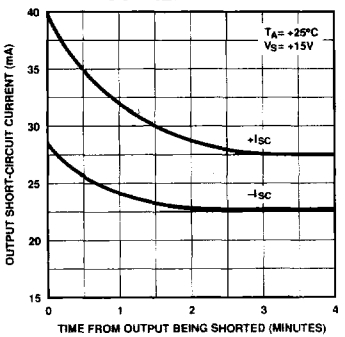
MAXIMUM OUTPUT SWING vs FREQUENCY



MAXIMUM OUTPUT VOLTAGE vs LOAD RESISTANCE



OUTPUT SHORT-CIRCUIT CURRENT vs TIME



APPLICATIONS INFORMATION

GAIN LINEARITY

The actual open-loop gain of most monolithic op amps varies at different output voltages. This nonlinearity causes errors in high closed-loop gain circuits.

It is important to know that the manufacturer's A_{VO} specification is only a part of the solution, since all automated testers use end-point testing and therefore only show the average gain. For example, Figure 1 shows a typical precision op amp with a respectable open-loop gain of 650V/mV. However, the gain is not constant through the output voltage range, causing nonlinear errors. An ideal op amp would show a horizontal scope trace.

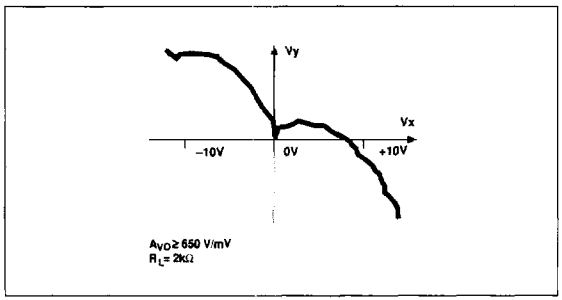


FIGURE 1: *Typical Precision Op-Amp*

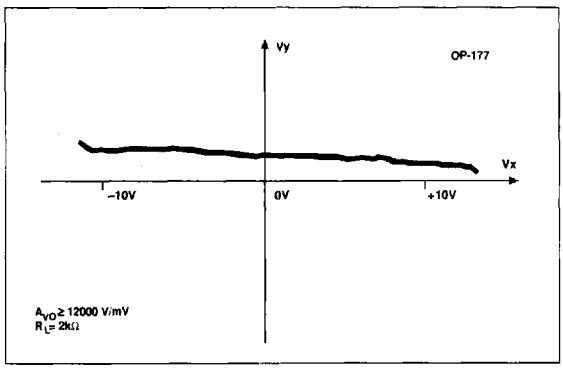


FIGURE 2: *OP-177's Output Gain Linearity Trace*

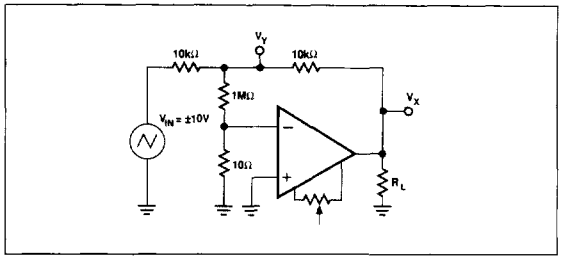


FIGURE 3: *Open-Loop Gain Linearity Test Circuit*

Figure 2 shows the OP-177's output gain linearity trace with its truly impressive average A_{VO} of 12000V/mV. The output trace is virtually horizontal at all points, assuring extremely high gain accuracy. PMI also performs additional testing to insure consistent high open-loop gain at various output voltages.

Figure 3 is a simple open-loop gain test circuit for your own evaluation.

THERMOCOUPLE AMPLIFIER WITH COLD-JUNCTION COMPENSATION

An example of a precision circuit is a thermocouple amplifier that must amplify very low level signals accurately without introducing linearity and offset errors to the circuit. In this circuit, an S-type thermocouple, which has a Seebeck coefficient of 10.3µV/°C, produces 10.3mV of output voltage at a temperature of 1,000°C. The amplifier gain is set at 973.16. Thus, it will produce an output voltage of 10.024V. Extended temperature ranges to beyond 1,500°C can be accomplished by reducing the amplifier gain. The circuit uses a low-cost diode to sense the temperature at the terminating junctions and in turn compensates for any ambient temperature change. The OP-177, with its high open-loop gain, plus low offset voltage and drift combines to yield a very precision temperature sensing circuit. Circuit values for other thermocouple types are shown in Table 1.

TABLE 1

THERMOCOUPLE TYPE	SEEBECK COEFFICIENT	R_1	R_2	R_7	R_9
K	39.2µV/°C	110Ω	5.76kΩ	102kΩ	269kΩ
J	50.2µV/°C	100Ω	4.02kΩ	80.6kΩ	200kΩ
S	10.3µV/°C	100Ω	20.5kΩ	392kΩ	1.07MΩ

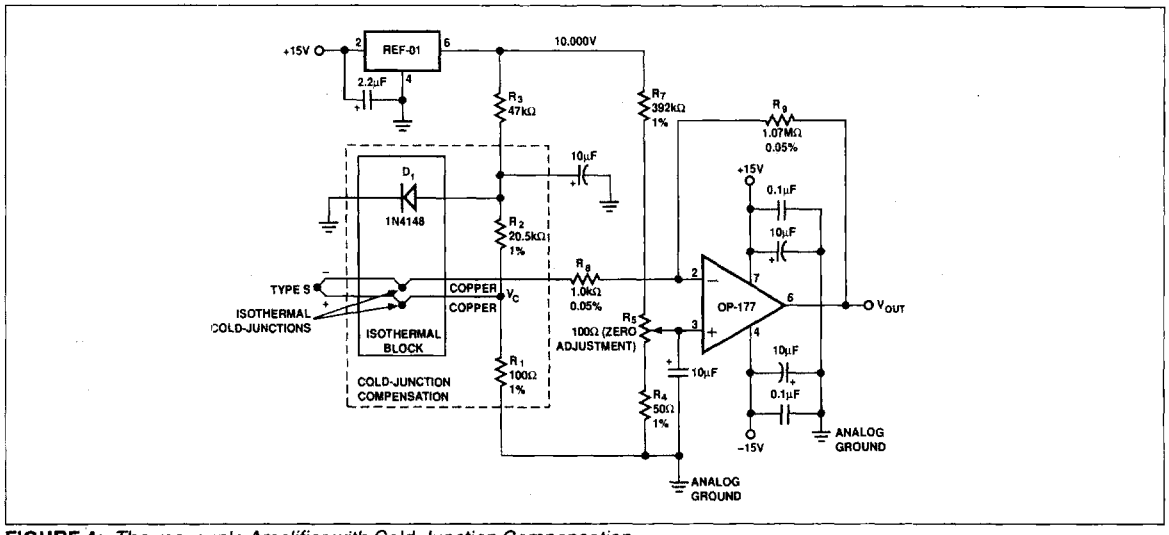


FIGURE 4: *Thermocouple Amplifier with Cold-Junction Compensation*

PRECISION HIGH-GAIN DIFFERENTIAL AMPLIFIER

The high gain, gain linearity, CMRR, and low TCV_{OS} of the OP-177 make it possible to obtain performance not previously available in single stage, very high-gain amplifier applications. See Figure 5.

For best CMR, $\frac{R_1}{R_2}$ must equal $\frac{R_3}{R_4}$. In this example, with a 10mV differential signal, the maximum errors are as listed in Table 2.

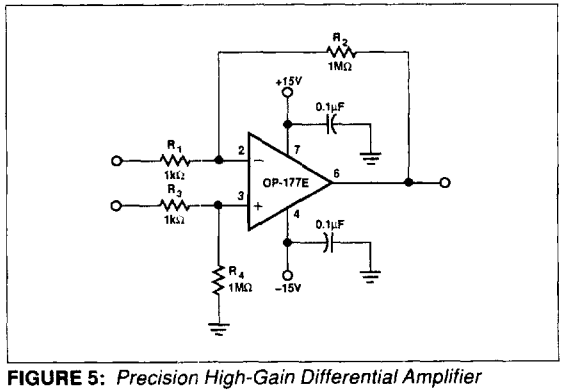


FIGURE 5: *Precision High-Gain Differential Amplifier*

TABLE 2: High Gain Differential Amp Performance

TYPE	AMOUNT
COMMON-MODE VOLTAGE	0.1%/V
GAIN LINEARITY, WORST CASE	0.02%
TCV_{OS}	0.0003%/°C
TCI_{OS}	0.008%/°C

ISOLATING LARGE CAPACITIVE LOADS

The circuit in Figure 6 reduces maximum slew-rate but allows driving capacitive loads of any size without instability. Because the 100Ω resistor is inside the feedback loop, its effect on output impedance is reduced to insignificance by the high open-loop gain of the OP-177.

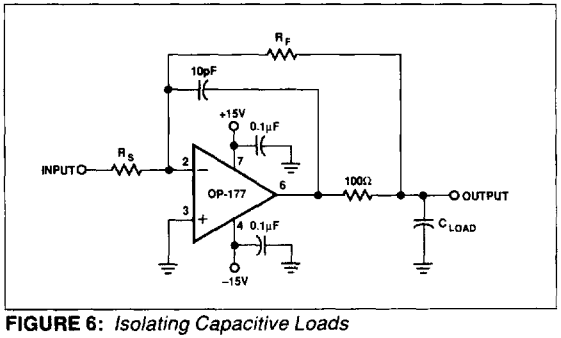


FIGURE 6: *Isolating Capacitive Loads*

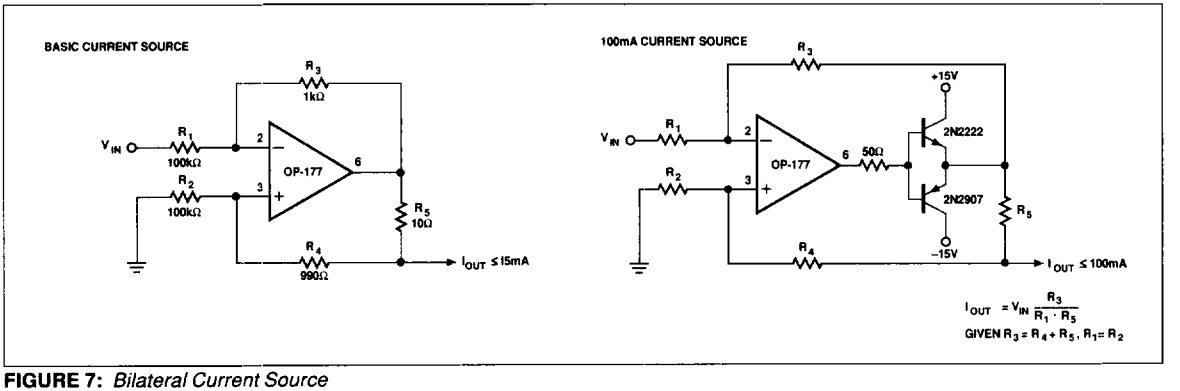


FIGURE 7: *Bilateral Current Source*

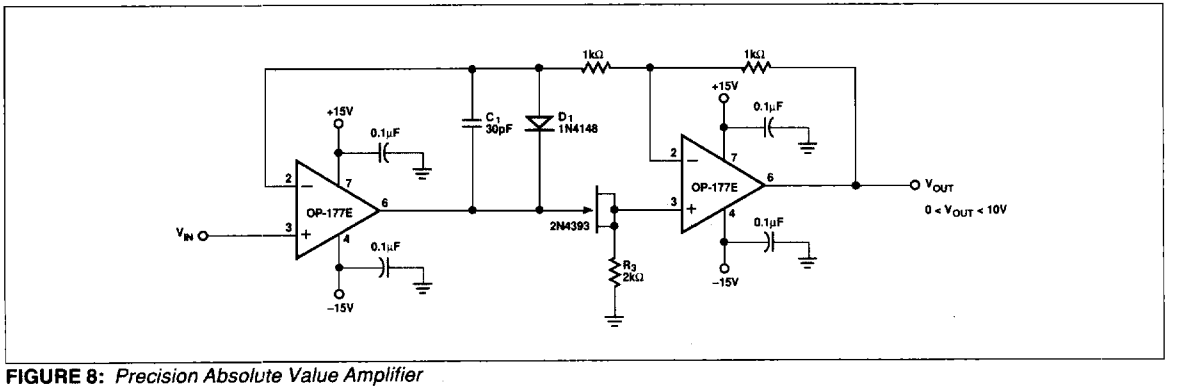


FIGURE 8: *Precision Absolute Value Amplifier*

BILATERAL CURRENT SOURCE

The current sources shown in Figure 7 will supply both positive and negative current into a grounded load.

Note that $Z_O = \dfrac{R_5\left(\dfrac{R_4}{R_2}+1\right)}{\dfrac{R_5+R_4}{R_2}-\dfrac{R_3}{R_1}}$

and that for Z_O to be infinite,

$\dfrac{R_5+R_4}{R_2}$ must $= \dfrac{R_3}{R_1}$

PRECISION ABSOLUTE VALUE AMPLIFIER

The high gain and low TCV_{OS} assure accurate operation with inputs from microvolts to volts. In this circuit, the signal always appears as a common-mode signal to the op amps. The OP-177E CMRR of 140dB assures errors of less than 1ppm. See Figure 8.

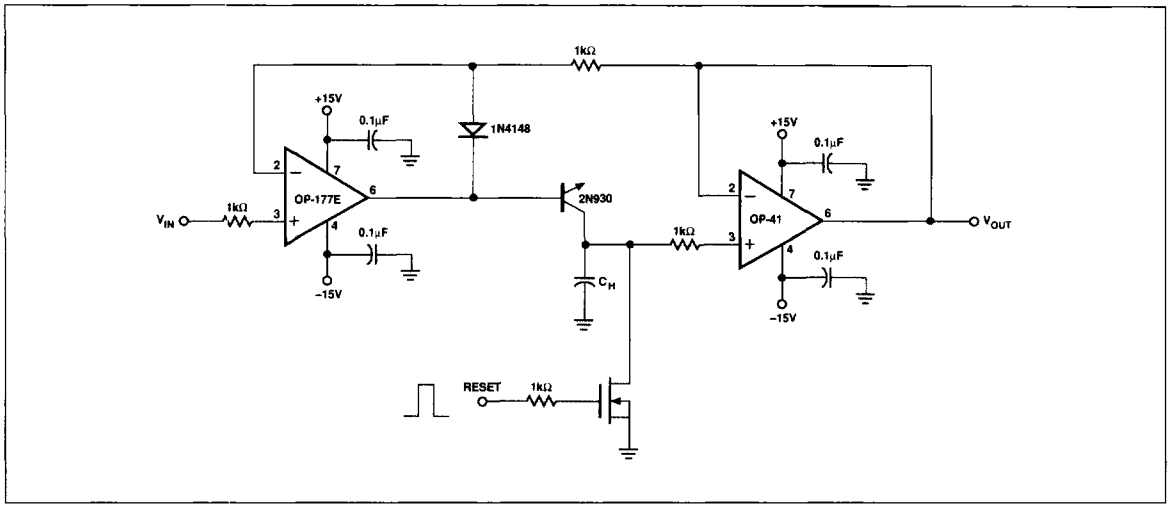


FIGURE 9: *Precision Positive Peak Detector*

PRECISION POSITIVE PEAK DETECTOR

In Figure 9, the C_H must be of polystyrene, Teflon*, or polyethylene to minimize dielectric absorption and leakage. The droop rate is determined by the size of C_H and the bias current of the OP-41.

PRECISION THRESHOLD DETECTOR/AMPLIFIER

In Figure 10, when $V_{IN} < V_{TH}$, amplifier output swings negative, reverse biasing diode D_1. $V_{OUT} = V_{TH}$ if $R_L = \infty$. When $V_{IN} \geq V_{TH}$, the loop closes,

$$V_{OUT} = V_{TH} + (V_{IN} - V_{TH})\left(1 + \frac{R_F}{R_S}\right)$$

C_C is selected to smooth the response of the loop.

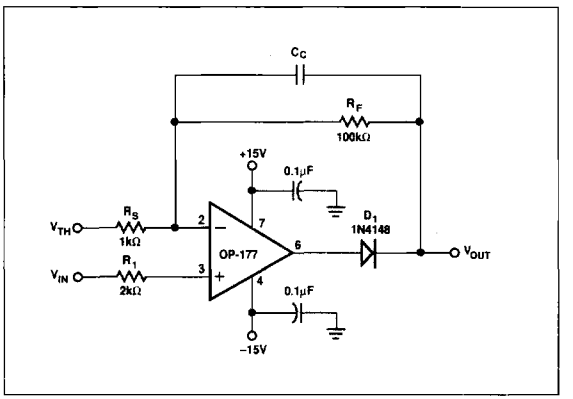


FIGURE 10: *Precision Threshold Detector/Amplifier*

*Teflon is a registered trademark of the Dupont Company