PAS6352 CMOS VGA IMAGE SENSOR

General Description

The PAS6352 is a highly integrated CMOS active-pixel image sensor that has output of 640 x 480 pixels. It embedded the new FinePixel™ sensor technology to perform the excellent image quality. PAS6352 outputs 10-bit RGB raw or YUV/YCrCb 4:2:2 or RGB565/555/444 data through a parallel data bus. It is available in CSP package.

The PAS6352 can be programmed to set the exposure time for different luminance condition via I2C™ serial control bus. By programming the internal register set, it performs on-chip frame rate adjustment and programmable gain control.

Features

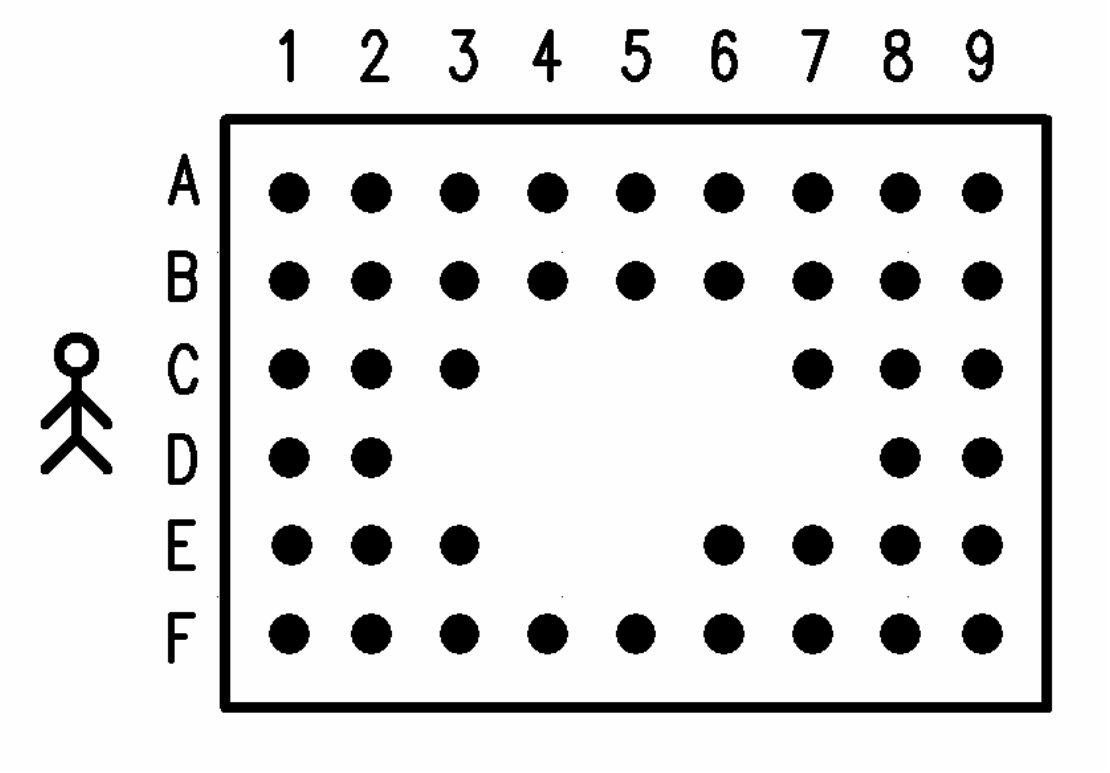
- Active Pixels: 648 x 488 pixels
- Resolution: 640 x 480 pixels, 1/4" Lens
- Bayer-RGB color filter array
- Output format :
  - RAW, 10-bit
  - YUV/YCrCb 4:2:2
  - RGB565/555/444
- On-chip 10-bit pipelined A/D converter
- On-chip manual analog gain control
- Continuous variable frame time & exposure time
- I2C™ Interface
- Support 1.7V~3.3V I/O
- Power dissipation: operating typ. TBD@ 2.8V (VGA YUV 60fps parallel-output, without loading), low power-down dissipation typ./max. TBD @ 2.8V
- Automatic Background Compensation
- ISP function:
  - AEC & AGC
  - AWB
  - Gamma
  - Color matrix
  - Sharpness
  - De-noise
  - Color saturation
  - Defect compensation
  - Lens shading compensation
  - Auto de-flicker
  - Decimation-AVG and Scaler
  - DRC (Dynamic Range Compensation)
  - WOI & Sub-sampling
- Dummy line & pixel timing
- Output Hsync at Vsync
- PLL
- Module size : TBD

Key Specification

Active Pixel		648(H) x 488(V)
Resolution		640 (H) x 480 (V)
Power	Analog	2.8V
	I/O	1.7V ~ 3.3V
	Core	1.8V
[Array diagonal]		1/4" Lens
Pixel Size		5.6um * 5.6um
Lens Chief Ray Angle		TBD
Max. Frame rate		VGA 60fps
Max. input clock		48 MHz
Max. Pixel clock		48 MHz, VGA YUV 60fps
Sensitivity		TBD
Color filter		RGB Bayer Pattern
Exposure Time		TBD
Scan Mode		Progressive
S/N Ratio		TBD
Dynamic range		TBD
Package		CSP

PixArt Imaging Inc.
E-mail: fae_service@pixart.com.tw

1. Pin Assignment



PAS6352LT (Top-view)

Pin No.	Name	Type	Description
A1	VDD18K_I	PWR	Digital core power, 1.8V typical
A2	VSSD	GND	Ground
A3	PXD11	OUT	Digital pixel data [5]
A4	PXD9	OUT	Digital pixel data [3]
A5	IOVDD	PWR	I/O power, 2.8V typical
A6	PXCLK	OUT	Pixel clock output
A7	PXD6	OUT	Digital pixel data [0], LSB
A8	VSSD	GND	Ground
A9	VDD18K_I	PWR	Digital core power, 1.8V typical
B1	HSYNC	OUT	Horizontal synchronization signal output
B2	PXD13	OUT	Digital pixel data [7], MSB
B3	VSYNC	OUT	Vertical synchronization signal output
B4	PXD8	OUT	Digital pixel data [2]
B5	PXD7	OUT	Digital pixel data [1]
B6	PXD4	OUT	Digital pixel data for raw mode
B7	PXD5	OUT	Digital pixel data for raw mode
B8	DVDD28	PWR	Main power, 2.8V typical
B9	SYSCLK	IN	External clock input
C1	PXD2	--	NC
C2	VSSD	GND	Ground

C3	PXD10	OUT	Digital pixel data [4]
C7	PXD12	OUT	Digital pixel data [6]
C8	VSSD	GND	Ground
C9	PXD3	--	NC
D1	IOVDD	PWR	I/O power, 2.8V typical
D2	VDD18K_I	PWR	Digital core power, 1.8V typical
D8	VDDREF	Ref	Voltage reference
D9	IOVDD	PWR	I/O power, 2.8V typical
E1	SDA	I/O	I2C data
E2	SCL	IN	I2C clock input
E3	FSOURCE	--	NC
E6	VSSD	GND	Ground
E7	VSSD	GND	Ground
E8	VDDAY	Ref	Voltage reference
E9	VSSA	GND	Ground
F1	AVDD28	PWR	Main power, 2.8V typical
F2	VSSA	GND	Ground
F3	RSTN	IN	Chip reset mode enable, active low
F4	FRAMESYNC	--	Test pin
F5	IOVDD	PWR	I/O power, 2.8V typical
F6	VSSD	GND	Ground
F7	CSB	IN	Power down mode enable, active high
F8	VSSAY	GND	Ground
F9	AVDD28	PWR	Main power, 2.8V typical

2. I2C™ Bus

PAS6352 supports I2C bus transfer protocol and acts as slave device. The 7-bits unique slave address is "1000000" and supports receiving / transmitting speed as maximum 400KHz.

I2C Bus Overview

- Only two wires SDA (serial data) and SCL (serial clock) carry information between the devices connected to the I2C bus. Normally both SDA and SCL lines are open collector structure and pulled high by external pull-up resistors.
- Only the master can initiates a transfer (start), generates clock signals, and terminates a transfer (stop).
- Start and stop condition : A high to low transition of the SDA line while SCL is high defines a start condition. A low to high transition of the SDA line while SCL is high defines a stop condition. Please refer to Figure 2.1.
- Valid data : The data on the SDA line must be stable during the high period of the SCL clock. Within each byte, MSB is always transferred first. Read / Write control bit is the LSB of the first byte. Please refer to Figure 2.2.
- Both the master and slave can transmit and receive data from the bus.
- Acknowledge : The receiving device should pull down the SDA line during high period of the SCL clock line when a complete byte was transferred by transmitter. In the case of a master received data from a slave, the master does not generate an acknowledgment on the last byte to indicate the end of a master read cycle.

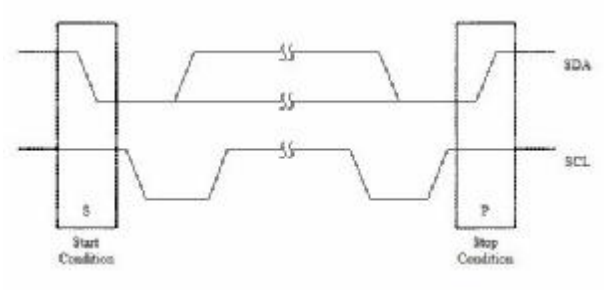


Figure 2.1 Start and Stop conditions

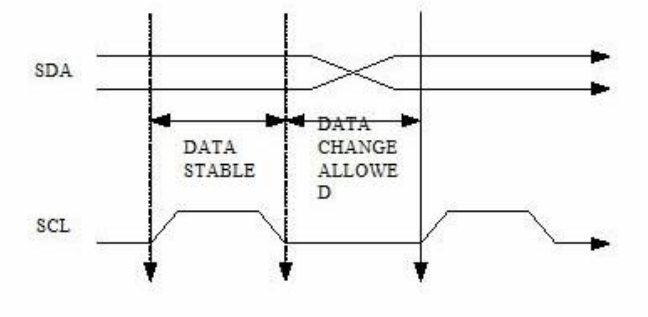
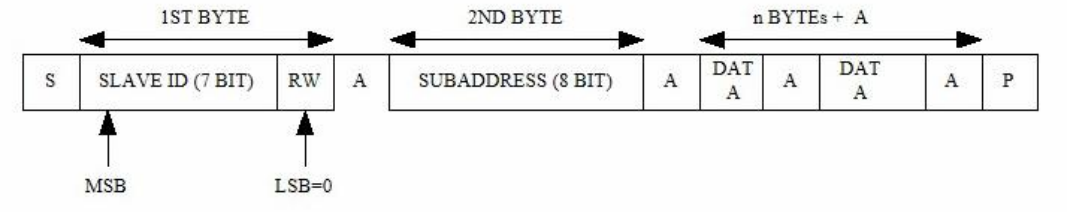


Figure 2.2 Valid Data

Data Transfer Format

Master transmits data to salve (write cycle)

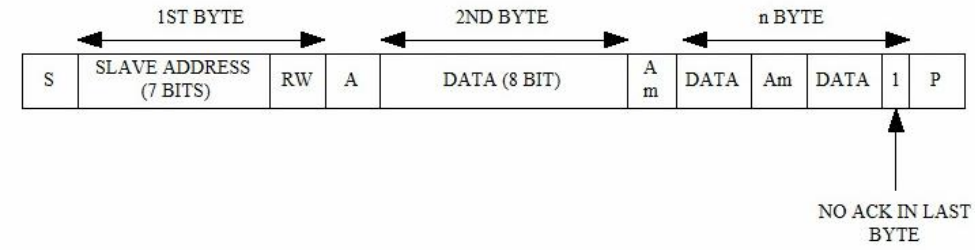
- S : Start.
- A : Acknowledge by salve.
- P : Stop.
- RW : The LSB of 1ST byte to decide whether current cycle is read or write cycle. RW = 1 – Read cycle, RW = 0 – Write cycle.
- SUBADDRESS : The address values of PAS6352 internal control registers. (Please refer to PAS6352 register description)



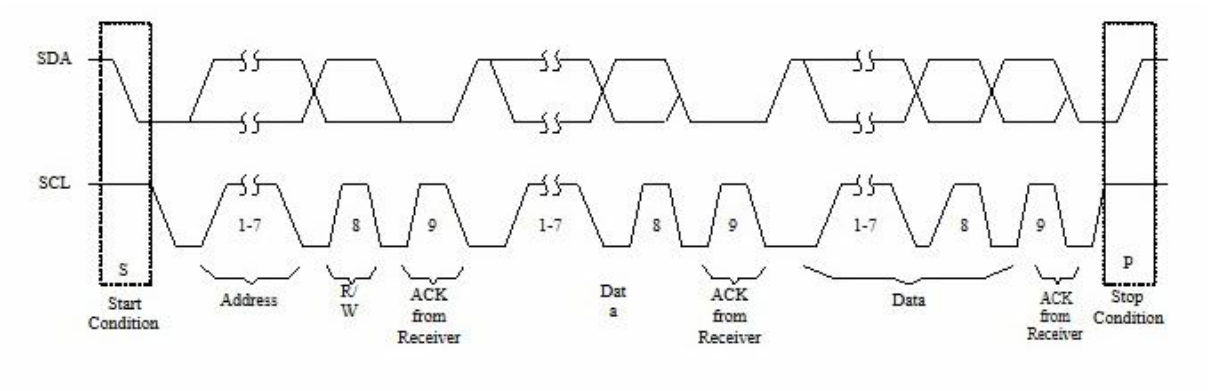
During write cycle, the master generates start condition and then places the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After slave (PAS6352) issues acknowledgment, the master places 2nd byte (Sub Address) data on SDA line. Again follow the PAS6352 acknowledgment, the master places the 8 bits data on SDA line and transmit to PAS6352 control register (address was assigned by 2nd byte). After PAS6352 issues acknowledgment, the master can generate a stop condition to end of this write cycle. In the condition of multi-byte write, the PAS6352 sub-address is automatically increment after each DATA byte transferred. The data and A cycles is repeat until last byte write. Every control registers value inside PAS6352 can be programming via this way.

Slave transmits data to master (read cycle)

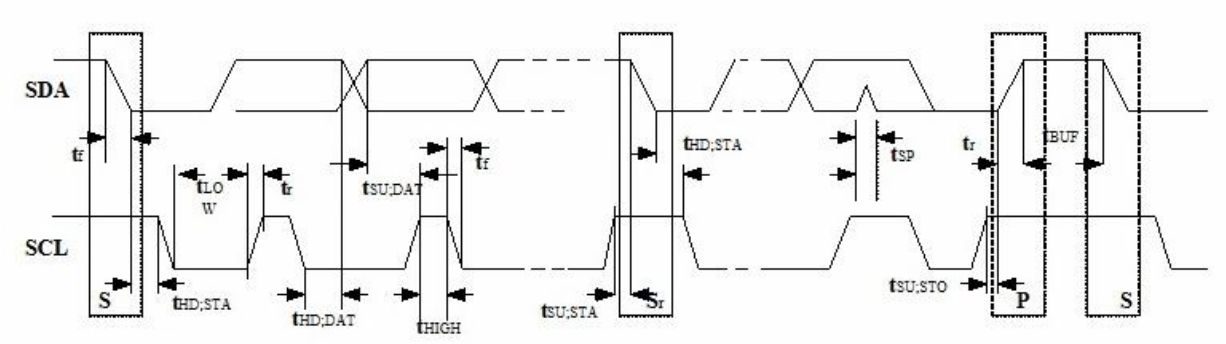
- The sub-address was taken from previous write cycle.
- The sub-address is automatically increment after each byte read.
- Am : Acknowledge by master.
- Note there is no acknowledgment from master after last byte read.



During read cycle, the master generates start condition and then place the 1st byte data that are combined slave address (7 bits) with a read / write control bit to SDA line. After issue acknowledgment, 8 bits DATA was also placed on SDA line by PAS6352. The 8 bits data was read from PAS6352 internal control register that address was assigned by previous write cycle. Follow the master acknowledgment, the PAS6352 place the next 8 bits data (address is increment automatically) on SDA line and then transmit to master serially. The DATA and Am cycles is repeat until the last byte read. After last byte read, Am is no longer generated by master but instead by keep SDA line high. The slave (PAS6352) must releases SDA line to master to generate STOP condition.



I2C™ Bus Timing



I2C™ Bus Timing Specification

Parameter	Symbol	Standard Mode		Unit
		Min.	Max	
SCL clock frequency.	f_{scl}	10	400	KHz
Hold time (repeated) Start condition. After this period, the first clock pulse is generated.	$t_{HD:STA}$	4.0	-	µs
Low period of the SCL clock.	t_{LOW}	4.7	-	µs
High period of the SCL clock.	t_{HIGH}	0.75	-	µs
Set-up time for a repeated START condition.	$t_{SU;STA}$	4.7	-	µs
Data hold time. For I2C-bus device.	$t_{HD;DAT}$	0	3.45	µs
Data set-up time.	$t_{SU;DAT}$	250	-	ns
Rise time of both SDA and SCL signals.	t_r	30	N.D.	ns (notel)
Fall time of both SDA and SCL signals.	t_f	30	N.D.	ns (notel)
Set-up time for STOP condition.	$t_{SU;STO}$	4.0	-	µs
Bus free time between a STOP and START.	t_{BUF}	4.7	-	µs
Capacitive load for each bus line.	C_b	1	15	pF
Noise margin at LOW level for each connected device. (Including hysteresis)	V_{nL}	0.1 VDD	-	V
Noise margin at HIGH level for each connected device. (including hysteresis)	V_{nH}	0.2 VDD	-	V

Note : It depends on the “high” period time of SCL.

3. Registers

Register Table

Bank	Address		Register Name	Description
0	F	[7:0]	R_AWB_Window_X[7:0]	AWB window width (by4)
0	11	[7:0]	R_AWB_Window_Y[7:0]	AWB window height (by4)
0	19	[7:0]	R_AWB_DGnR_LB_by2[7:0]	AWB digital gain lower bound for R
0	1A	[7:0]	R_AWB_DGnR_UB_by2[7:0]	AWB digital gain upper bound for B
0	1B	[7:0]	R_AWB_DGnB_LB_by2[7:0]	AWB digital gain lower bound for B
0	1C	[7:0]	R_AWB_DGnB_UB_by2[7:0]	AWB digital gain upper bound for R
0	1F	[4]	R_DeNoiseEn	DeNoise Enable
0	20	[7:0]	R_DeNoise_Str__G[7:0]	Denoise Strength (for color G)
0	23	[7:0]	R_DeNoise_Str__RB[7:0]	Denoise Strength (for color R/B)
0	28	[7:0]	R_ISP_YED	ISP Gamma YED (256)
0	29	[0]	R_ISP_Gamma_EnH	ISP gamma correction enable
0	2A	[7:0]	R_ISP_Y00	ISP Gamma Y0 (4)
0	2B	[7:0]	R_ISP_Y01	ISP Gamma Y1 (8)
0	2C	[7:0]	R_ISP_Y02	ISP Gamma Y2 (16)
0	2D	[7:0]	R_ISP_Y03	ISP Gamma Y3 (32)
0	2E	[7:0]	R_ISP_Y04	ISP Gamma Y4 (40)
0	2F	[7:0]	R_ISP_Y05	ISP Gamma Y5 (48)
0	30	[7:0]	R_ISP_Y06	ISP Gamma Y6 (56)
0	31	[7:0]	R_ISP_Y07	ISP Gamma Y7 (64)
0	32	[7:0]	R_ISP_Y08	ISP Gamma Y8 (80)
0	33	[7:0]	R_ISP_Y09	ISP Gamma Y9 (96)
0	34	[7:0]	R_ISP_Y10	ISP Gamma Y10 (112)
0	35	[7:0]	R_ISP_Y11	ISP Gamma Y11 (128)
0	36	[7:0]	R_ISP_Y12	ISP Gamma Y12 (160)
0	37	[7:0]	R_ISP_Y13	ISP Gamma Y13 (192)
0	38	[7:0]	R_ISP_Y14	ISP Gamma Y14 (224)
0	47	[1:0]	R_AWB_Speed	AWB adjust speed. The more, the slower 0: 1 x 1: 1/2 x 2: 1/4 x 3: 1/8 x
0	49	[7:0]	R_AWB_SumRatio_B	AWB B sum ratio = 128/X
0	4A	[7:0]	R_AWB_SumRatio_R	AWB R sum ratio = 128/X
0	4D	[7:0]	R_AWB_CbThdL[7:0]	AWB region test Cb Low threshold -128 ~ +127 (2's complement)
0	4E	[7:0]	R_AWB_CrThdL[7:0]	AWB region test Cr Low threshold -128 ~ +127 (2's complement)
0	4F	[7:0]	R_AWB_CbCrThdL[7:0]	AWB region test Cb+Cr Low threshold -128 ~ +127 (2's complement)
0	50	[7:0]	R_AWB_CbThdH[7:0]	AWB region test Cb High threshold -128 ~ +127 (2's complement)
0	51	[7:0]	R_AWB_CrThdH[7:0]	AWB region test Cr High threshold -128 ~ +127 (2's complement)
0	52	[7:0]	R_AWB_CbCrThdH[7:0]	AWB region test Cb+Cr High threshold -128 ~ +127 (2's complement)
0	53	[7:0]	R_Ylow	Low bound of “light-pixel” Y in AWB
0	54	[7:0]	R_Yhigh	High bound of “light-pixel” Y in AWB

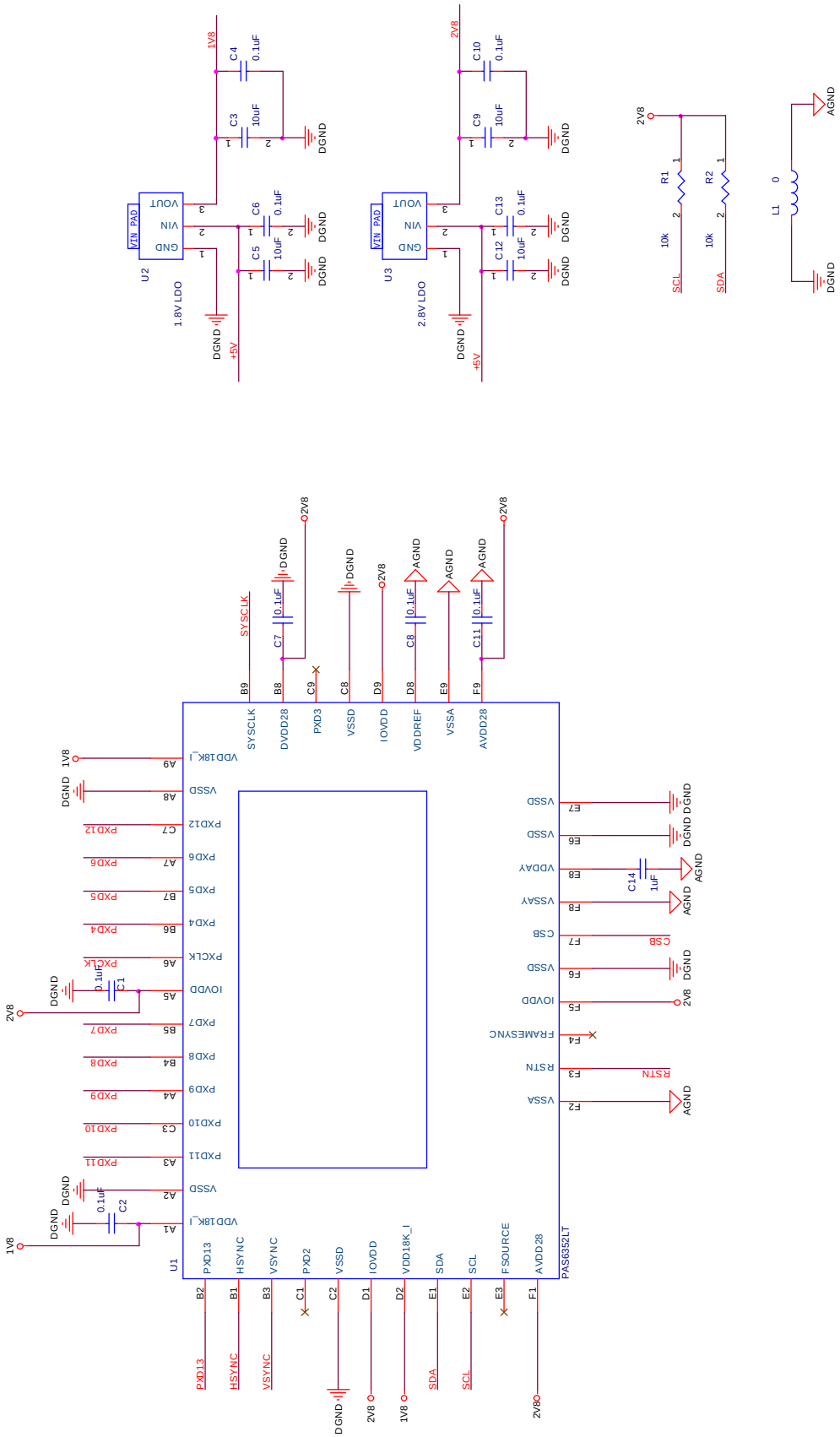
0	66	[4]	R_AE_EnH	AE enable
0	66	[0]	R_freq_60	Set de-flicker frequency 0/1: 50/60Hz
0	67	[7:0]	R_SysClk_freq[7:0]	Input_frequency/2048
0	68	[6:0]	R_SysClk_freq[14:8]	Input_frequency/2048
0	69	[7:0]	R_DeNoise_Str__G__HS[7:0]	Denoise Strength (for color G) in HS mode
0	6A	[7:0]	R_DeNoise_Str__RB_HS[7:0]	Denoise Strength (for color R/B) in HS mode
0	6B	[4:0]	R_AE_minStage[4:0]	Minimum AE stage
0	6C	[4:0]	R_AE_maxStage[4:0]	Maximum AE stage (AE_maxStage<=31)
0	6D	[7:0]	R_AG_stage_UB	AG_stage upper bound at max AE_stage (0:2x; 16:4x, 32:8x, 48:16x, 64:32x, 80:64x, 96:128x)
0	6F	[7:0]	R_Ytar8bit	0~255, Target luminance of AE
0	72	[0]	R_AWB_EnH	Auto-white balance enable
0	72	[4]	R_AWB_Gain_rst	AWB gain reset
0	79	[7:0]	R_ISP_HOffset[7:0]	ISP Hsize Offset
0	7B	[7:0]	R_ISP_VOffset[7:0]	ISP Vsize Offset
0	81	[5:4]	R_AE_Speed	AE speed, the more, the slower 0: 1 x 1: 1/2 x 2: 1/4 x 3: 1/8 x
0	8F	[7:0]	R_ImgEffect_c0	Image Effect parameter 0 (ISP_UpdateFlag=1, update)
0	90	[7:0]	R_ImgEffect_c1	Image Effect parameter 1 (ISP_UpdateFlag=1, update)
0	91	[7:0]	R_ImgEffect_c2	Image Effect parameter 2 (ISP_UpdateFlag=1, update)
0	93	[3:0]	R_ImgEffectMode	Image Effect mode 0: monochrome 1: negative 2: x-ray 3: Sepia/Cold/Warm/Sunset 6: Solarize 10: Pixelate (ISP_UpdateFlag=1, update)
0	94	[0]	R_ISP_ImgEffect_En	1: Image effect function enable (ISP_UpdateFlag=1, update)
0	97	[4]	R_Shading_EnH	Lens shading enable
0	99	[6:0]	R_OffsetX_R[6:0]	Horizontal distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63
0	9A	[6:0]	R_OffsetY_R[6:0]	Vertical distances between shading center and sensor array center of R-channel, MSB:sign bit, -63~+63

0	9B	[6:0]	R_OffsetX_G[6:0]	Horizontal distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	9C	[6:0]	R_OffsetY_G[6:0]	Vertical distances between shading center and sensor array center of G-channel, MSB:sign bit, -63~+63
0	9D	[6:0]	R_OffsetX_B[6:0]	Horizontal distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63
0	9E	[6:0]	R_OffsetY_B[6:0]	Vertical distances between shading center and sensor array center of B-channel, MSB:sign bit, -63~+63
0	9F	[5:0]	R_LSC_R1[5:0]	Quartic parameter of R-channel
0	A0	[5:0]	R_LSC_G1[5:0]	Quartic parameter of G-channel
0	A1	[5:0]	R_LSC_B1[5:0]	Quartic parameter of B-channel
0	A2	[5:0]	R_LSC_R2[5:0]	Square parameter of R-channel
0	A3	[5:0]	R_LSC_G2[5:0]	Square parameter of G-channel
0	A4	[5:0]	R_LSC_B2[5:0]	Square parameter of B-channel
0	A5	[2:0]	R_LSFT_1[2:0]	Lens shading coefficient coarse shift value
0	A6	[1:0]	R_LSFT_2[1:0]	Lens shading coefficient coarse shift value
0	A7	[1:0]	R_LSFT_3[1:0]	Lens shading coefficient coarse shift value
0	A8	[1:0]	R_LSFT_4[1:0]	Lens shading coefficient coarse shift value
2	8	[7:0]	R_ImgEffect_Y_offset[7:0]	Y offset value
2	9	[7:0]	R_ImgEffect_U_offset[7:0]	U offset value
2	A	[7:0]	R_ImgEffect_V_offset[7:0]	V offset value
2	B	[0]	R_ISP_ImgEffect_1_En	YUV value offset enable
2	2A	[7]	R_ISP_Edge_En0	ISP edge enhancement enable
2	2F	[4:0]	R_AE_stage_LL[4:0]	(AE_stage >= R_AE_stage_LL) && (AG_stage >= R_AG_stage_LL) =>Low Light
2	30	[4:0]	R_AE_stage_NL[4:0]	(AE_stage <= R_AE_stage_NL) && (AG_stage <= R_AG_stage_NL) =>Normal Light
2	32	[7:0]	R_AG_stage_LL[7:0]	(AE_stage >= R_AE_stage_LL) && (AG_stage >= R_AG_stage_LL) =>Low Light
2	33	[7:0]	R_AG_stage_NL[7:0]	(AE_stage <= R_AE_stage_NL) && (AG_stage <= R_AG_stage_NL) =>Normal Light
2	56	[4:0]	R_EdgeRatio_Delta[4:0]	Increment when AE/AG state change
2	57	[4:0]	R_EdgeRatio_LL[4:0]	Edge ratio @Low Light
2	58	[4:0]	R_EdgeRatio_NL[4:0]	Edge ratio @Normal Light
2	5A	[4:0]	R_Edge_th_Delta[4:0]	Increment when AE/AG state change
2	5B	[7:0]	R_Edge_th_LL[7:0]	Edge threshold @ Low Light
2	5C	[7:0]	R_Edge_th_NL[7:0]	Edge threshold @ Normal Light
2	5D	[1]	R_Saturation_2X	Color Saturation double
2	5E	[4:0]	R_Saturation_Delta[4:0]	Increment when AE/AG state change
2	5F	[4:0]	R_Saturation_LL[4:0]	Color Saturation @ Low Light
2	60	[4:0]	R_Saturation_NL[4:0]	Color Saturation @ Normal Light

2	62	[4:0]	R_Shading_CP_R_Delta[4:0]	Increment when AE/AG state change
2	63	[3:0]	R_Shading_CP_R_NL[3:0]	Shading compensation percentage @Normal Light
2	63	[7:4]	R_Shading_CP_R_LL[3:0]	Shading compensation percentage @Low Light
2	64	[0]	R_Contrast_En	Contrast Enable
2	69	[7:0]	R_Brightness_LL[7:0]	Brightness @ Low Light
2	6A	[7:0]	R_Brightness_NL[7:0]	Brightness @ Normal Light
2	9B	[1:0]	R_ISP_WOI_HSize[9:8]	Output image Hsize (ISP2_UpdateFlag=1, update)
2	9C	[7:0]	R_ISP_WOI_HSize[7:0]	Output image Hsize (ISP2_UpdateFlag=1, update)
2	9D	[1:0]	R_ISP_WOI_VSize[9:8]	Output image Vsize (ISP2_UpdateFlag=1, update)
2	9E	[7:0]	R_ISP_WOI_VSize[7:0]	Output image Vsize (ISP2_UpdateFlag=1, update)
2	9F	[1:0]	R_ISP_WOI_HOffset[9:8]	Output image H offset (ISP2_UpdateFlag=1, update)
2	A0	[7:0]	R_ISP_WOI_HOffset[7:0]	Output image H offset (ISP2_UpdateFlag=1, update)
2	A1	[1:0]	R_ISP_WOI_VOffset[9:8]	Output image V offset (ISP2_UpdateFlag=1, update)
2	A2	[7:0]	R_ISP_WOI_VOffset[7:0]	Output image V offset (ISP2_UpdateFlag=1, update)
2	B0	[7]	R_Scaler_X_En	Scaling Down X Enable (ISP2_UpdateFlag=1, update)
2	B0	[5:0]	R_ScaleDenr_X[5:0]	Scaling Down 16/x , 15<x<63 (ISP2_UpdateFlag=1, update)
2	B1	[7]	R_Scaler_Y_En	Scaling Down Y Enable (ISP2_UpdateFlag=1, update)
2	B1	[5:0]	R_ScaleDenr_Y[5:0]	Scaling Down 16/x , 15<x<63 (ISP2_UpdateFlag=1, update)
2	B2	[3:0]	R_EncDecimationNo_X[3:0]	ISP decimation no in X-direction (ISP_Zoom_UpdateFlag=1, update)
2	B2	[7:4]	R_EncDecimationNo_Y[3:0]	ISP decimation no in Y-direction (ISP_Zoom_UpdateFlag=1, update)
2	BF	[1]	R_UV_Swap	U V Swap
2	BF	[2]	R_YC_Swap	Y C Swap
2	C0	[3:0]	R_RGB565_mode[3:0]	RGB565_mode
2	C0	[5:4]	R_Format_Sel	Output Data format select 0:YUV 1:RGB565 2:RGB555 3:RGB444 (ISP2_UpdateFlag=1, update)
2	C1	[0]	R_Vsync_INV	Vsync inverse
2	C1	[1]	R_Hsync_INV	Hsync inverse
2	C1	[2]	R_Pxclk_INV	Pxclk inverse
3	2	[0]	R_CCMASign[8]	ACCM Base matrix coefficient
3	3	[7:0]	R_CCMASign[7:0]	ACCM Base matrix coefficient

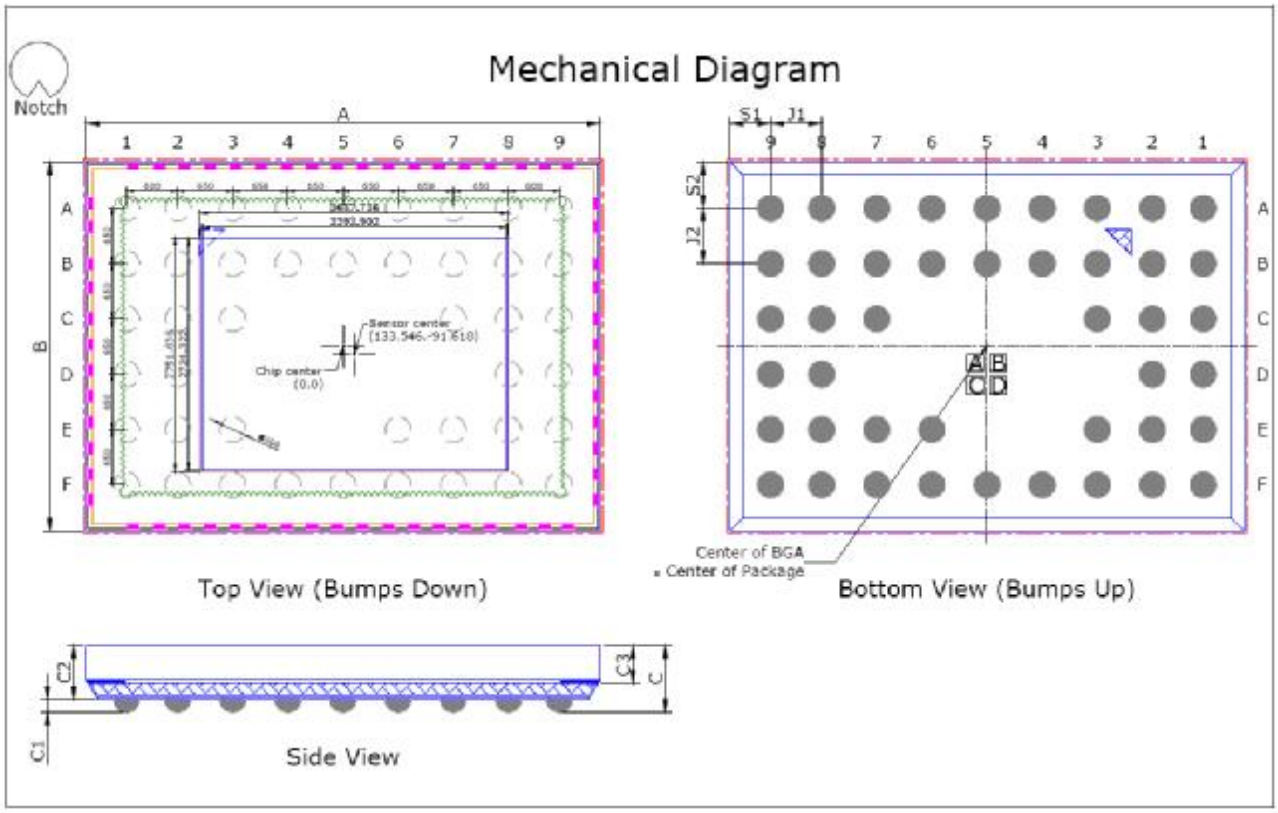
3	4	[7:0]	R_CCMA0_0[7:0]	ACCM Base matrix coefficient
3	5	[7:0]	R_CCMA0_1[7:0]	ACCM Base matrix coefficient
3	6	[7:0]	R_CCMA0_2[7:0]	ACCM Base matrix coefficient
3	7	[7:0]	R_CCMA1_0[7:0]	ACCM Base matrix coefficient
3	8	[7:0]	R_CCMA1_1[7:0]	ACCM Base matrix coefficient
3	9	[7:0]	R_CCMA1_2[7:0]	ACCM Base matrix coefficient
3	A	[7:0]	R_CCMA2_0[7:0]	ACCM Base matrix coefficient
3	B	[7:0]	R_CCMA2_1[7:0]	ACCM Base matrix coefficient
3	C	[7:0]	R_CCMA2_2[7:0]	ACCM Base matrix coefficient

4. Reference Circuit Schematic

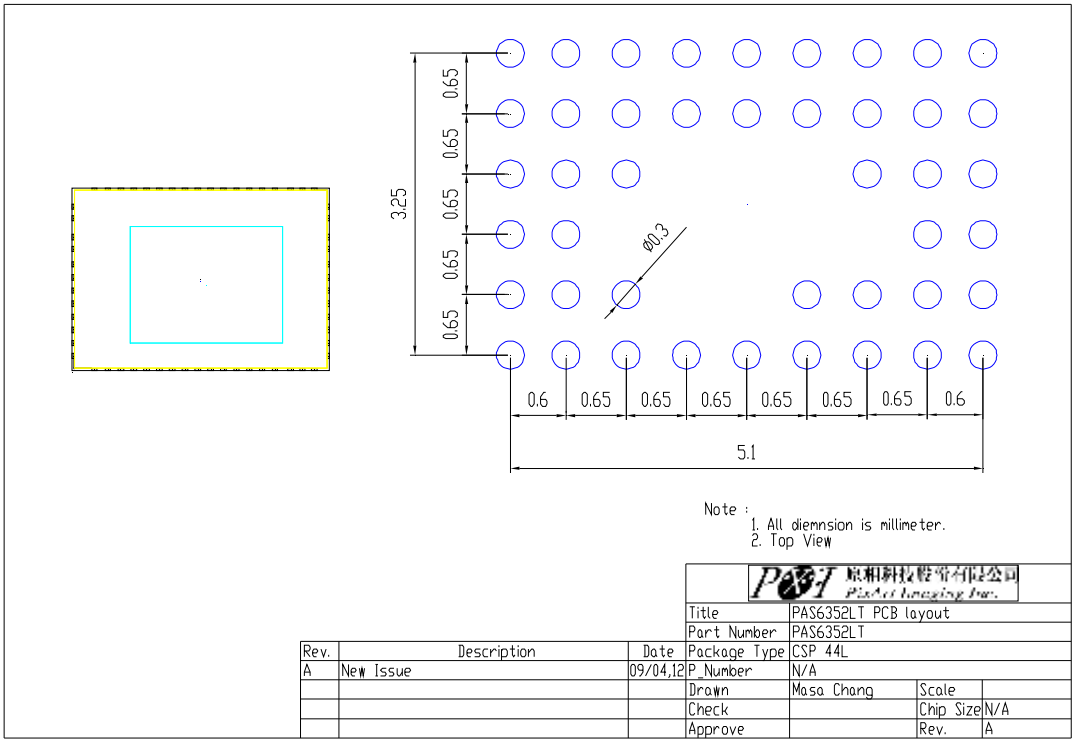


5. Package Information

	Symbol	Nominal	Min.	Max.
		µm		
Package Body Dimension X	A	6058.6	6033.6	6083.6
Package Body Dimension Y	B	4332	4307	4357
Package Height	C	790	730	850
Ball Height	C1	160	130	190
Package Body Thickness	C2	630	585	675
Thickness of Glass surface to wafer	C3	445	425	465
Ball Diameter	D	300	270	330
Total Pin Count	N	44		
Pin Count X axis	N1	9		
Pin Count Y axis	N2	6		
Pins Pitch X axis	J1	600/650		
Pins Pitch Y axis	J2	650		
Edge to Pin Center Distance along X	S1	479.3	449.3	509.3
Edge to Pin Center Distance along Y	S2	541	511	571



Recommended PCB Layout



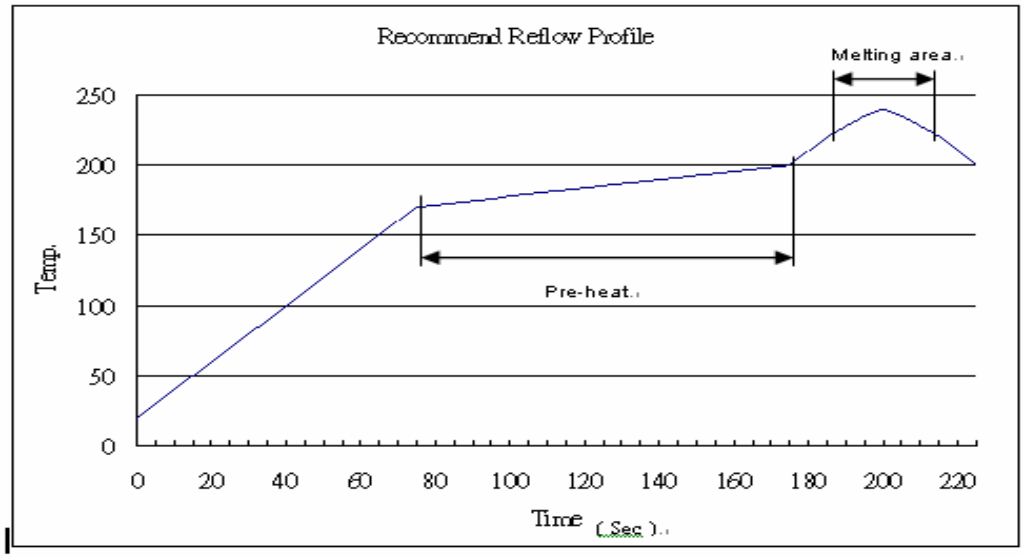
Recommended Guideline for PCB Assembly

Recommended vender and type for Pb-free solder paste

1. Almit LFM-48W TM-HP
2. Senju M705-GRN360-K

IR Reflow Soldering Profile:

Temperature profile is the most important control in reflow soldering. It must be fine tuned to establish a robust process. The typical recommended IR reflow profile is showed in figure below.



IR Reflow Profile

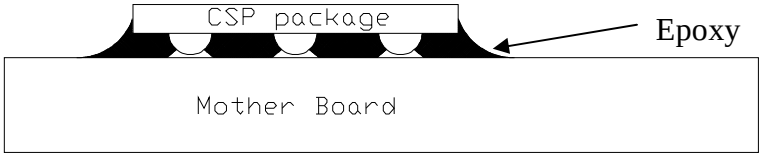
Reflow Profile :

1. Average Ramp-up Rate (30°C to preheat zone): 1.5~ 2.5 Degree C/ Sec
2. Preheat zone:
   - 2.1 Temp ramp from 170~ 200 degree C
   - 2.2 Exposure time: 90 +/- 30 sec
3. Melting zone:
   - 3.1 Melting area temp > 220 degree C for at least 30 ~ 50 sec
   - 3.2 Peak temperature : 245 degree C.

Others:

Epoxy under-filled process is required post IC mounting process.

⊙ Dispense Epoxy



Epoxy Under-filled