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RENESAS

MOS INTEGRATED CIRCUIT

μPD178046, 178048

8-BIT SINGLE-CHIP MICROCONTROLLER

DESCRIPTION

The μPD178046 and 178048 are 8-bit single-chip CMOS microcontrollers with hardware for digital tuning systems.

Employing the 78K/0 architecture as the CPU, these microcontrollers provide easy control access to the internal memories and peripheral hardware. The instructions are high-speed 78K/0 instructions suitable for system control.

As the peripheral hardware, an OSD (on-screen display) controller and PWM (pulse width modulation) output for TV use, as well as many I/O ports, timers, A/D converter, serial interface, and power-ON clear circuit are provided.

A flash memory model, μPD178F048, that can operate on the same supply voltage as the mask ROM models, and many development tools are under development.

The functions of these microcontrollers are described in detail in the following User's Manuals. Be sure to read these manuals when you design your system.

μPD178048 Subseries User's Manual : Planned to be published
78K/0 Series User's Manual - Instruction : U12326E

FEATURES

- ROM and RAM capacities

Item / Part Number	Program Memory (ROM)	Character ROM (CROM)	Data Memory		Video RAM (VRAM)
			Internal high-speed RAM	Internal expansion RAM	
μPD178046	48K bytes	6912 bytes (256 characters)	512 bytes	512 bytes	482 bytes (12 × 24 characters MAX.)
μPD178048	60K bytes				

- Instruction cycle: 0.4 μs (with 5.0-MHz crystal resonator)
- Many peripheral hardware circuits
  General-purpose I/O ports, A/D converter, serial interface, timers, power-ON clear circuit
- OSD controller and PWM output
- Vectored interrupts: 17
- Supply voltage: V_{DD} = 4.5 to 5.5 V

Document No. U13183EJ1V0PM00 (1st edition)
Date Published June 1998 N CP(K)
Printed in Japan

APPLICATION FIELD

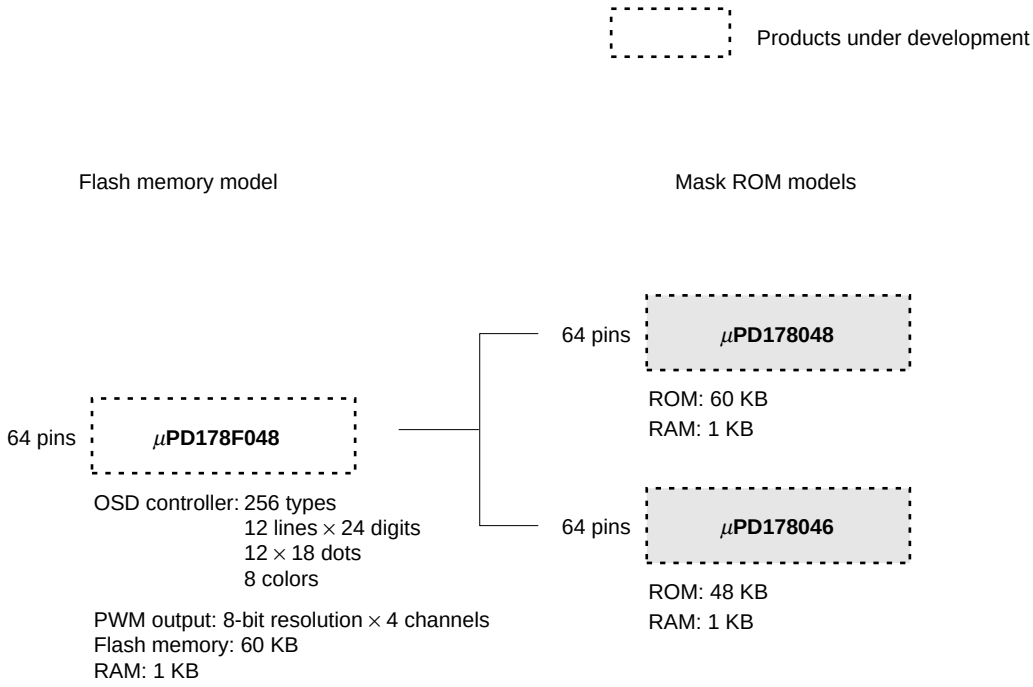
TV

ORDERING INFORMATION

Part Number	Package
μPD178046CW-×××	64-pin plastic shrink DIP (750 mil)
μPD178048CW-×××	64-pin plastic shrink DIP (750 mil)

Remark ××× indicates ROM code suffix. The ROM code suffix is E×× when an I^2C bus is used.

DEVELOPMENT OF μPD178048 SUBSERIES



FUNCTION OUTLINE

(1/2)

Item \ Part Number		μPD178046	μPD178048
Internal memory	ROM	48K bytes	60K bytes
	Character ROM (CROM)	6912 bytes (256 characters)	
	High-speed RAM	512 bytes	
	Expansion RAM	512 bytes	
	Video RAM (VRAM)	432 bytes (12 × 24 characters MAX.)	
General-purpose register		8 bits × 32 registers (8 bits × 8 bits × 4 banks)	
Minimum instruction execution time		0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (with 5.0-MHz crystal resonator)	
Instruction set		• 16-bit operation • Multiplication/division (8 bits × 8 bits, 16 bits ÷ 8 bits) • Bit manipulation (set, reset, test, Boolean operation) • BCD adjustment, etc.	
I/O ports		Total : 46 pins • CMOS input : 4 pins • CMOS I/O : 37 pins • N-ch open-drain output : 5 pins	
A/D converter		8-bit resolution × 4 channels	
Serial interface		• I^2C bus mode[Note] : 2 channels (shift register: 1 channel) • 3-wire serial I/O mode : 1 channel	
Timer		• Basic timer (timer carry (10 Hz)) : 1 channel • 8-bit timer/event counter : 1 channel • 8-bit timer : 1 channel • 8-bit event counter : 1 channel • 8-bit remote control timer : 1 channel • Watchdog timer : 1 channel	

Note If the I^2C bus mode is used (including when it is implemented in software without using the peripheral hardware), inform NEC when you order a mask.

(2/2)

Item \ Part Number		μPD178046	μPD178048
PWM output		• 8-bit resolution × 4 channel • 14-bit resolution × 1 channel	
OSD controller	Number of display characters	288 characters MAX. per screen (12 lines × 24 digits)	
	Character type	256 types (stored in CROM)	
	Character format	12 (width) × 18 (height) dots	
	Character size	1 × 1, 2 × 2, 3 × 3, or 4 × 4 selectable	
	Character color	8 colors	
	Character frame	Framed or non-framed characters selected in screen units	
	Background	No background, blank, or filled selectable. Background color (8 colors) can be specified.	
	Half blanking	Can be specified in character units.	
ROM correction		2 places	
Vectored interrupt source	Maskable	Internal: 11, external: 5	
	Non-maskable	Internal: 1	
	Software	1	
Standby function		• HALT mode • STOP mode	

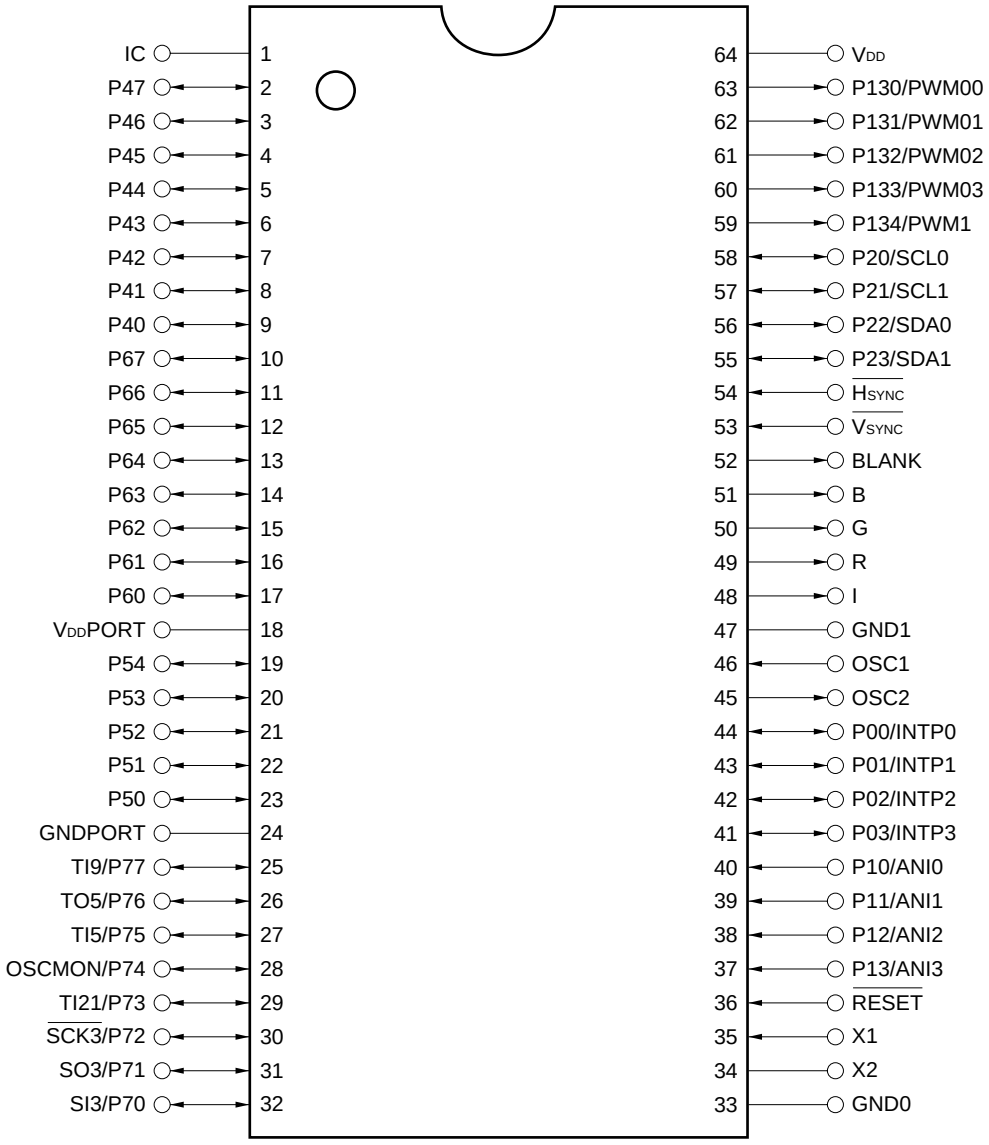
Reset		• Reset by $\overline{\text{RESET}}$ pin
		• Internal reset by watchdog timer
		• Reset by power-ON clear circuit
		  • Detection of less than 4.5 V[Note] (during CPU operation and on power application)
		  • Detection of less than 2.5 V[Note] (in STOP mode)	

Supply voltage		V_{DD} = 4.5 to 5.5 V	
Package		64-pin plastic shrink DIP (750 mil)	

Note These values are the maximum values. Actually, reset is effected at lower voltages.

PIN CONFIGURATION (Top View)

- **64-pin plastic shrink DIP (750 mil)**
  μPD178046CW-×××
  μPD178048CW-×××



Cautions 1. Directly connect IC (Internally Connected) pins to GND0 or GND1.

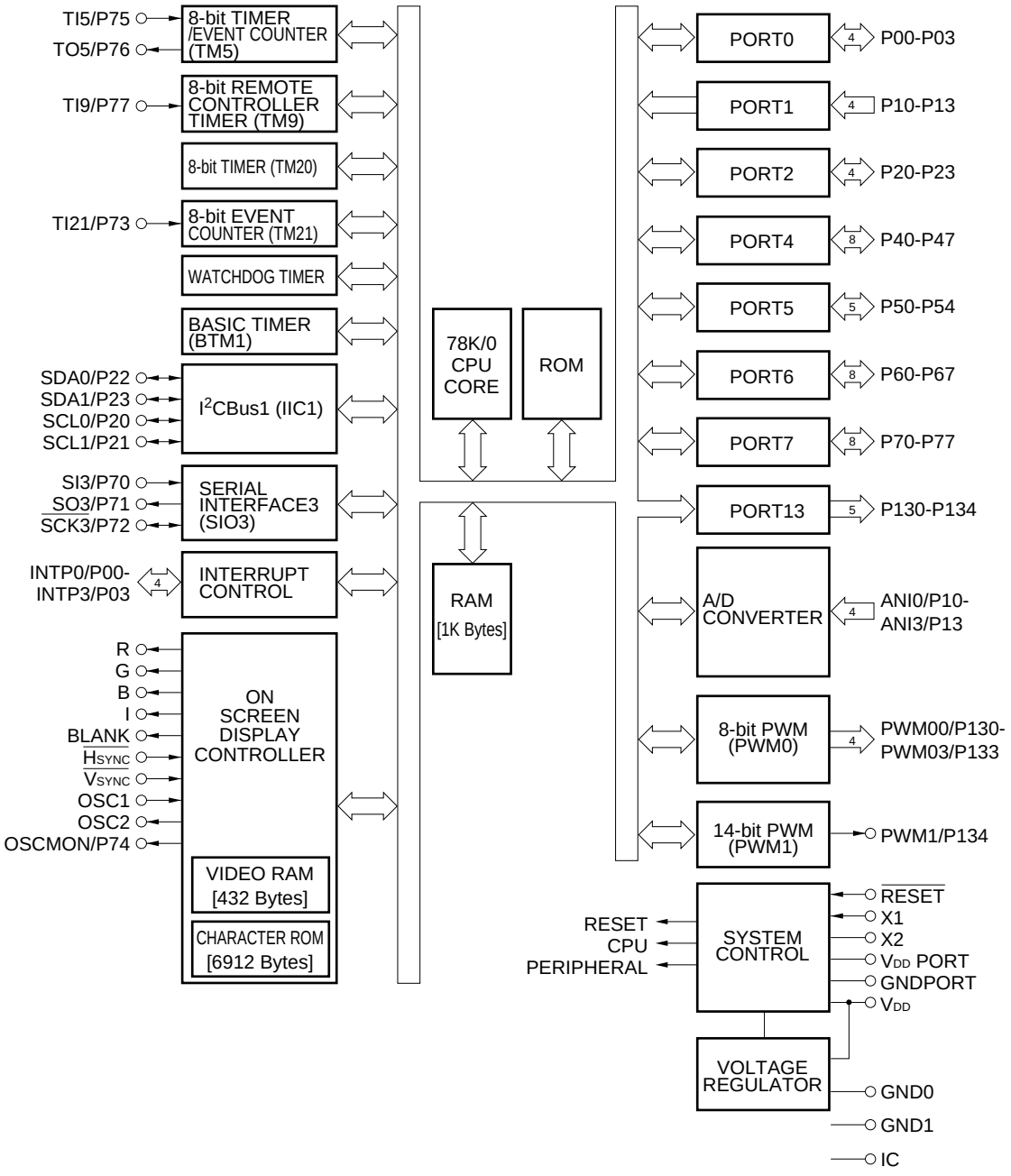
2. Keep the voltage at the V_{DD}PORT pin the same as the V_{DD} pin.

3. Keep the voltage at the GNDPORT pin the same as GND0 or GND1.

PIN NAMES

ANI0-ANI3	:	A/D converter input
B	:	Character signal output
BLANK	:	Blanking signal output
G	:	Character signal output
GND0, GND1	:	Ground
GNDPORT	:	Port ground
$\overline{\text{HSYNC}}$	:	Horizontal sync signal input
I	:	Character signal output
IC	:	Internally connected
INTP0-INTP3	:	Interrupt input
OSC1, OSC2	:	LC connection for OSD dot clock oscillation
OSCMON	:	OSD clock output
P00-P03	:	Port 0
P10-P13	:	Port 1
P20-P23	:	Port 2
P40-P47	:	Port 4
P50-P54	:	Port 5
P60-P67	:	Port 6
P70-P77	:	Port 7
P130-P134	:	Port 13
PWM00-PWM03	:	8-bit PWM output
PWM1	:	14-bit PWM output
R	:	Character signal output
$\overline{\text{RESET}}$	:	Reset input
$\overline{\text{SCK3}}$	:	Serial clock input/output
SCL0, SCL1	:	Serial clock input/output
SDA0, SDA1	:	Serial data input/output
SI3	:	Serial data input
SO3	:	Serial data output
TI5, TI9, TI21	:	8-bit timer clock input
TO5	:	8-bit timer output
V_{DD}	:	Power supply
V_{DD}PORT	:	Port power supply
$\overline{\text{VSYNC}}$	:	Vertical sync signal input
X1, X2	:	Crystal resonator connection for system clock oscillation

BLOCK DIAGRAM



Remark The internal ROM capacity differs depending on the model.

TABLE OF CONTENTS

1. PIN FUNCTIONS

1.1 Port Pins

Pin Name	I/O	Function	At Reset	Shared with:
P00-P03	I/O	Port 0. 4-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	INTP0-INTP3
P10-P13	Input	Port 1. 4-bit input port.	Input	ANI0-ANI3
P20, P21	I/O	Port 2. 4-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	SCL0, SCL1
P22, P23				SDA0, SDA1
P40-P47	I/O	Port 4. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	—
P50-P54	I/O	Port 5. 5-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	—
P60-P67	I/O	Port 6. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	—
P70	I/O	Port 7. 8-bit I/O port. Can be set in input or output mode in 1-bit units.	Input	SI3
P71				SO3
P72				$\overline{\text{SCK3}}$
P73				TI21
P74				OSCMON
P75				TI5
P76				TO5
P77				TI9
P130-P133	Output	Port 13. 5-bit output port. N-ch open-drain output port (5 V withstand voltage).	—	PWM00-PWM03
P134				PWM1

1.2 Pins Other Than Port Pins

Pin Name	I/O	Function		At Reset	Shared with:
INTP0-INTP3	Input	External maskable interrupt input whose valid edge can be specified (rising edge, falling edge, or both rising and falling edges)		Input	P00-P03
SI3	Input	Serial data input to serial interface		Input	P70
SO3	Output	Serial data output from serial interface		Input	P71
SDA0, SDA1	I/O	Serial data input/output to/from serial interface	N-ch open-drain I/O	Input	P22, P23
$\overline{SCK3}$	I/O	Serial clock input/output to/from serial interface		Input	P72
SCL0, SCL1	I/O		N-ch open-drain I/O	Input	P20, P21
TI5	Input	External count clock input to 8-bit timer/event counter (TM5)		Input	P75
TI9		External count clock input to 8-bit remote control timer (TM9)			P77
TI21		External count clock input to 8-bit event counter (TM21)			P73
TO5	Output	8-bit timer/event counter (TM5) output		Input	P76
ANI0-ANI3	Input	Analog input to A/D converter		Input	P10-P13
PWM00-PWM03	Output	8-bit PWM output	N-ch open-drain I/O	—	P130-P133
PWM1		14-bit PWM output			P134
OSCMON	Output	OSD clock output		Input	P74
$\overline{V_{SYNC}}$	Input	OSD vertical sync signal input		Input	—
$\overline{H_{SYNC}}$		OSD horizontal sync signal input			—
R	Output	RED output for OSD characters and background		Low-level output	—
G		GREEN output for OSD characters and background			—
B		BLUE output for OSD characters and background			—
I		Character background output for OSD characters and blank background mode			—
BLANK		OSD blanking signal output			—
$\overline{RESET}$	Input	System reset input		—	—
X1	Input	Crystal resonator connection for system clock oscillation		—	—
X2	—			—	—
OSC1	Input	LC connection for OSD dot clock oscillation		—	—
OSC2	Output			—	—
V_{DD}	—	Positive power supply		—	—
GND0, GND1	—	Ground		—	—
V_{DD}PORT	—	Port power supply		—	—
GNDPORT	—	Port ground		—	—
IC	—	Internally connected. Directly connect this pin to GND0 or GND1.		—	—

1.3 I/O Circuits of Respective Pins and Recommended Connection of Unused Pins

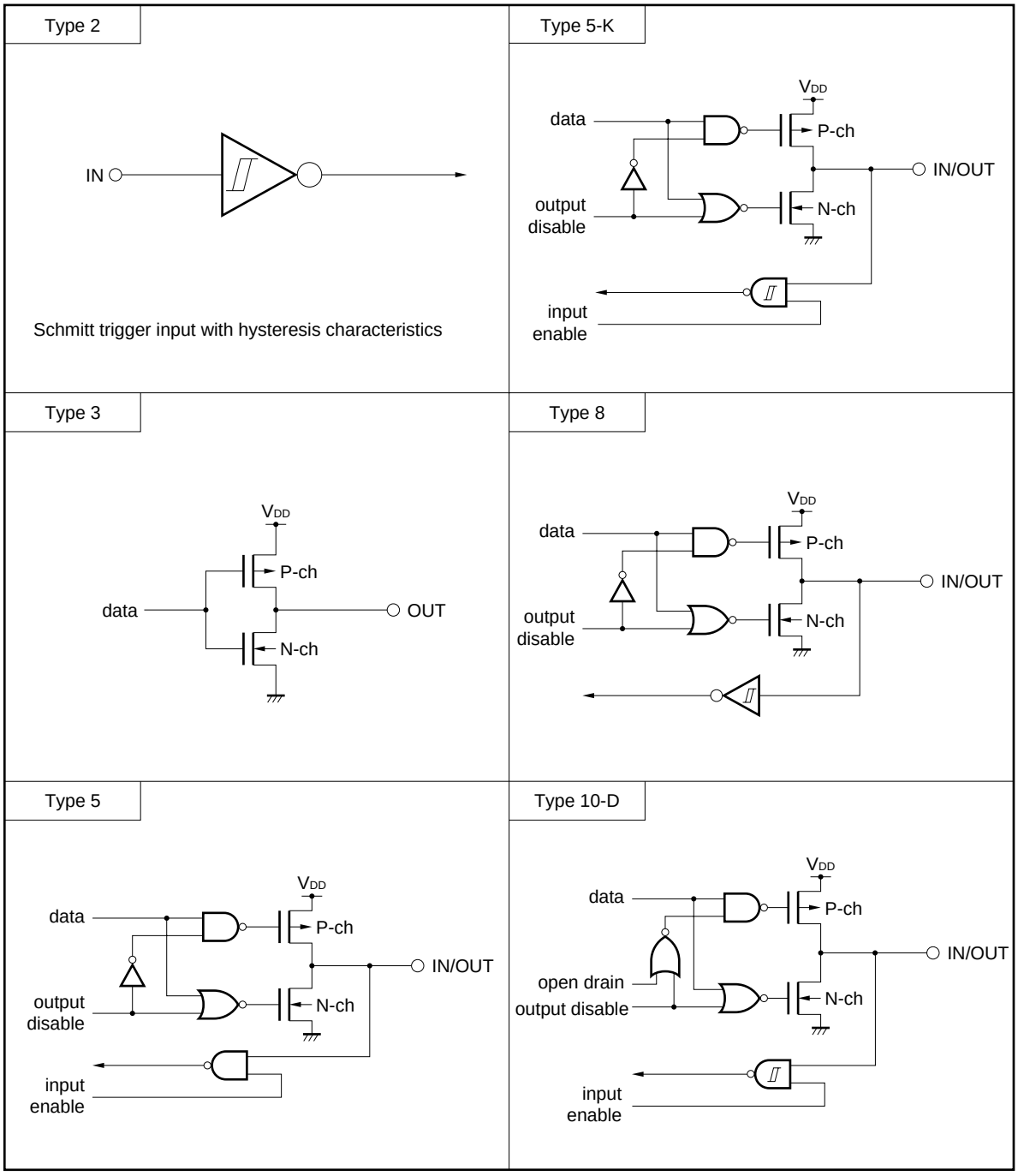
Table 1-1 shows the I/O circuit type of each pin and the recommended connection of unused pins.

For the configuration of each I/O circuit, refer to **Figure 1-1**.

Table 1-1. I/O Circuits of Respective Pins and Recommended Connection of Unused Pins

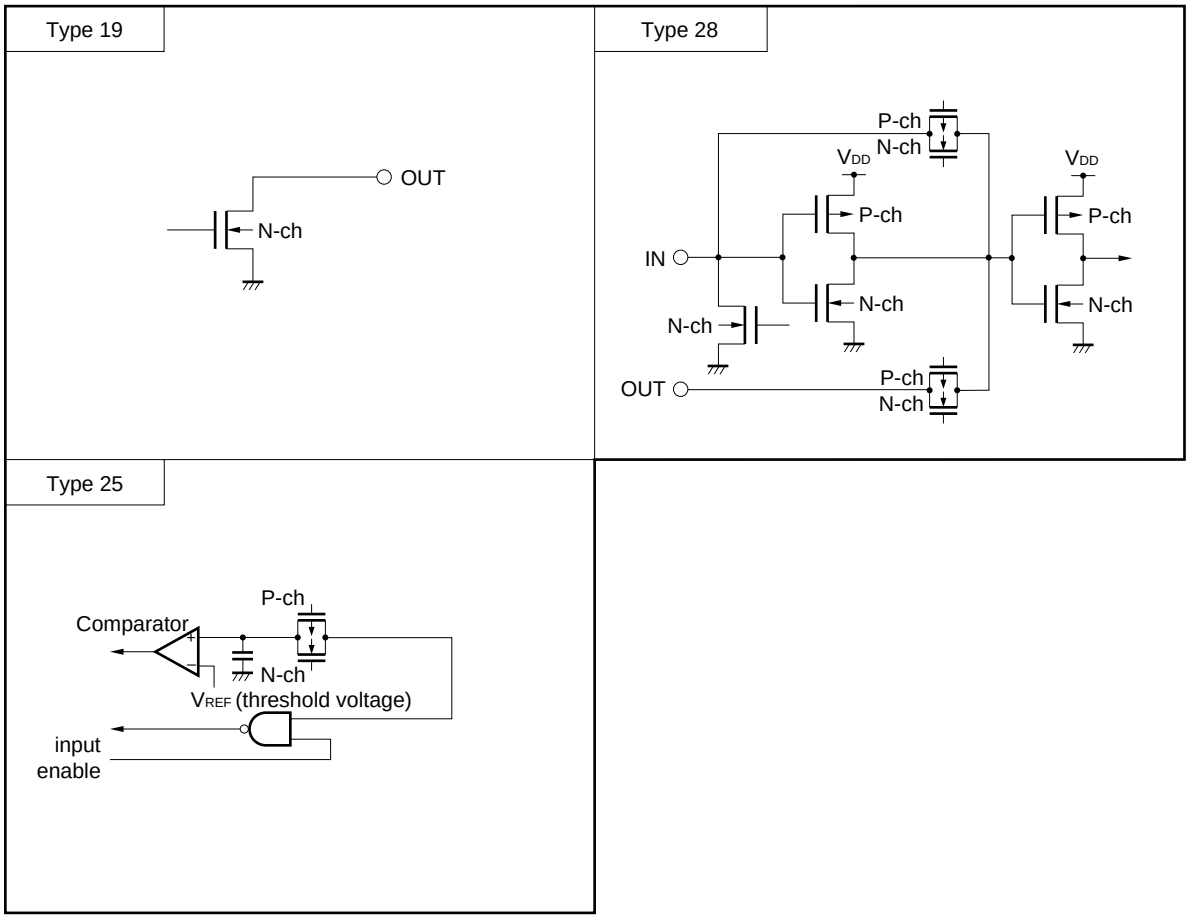
Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0-P03/INTP3	8	I/O	Set in general-purpose input port mode by software, and individually connect to GND0, GND1, or GNDPORT via resistor.
P10/ANI0-P13/ANI3	25	Input	Individually connect to V_{DD}, V_{DD}PORT, GND0, GND1, and GNDPORT via resistor.
P20/SCL0, P21/SCL1	10-D	I/O	Set in general-purpose input port mode by software, and individually connect to V_{DD}, V_{DD}PORT, GND0, GND1, or GNDPORT via resistor.
P22/SDA0, P23/SDA1			
P40-P47	5		
P50-P54			
P60-P67			
P70/SI3	5-K		
P71/SO3	5		
P72/SCK3	5-K		
P73/TI21			
P74/OSCMON	5		
P75/TI5	5-K		
P76/TO5	5		
P77/TI9	5-K		
P130/PWM00 -P133/PWM03	19	Output	Set to low-level output by software and leave unconnected.
P134/PWM1			
$\overline{V_{SYNC}}$	2	Input	Individually connect to GND0 or GND1 via resistor.
$\overline{H_{SYNC}}$			
R	3	Output	Set OSD display to OFF by software and leave unconnected.
G			
B			
I			
BLANK			
$\overline{RESET}$	2	Input	—
OSC1	28	Input	Set LC oscillation to OFF by software and leave unconnected.
OSC2		Output	Leave unconnected.
IC	—	—	Directly connect to GND0 or GND1.

Figure 1-1. I/O Circuits of Respective Pins (1/2)



Remark V_{DD} and GND are positive power supply and ground pins for ports. Take them as V_{DD}PORT and GNDPORT.

Figure 1-1. I/O Circuits of Respective Pins (2/2)

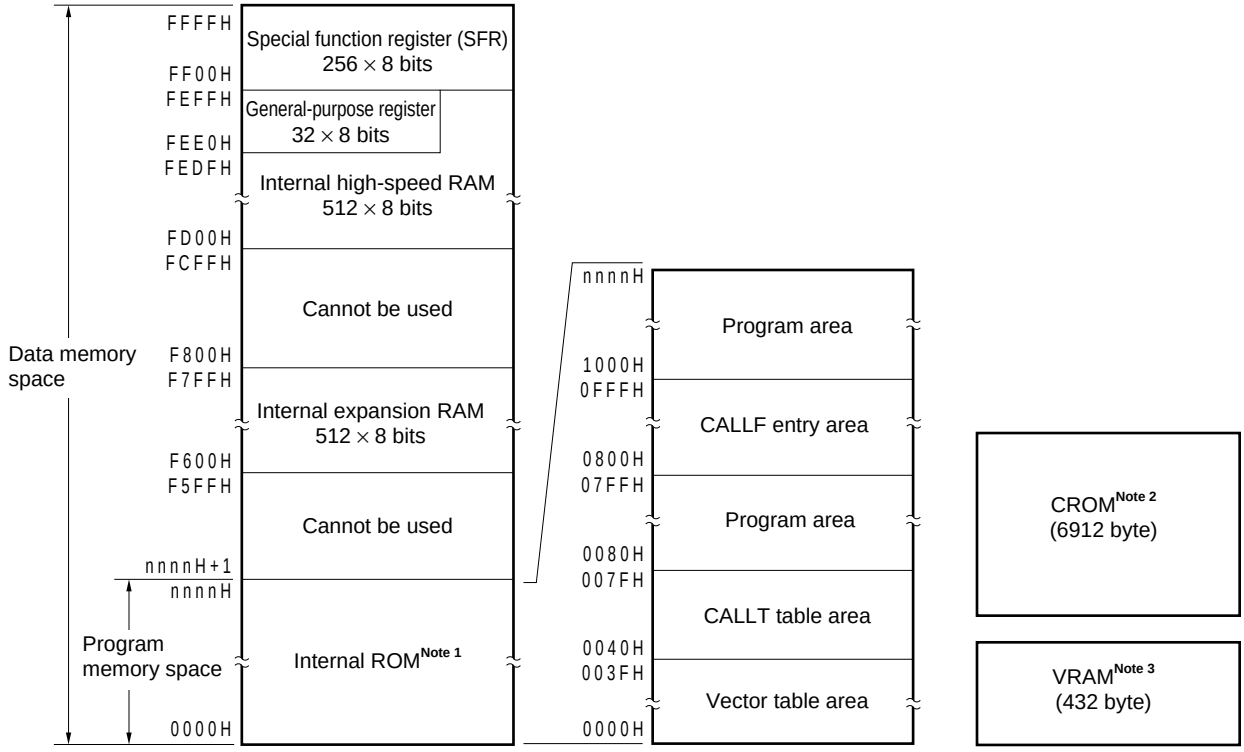


Remark V_{DD} and GND are positive power supply and ground pins for ports. Take them as V_{DD}PORT and GNDPORT.

2. MEMORY SPACE

Figure 2-1 shows the memory map of the μPD178046 and 178048.

Figure 2-1. Memory Map



Notes 1. The internal ROM capacity differs depending on the model (refer to the **table** below).

Part Number	Internal ROM End Address nnnnH
μPD178046	BFFFH
μPD178048	EFFFH

2. CROM cannot be read by software.

3. VRAM can be written via SFR.

2.1 Memory Size Select Register (IMS)

The internal memory capacities can be changed by using the memory size select register (IMS).

Set IMS to the value shown in Table 2-1 depending on the internal memory capacity of each model.

Use an 8-bit memory manipulation instruction to set this register.

IMS is set to CFH at reset.

Figure 2-2. Format of Memory Size Select Register (IMS)

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CFH	R/W

RAM2	RAM1	RAM0	Selects internal high-speed RAM capacity
0	1	0	512 bytes
Others			Setting prohibited

RAM3	RAM2	RAM1	RAM0	Selects internal ROM capacity
1	1	0	0	48K bytes
1	1	1	1	60K bytes
Others				Setting prohibited

Table 2-1. Set Value of Memory Size Select Register (IMS)

Part Number	Set Value of IMS
μPD178046	4CH
μPD178048	4FH

2.2 Internal Expansion RAM Size Select Register (IXS)

The internal expansion RAM capacity can be selected by using the internal expansion RAM size select register.

This register of the μPD178046 and 178048 must be set to 0BH.

Use an 8-bit memory manipulation instruction to set IXS.

The value of this register is set to 0CH at reset.

Figure 2-3. Format of Internal Expansion RAM Size Select Register (IXS)

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IXS	0	0	0	IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	FFF4H	0CH	R/W

IXRAM4	IXRAM3	IXRAM2	IXRAM1	IXRAM0	Selects internal expansion RAM capacity
0	1	0	1	1	512 bytes
Others					Setting prohibited

3. FEATURES OF PERIPHERAL HARDWARE FUNCTIONS

3.1 Ports

The following three types of I/O ports are available:

- CMOS input (port 1) : 4 pins
- CMOS I/O (ports 0 and 2 through 7) : 37 pins
- N-ch open-drain output (port 13) : 5 pins

Total : 46 pins

Table 3-1. Port Functions

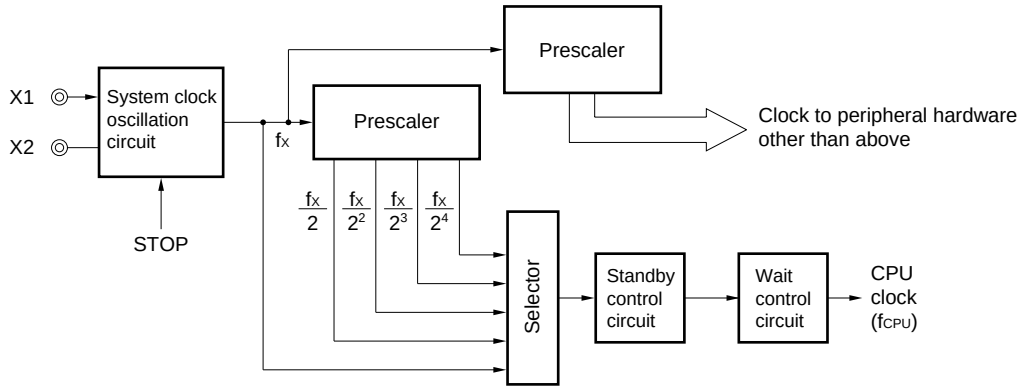
Name	Pin Name	Function
Port 0	P00-P03	I/O port. Can be set in input or output mode in 1-bit units.
Port 1	P10-P13	Input port
Port 2	P20-P23	I/O port. Can be set in input or output mode in 1-bit units.
Port 4	P40-P47	I/O port. Can be set in input or output mode in 1-bit units.
Port 5	P50-P54	I/O port. Can be set in input or output mode in 1-bit units.
Port 6	P60-P67	I/O port. Can be set in input or output mode in 1-bit units.
Port 7	P70-P77	I/O port. Can be set in input or output mode in 1-bit units.
Port 13	P130-P134	N-ch open-drain output port

3.2 Clock Generation Circuit

The instruction execution time can be changed as follows:

- 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (system clock: 5.0-MHz crystal resonator)

Figure 3-1. Block Diagram of Clock Generation Circuit



3.3 Timers

Six timer channels are provided.

- Basic timer : 1 channel
- 8-bit timer/event counter : 1 channel
- 8-bit timer : 1 channel
- 8-bit event counter : 1 channel
- 8-bit remote control timer : 1 channel
- Watchdog timer : 1 channel

Figure 3-2. Block Diagram of Basic Timer (BTM1)

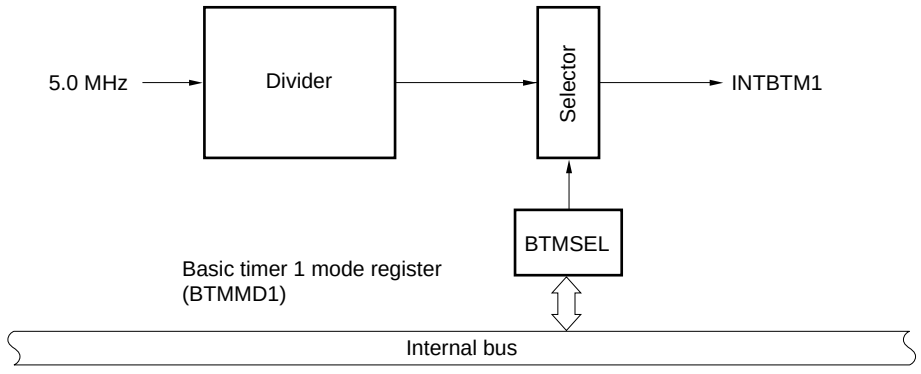


Figure 3-3. Block Diagram of 8-Bit Timer/Event Counter (TM5)

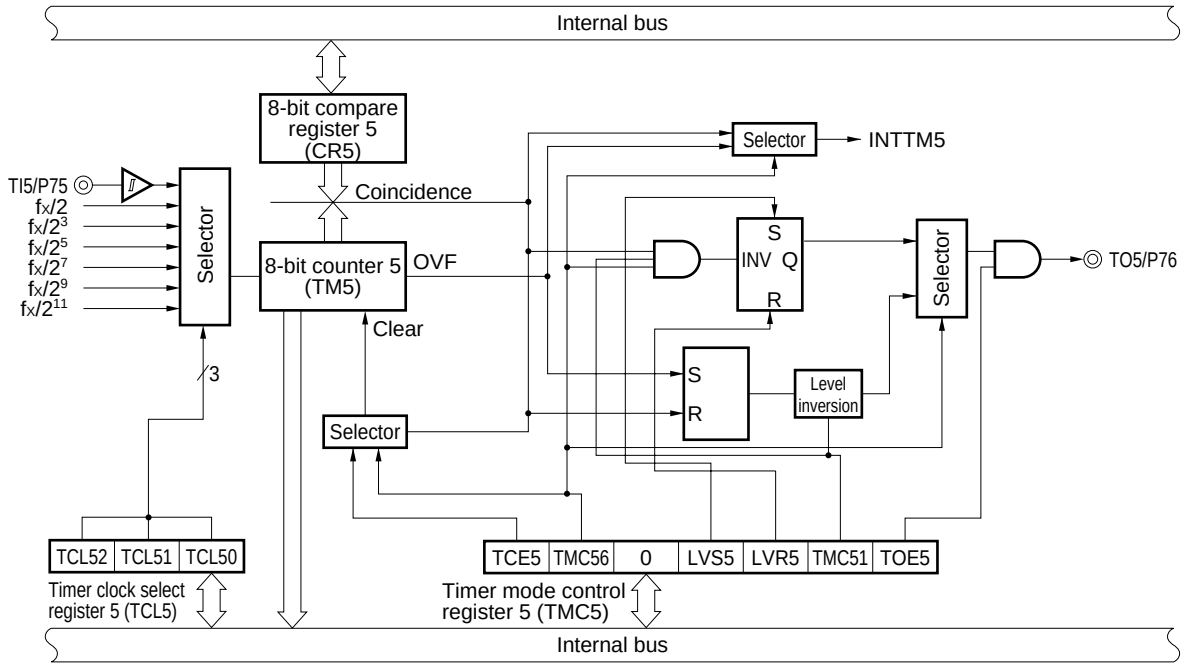


Figure 3-4. Block Diagram of 8-Bit Timer (TM20)

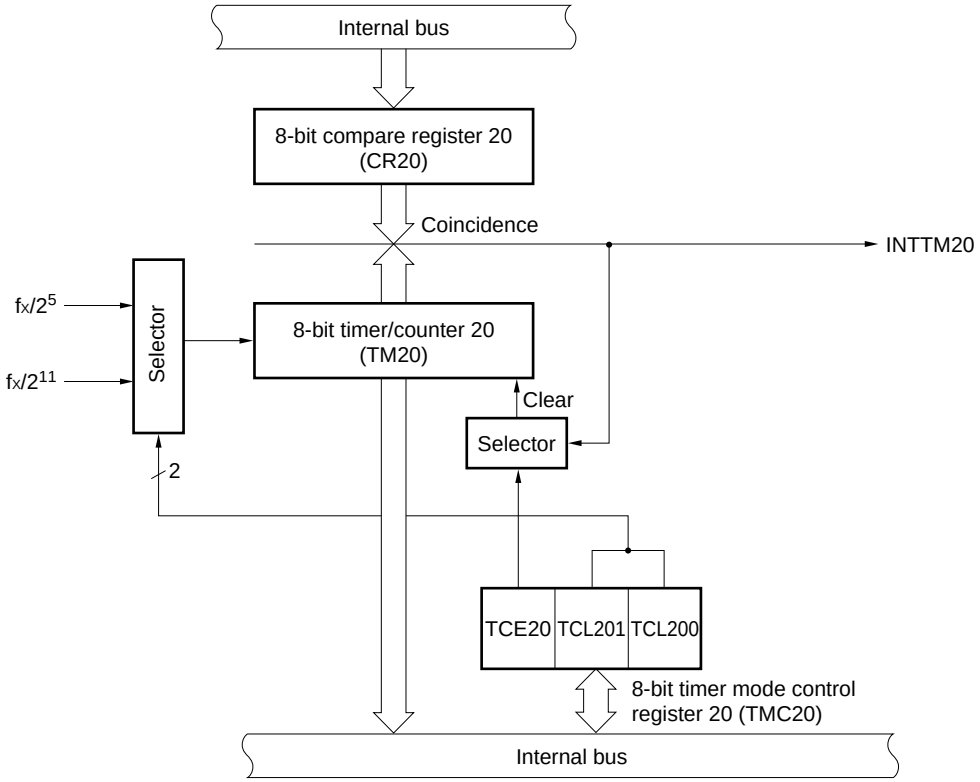
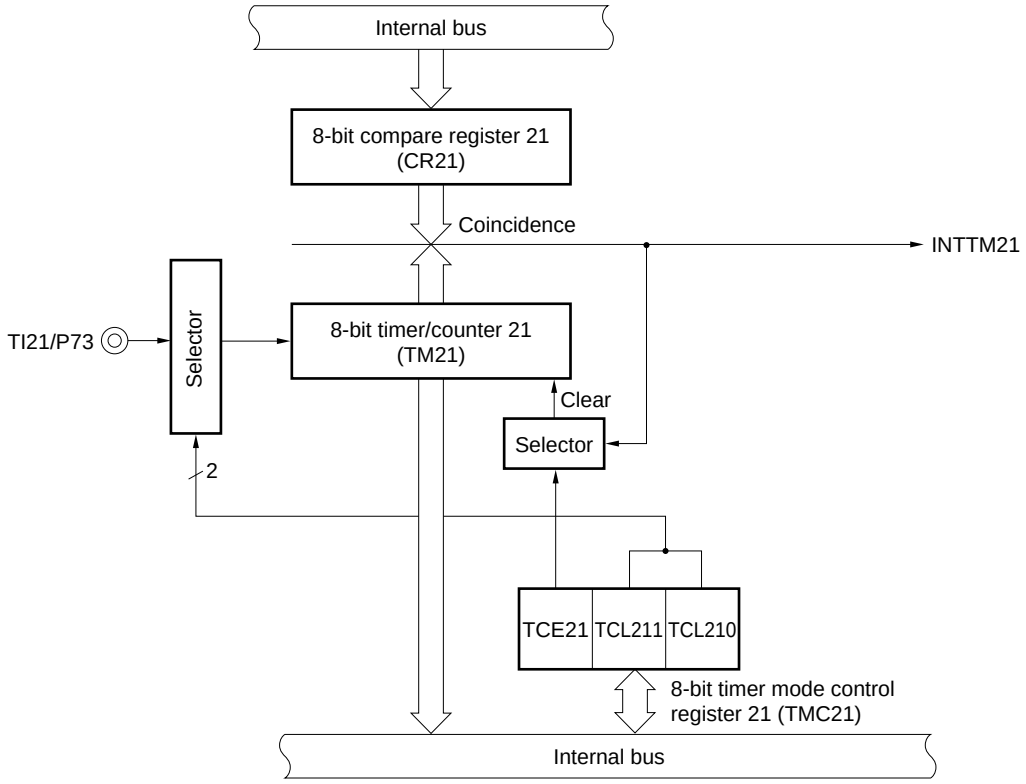


Figure 3-5. Block Diagram of 8-Bit Event Counter (TM21)



Remark The 8-bit event counter (TM21) can be also used as an HSYNC counter.

Figure 3-6. Block Diagram of 8-Bit Remote Control Timer (TM9)

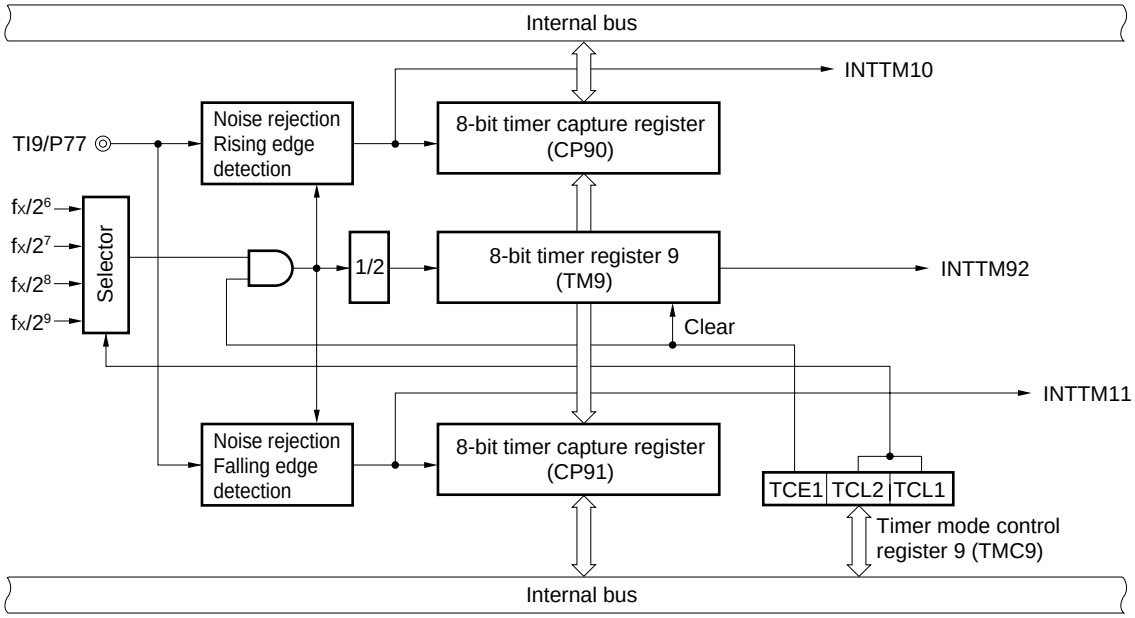
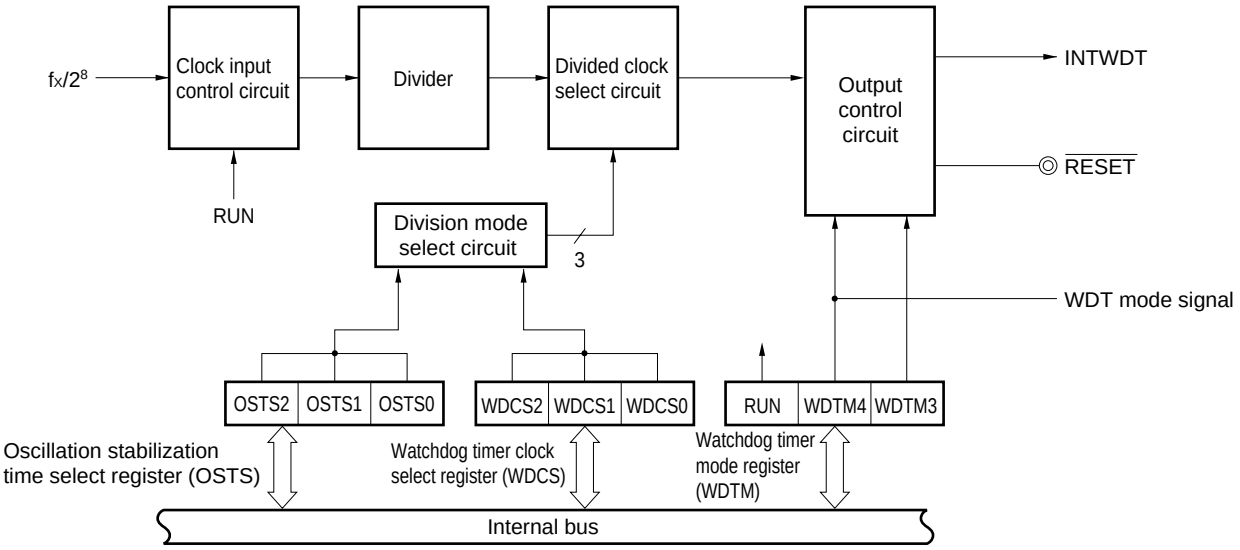


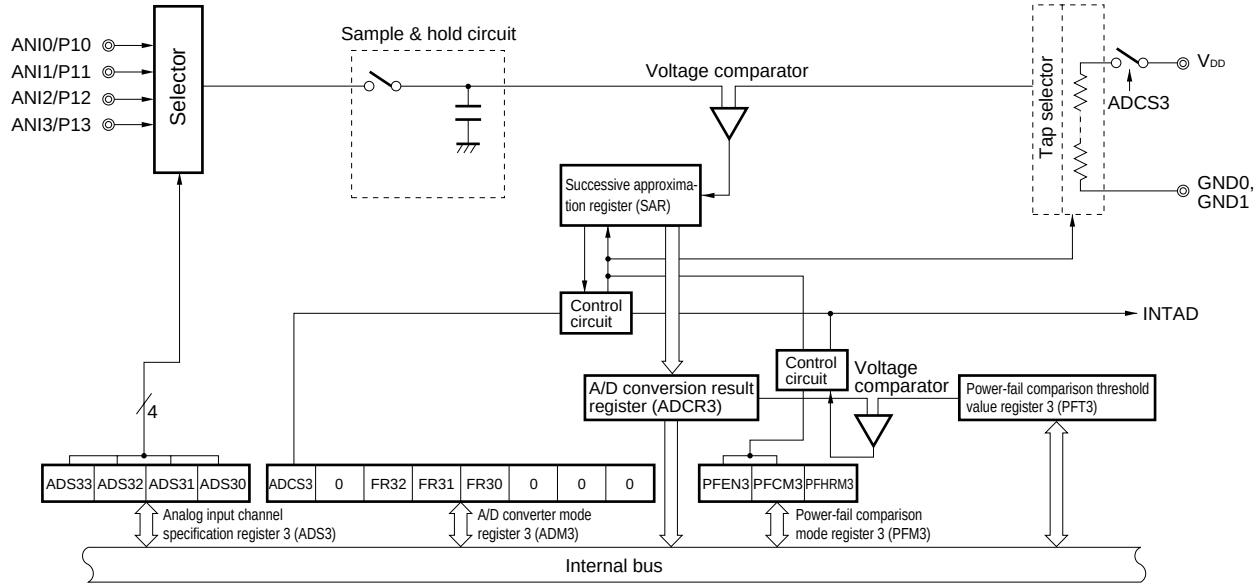
Figure 3-7. Block Diagram of Watchdog Timer



3.4 A/D Converter

An A/D converter with a resolution of 8 bits and 4 channels is provided.

Figure 3-8. Block Diagram of A/D Converter



3.5 Serial Interface

Two serial interface channels are provided.

- Serial interface (IIC1)
- Serial interface (SIO3)

Table 3-2. Types and Functions of Serial Interfaces

Function	IIC1	SIO3
I^2C bus mode	○ (MSB first)	—
3-wire serial I/O mode	—	○ (MSB first)

Figure 3-9. Block Diagram of Serial Interface (IIC1)

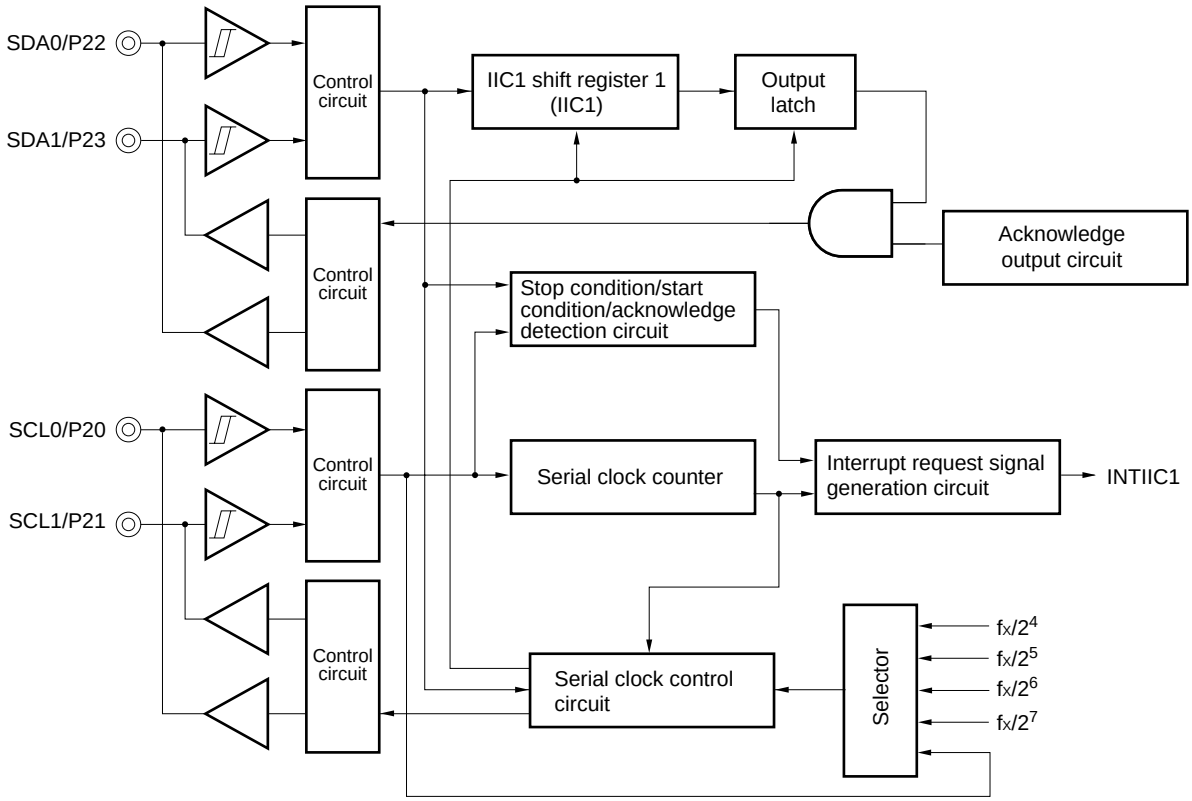
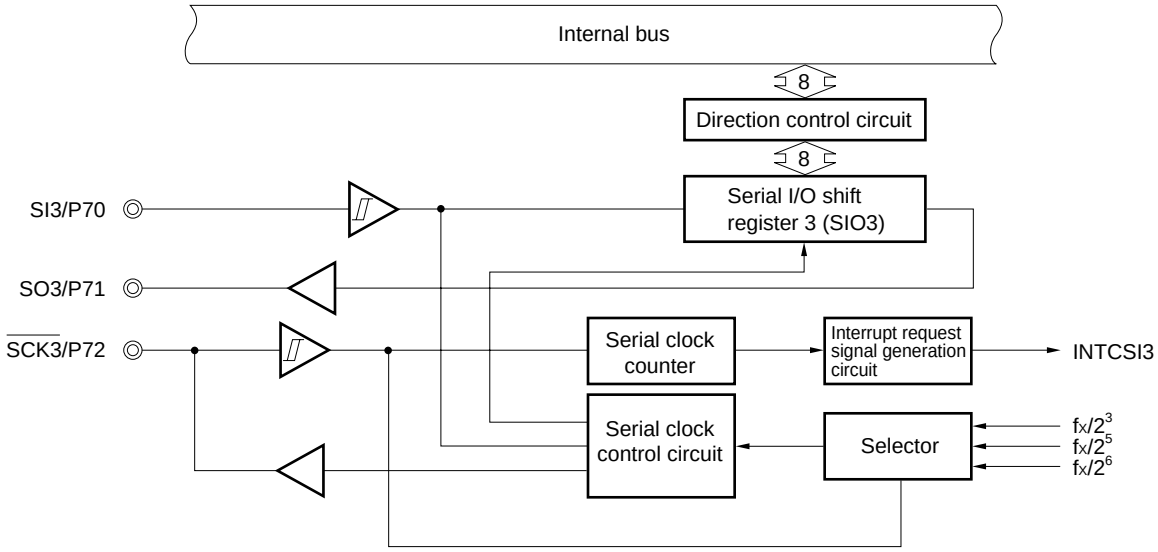


Figure 3-10. Block Diagram of Serial Interface (SIO3)

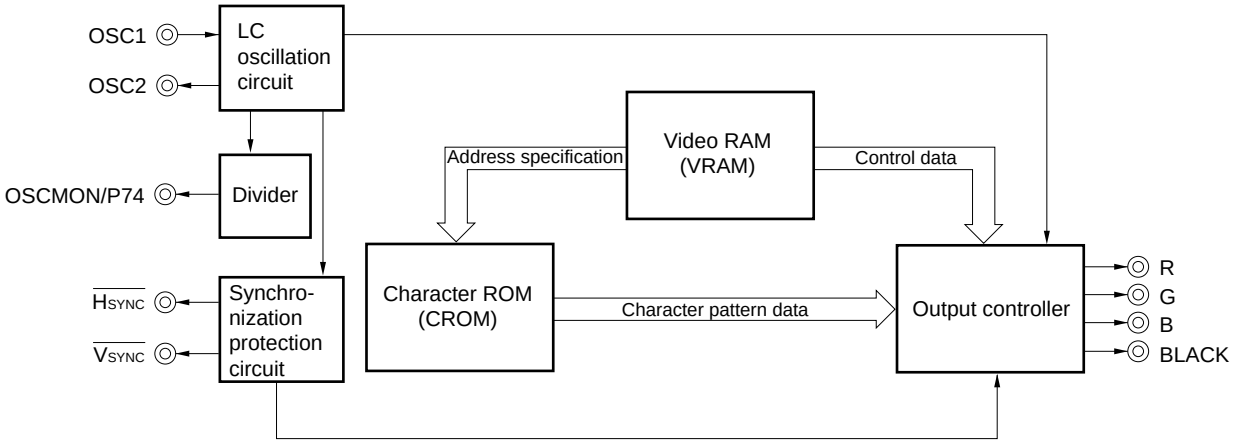


3.6 OSD Controller

OSD (On-screen display) is a function to display the channel number, volume, and time on the TV screen. User-programmable display patterns for OSD are defied in the CROM (character ROM) area.

The patterns actually displayed are stored in VRAM (video RAM).

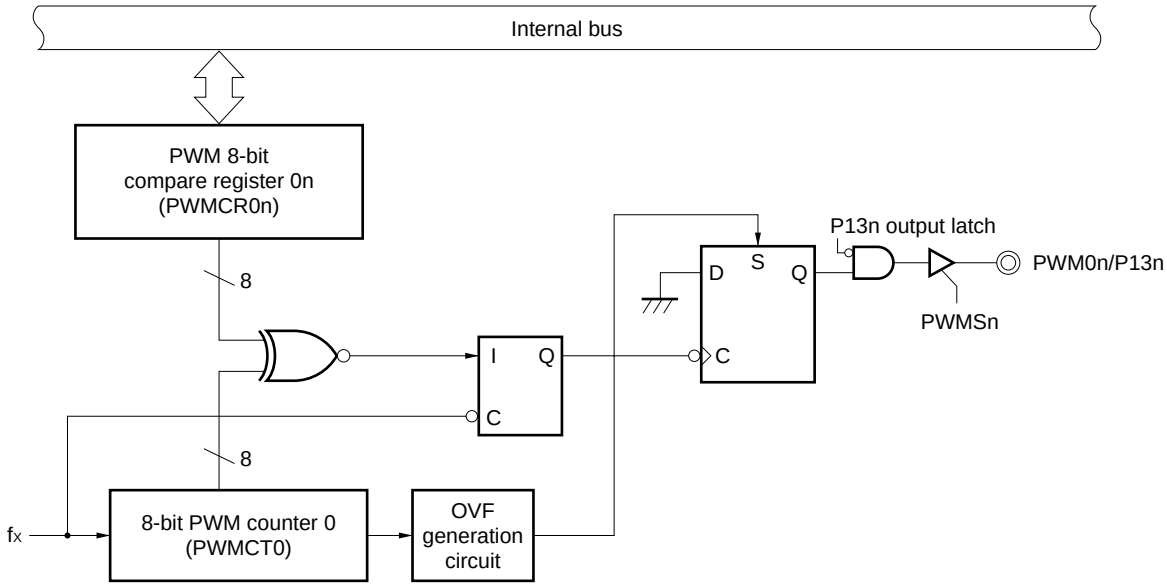
Figure 3-11. Block Diagram of OSD Controller



3.7 PWM Output

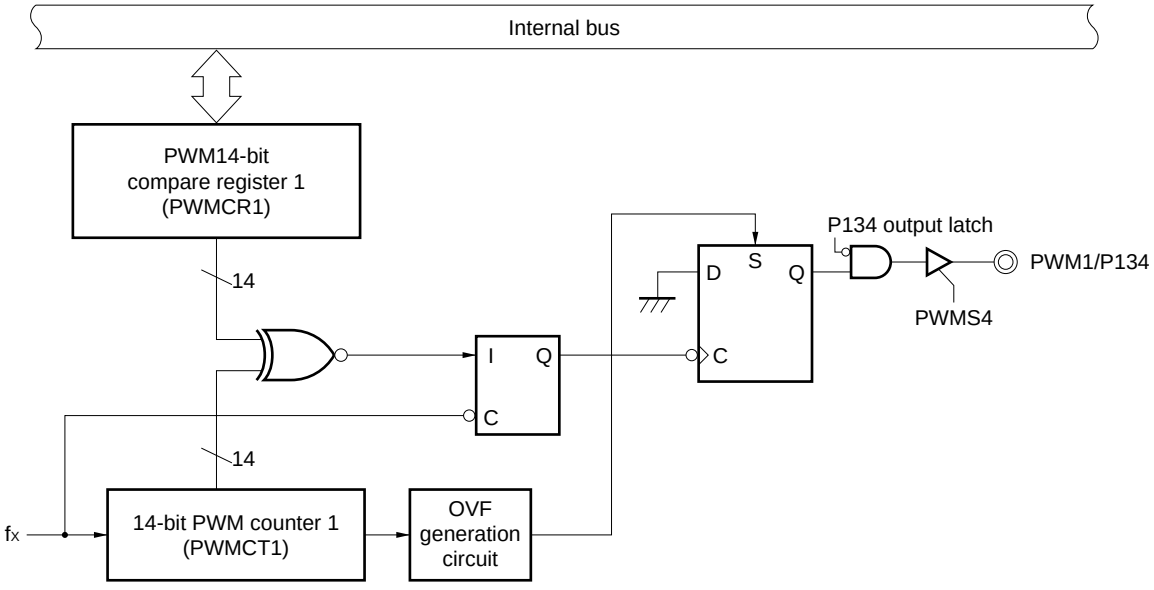
Four 8-bit PWM output channels and one 14-bit PWM output channel are provided.

Figure 3-12. Block Diagram of 8-Bit PWM (PWM0)



Remark PWMSn: Bit n of PWM output select register (PWMS)
n = 0 to 3

Figure 3-13. Block Diagram of 14-Bit PWM (PWM1)



Remark PWMS4: Bit 4 of PWM output select register (PWMS)

4. INTERRUPT FUNCTION

The following three types and 17 sources of interrupts are available:

- Non-maskable : 1 Note
- Maskable : 16 Note
- Software : 1

Note One of two types of interrupt sources (INTWDT), non-maskable and maskable (internal) is selectable as the watchdog timer interrupt source.

Table 4-1. Interrupt Sources

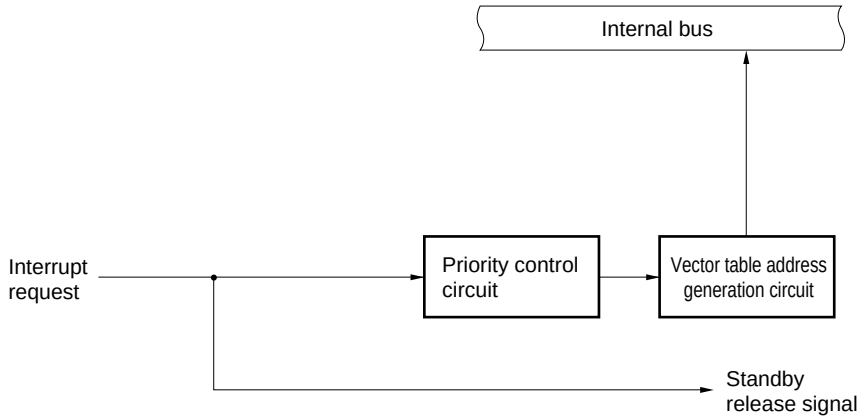
Interrupt Type	Default Priority Note 1	Interrupt Source		Internal/ External	Vector Table Address	Basic Configuration Type Note 2
		Name	Trigger			
Non-maskable	—	INTWDT	Overflow of watchdog timer (when non-maskable interrupt is selected)	Internal	0004H	(A)
Maskable	0	INTWDT	Overflow of watchdog timer (when interval timer mode is selected)			(B)
	1	INTP0	Detection of edge input to pin	External	0006H	(C)
	2	INTP1			0008H	
	3	INTP2			000AH	
	4	INTP3			000CH	
	5	INTTM90	Detection of 8-bit remote control timer (TM9) edge	Internal	000EH	(B)
	6	INTTM91			0010H	
	7	INTVSYNC	Detection of $\overline{V_{SYNC}}$ signal edge	External	0012H	(C)
	8	INTTM21	Generation of coincidence signal from 8-bit event counter (TM21)	Internal	0014H	(B)
	9	INTIIC1	End of transfer of serial interface (IIC1)		0016H	
	10	INTTM92	Overflow of 8-bit remote control timer (TM9)		0018H	
	11	INTCSI3	End of transfer of serial interface (SIO3)		001AH	
	12	INTTM5	Generation of coincidence signal from 8-bit timer/event counter (TM5)		001CH	
	13	INTTM20	Generation of coincidence signal from 8-bit timer (TM20)		001EH	
	14	INTBTM1	Signal generation by basic timer (BTM1) at 1- or 10-ms intervals		0020H	
	15	INTAD	End of conversion of A/D converter		0022H	
Software	—	BRK	Execution of BRK instruction	—	003EH	(D)

Notes 1. The default priority is used if two or more maskable interrupts occur at the same time. 0 is the highest and 15 is the lowest.

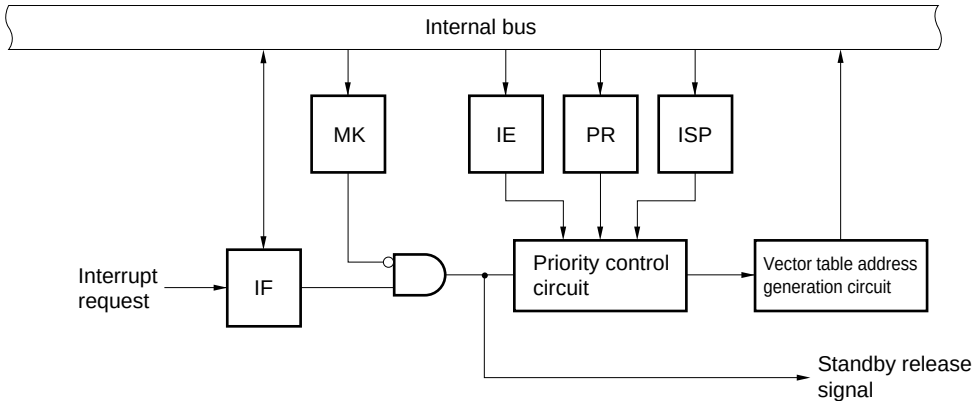
2. (A) through (D) in Basic Configuration Type correspond to (A) through (D) in Figure 4-1.

Figure 4-1. Basic Configuration of Interrupt Functions (1/2)

(A) Internal non-maskable interrupt



(B) Internal maskable interrupt



(C) External maskable interrupt

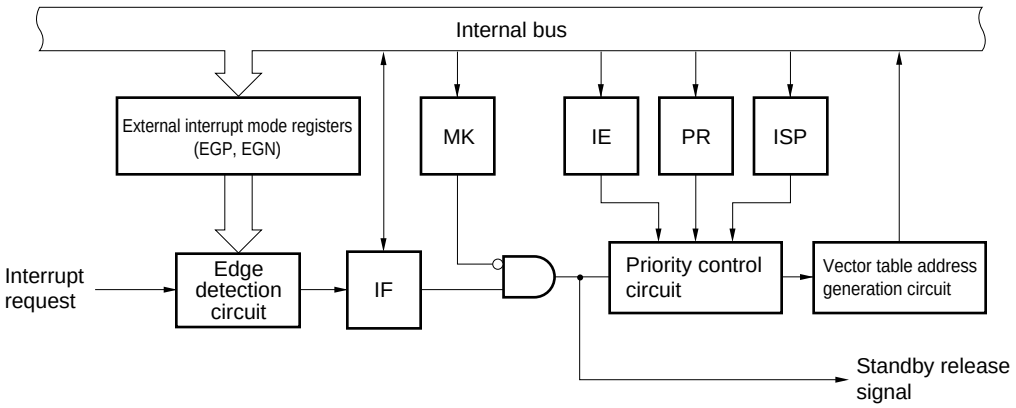
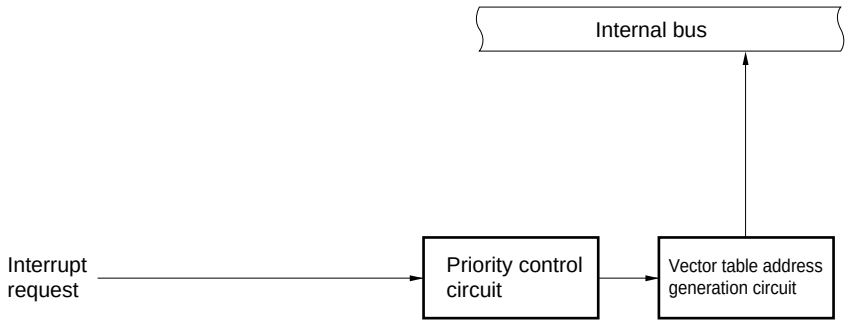


Figure 4-1. Basic Configuration of Interrupt Functions (2/2)

(D) Software interrupt



Remark IF : Interrupt request flag
IE : Interrupt enable flag
ISP : In-service priority flag
MK : Interrupt mask flag
PR : Priority specification flag

5. ROM CORRECTION

The μPD178046 and 178048 allow part of the program in the mask ROM to be replaced with a program in the internal expansion RAM for execution.

By using this ROM correction function, bugs found in the mask ROM can be removed and program flow can be changed.

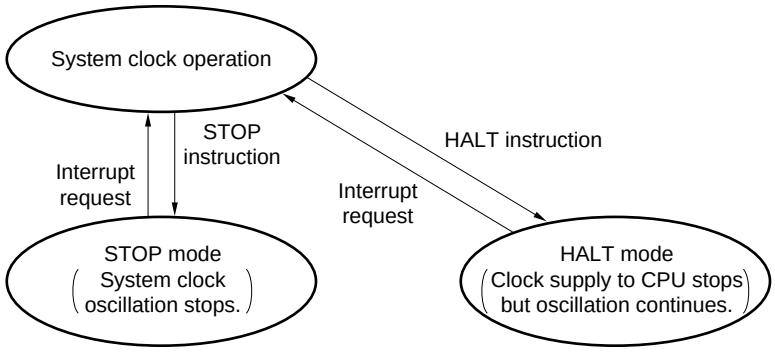
The ROM correction function can be used at up to two places in the internal ROM (program).

6. STANDBY FUNCTION

The standby function is used to reduce the current power consumption and can be used in the following two modes.

- HALT mode : The operation clock of the CPU is stopped in this mode. The average current consumption can be reduced by using this mode in combination with the normal operation mode and operating intermittently.
- STOP mode: The oscillation of the system clock is stopped in this mode. All the operations using the system clock are stopped and therefore, the current consumption can be substantially reduced.

Figure 6-1. Standby Function



7. RESET FUNCTION

The μPD178046 and 178048 can be reset in the following three ways:

- External reset by using the $\overline{\text{RESET}}$ pin
- Internal reset by detecting hang-up time of the watchdog timer
- Internal reset by means of power-ON clear (POC)

8. INSTRUCTION SET

(1) 8-bit instructions

MOV, XCH, ADD, ADDC, SUB, SUBC, AND, OR, XOR, CMP, MULU, DIVUW, INC, DEC, ROR, ROL, RORC, ROLC, ROR4, ROL4, PUSH, POP, DBNZ

Second Operand / First Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
A	ADD ADDC SUB SUBC AND OR XOR CMP		MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV	MOV XCH	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP	MOV XCH ADD ADDC SUB SUBC AND OR XOR CMP		ROR ROL RORC ROLC	
r	MOV	MOV ADD ADDC SUB SUBC AND OR XOR CMP											INC DEC
B, C											DBNZ		
sfr	MOV	MOV											
saddr	MOV ADD ADDC SUB SUBC AND OR XOR CMP	MOV									DBNZ		INC DEC
!addr16		MOV											
PSW	MOV	MOV											PUSH POP
[DE]													

Note Except r = A

First Operand \ Second Operand	#byte	A	r[Note]	sfr	saddr	!addr16	PSW	[DE]	[HL]	[HL+byte] [HL+B] [HL+C]	$addr16	1	None
[HL]		MOV											ROR4 ROL4
[HL+byte] [HL+B] [HL+C]		MOV											
X													MULU
C													DIVUW

Note Except r = A

(2) 16-bit instructions

MOVW, XCHW, ADDW, SUBW, CMPW, PUSH, POP, INCW, DECW

First Operand \ Second Operand	#word	AX	rp[Note]	sfrp	saddrp	!addr16	SP	None
AX	ADDW SUBW CMPW		MOVW XCHW	MOVW	MOVW	MOVW	MOVW	
rp	MOVW	MOVW[Note]						INCW DECW PUSH POP
sfrp	MOVW	MOVW						
saddrp	MOVW	MOVW						
!addr16		MOVW						
SP	MOVW	MOVW						

Note Only when rp = BC, DE, or HL

(3) Bit manipulation instruction

MOV1, AND1, OR1, XOR1, SET1, CLR1, NOT1, BT, BF, BTCLR

Second Operand / First Operand	A.bit	sfr.bit	saddr.bit	PSW.bit	[HL].bit	CY	$addr16	None
A.bit						MOV1	BT BF BTCLR	SET1 CLR1
sfr.bit						MOV1	BT BF BTCLR	SET1 CLR1
saddr.bit						MOV1	BT BF BTCLR	SET1 CLR1
PSW.bit						MOV1	BT BF BTCLR	SET1 CLR1
[HL].bit						MOV1	BT BF BTCLR	SET1 CLR1
CY	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1	MOV1 AND1 OR1 XOR1			SET1 CLR1 NOT1

(4) Call instruction/branch instruction

CALL, CALLF, CALLT, BR, BC, BNC, BZ, BNZ, BT, BF, BTCLR, DBNZ

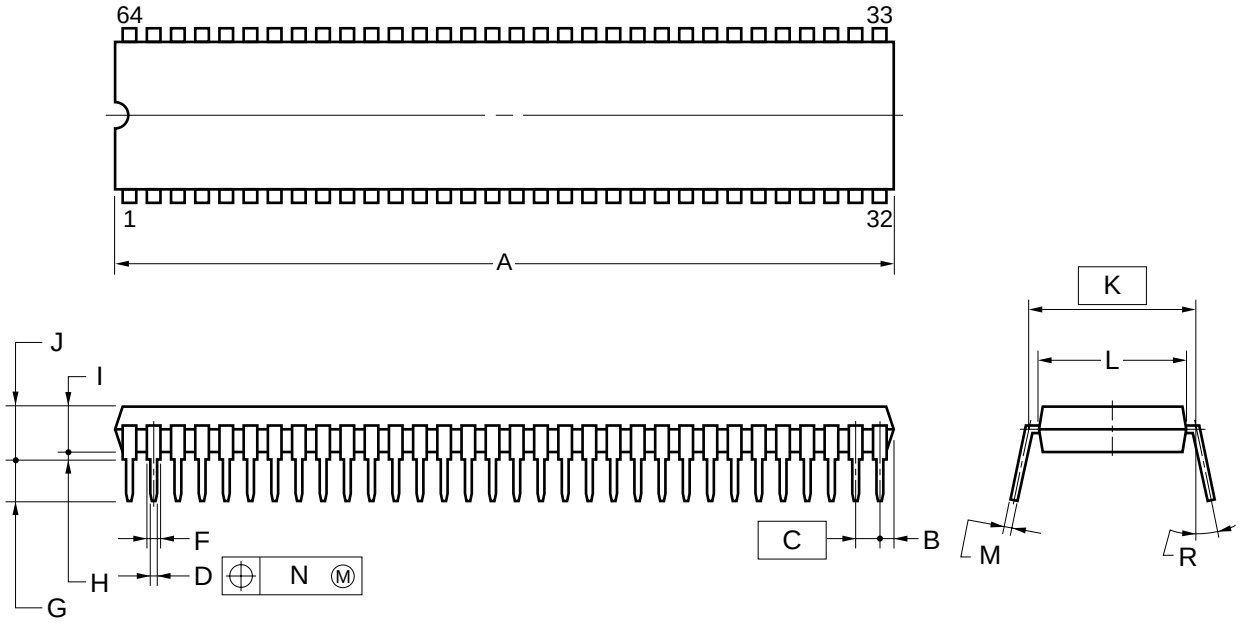
Second Operand / First Operand	AX	!addr16	!addr11	[addr5]	$addr16
Basic instruction	BR	CALL BR	CALLF	CALLT	BR, BC, BNC BZ, BNZ
Compound instruction					BT, BF BTCLR DBNZ

(5) Other instructions

ADJBA, ADJBS, BRK, RET, RETI, RETB, SEL, NOP, EI, DI, HALT, STOP

9. PACKAGE DRAWING

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTES

1. Controlling dimension—— millimeter.
2. Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
3. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	$58.0^{+0.68}_{-0.20}$	$2.283^{+0.028}_{-0.008}$
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50±0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	$4.05^{+0.26}_{-0.20}$	$0.159^{+0.011}_{-0.008}$
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0±0.2	$0.669^{+0.009}_{-0.008}$
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0 to 15°	0 to 15°

P64C-70-750A,C-3

APPENDIX A. DEVELOPMENT TOOLS

The following systems are available for developing a system using the μPD178046 and 178048.
Also refer to **(5) Note on using development tools**.

(1) Language processor software

RA78K/0	Common 78K/0 series assembler package
CC78K/0	Common 78K/0 series C compiler package
DF178048[Note]	Device file for μPD178048 subseries
CC78K/0-L	Common 78K/0 series C compiler library source file

(2) Flash memory writing tools

Flashpro II	Dedicated Flash Pro
Product name pending[Note]	Flash writing adapter

(3) Debugging tools

IE-78K0-NS	Common 78K/0 series in-circuit emulator
IE-70000-MC-PS-B	Power supply unit for IE-78K0-NS
IE-70000-98-IF-C	Interface adapter when PC-9800 series (except notebook type) is used as host machine
IE-70000-CD-IF	PC card and interface cable when notebook type of PC-9800 series is used as host machine
IE-70000-PC-IF-C	Interface adapter when IBM PC/AT™ or compatible machine is used as host machine
IE-178048-NS-EM1[Note]	Emulation board for emulating μPD178048 subseries
Product name pending[Note]	Emulation probe for 64-pin plastic shrink DIP
ID78K0-NS[Note]	Integrated debugger for IE-78K0-NS
SM78K0	Common system simulator for 78K/0 series
DF178048[Note]	Device file for μPD178048 subseries

Note Under development

(4) Real-time OS

RX78K/0	Real-time OS for 78K/0 series
MX78K0	OS for 78K/0 series

(5) Notes on using development tools

- Use the ID78K0-NS and SM78K0 with the DF178048.
- Use the RX78K/0 with the RA78K/0 and DF178048.
- The Flashpro II, flash writing adapter (product name pending), and emulation probe (product name pending) are products of Naito Densei Machida Mfg. Co., Ltd. (TEL (044) 822-3813). Consult NEC when purchasing these products.
- For a description of development tools from the third parties, refer to **78K/0 Series Selection Guide (U11126E)**.
- The host machine and OS corresponding to each software package are as follows:

Host Machine [OS] / Software	PC	EWS
	PC-9800 series [Japanese Windows™] IBM PC/AT and compatible machine [Japanese/English Windows]	HP9000 series 700™ [HP-UX™] SPARCstation™ [SunOS™] NEWS (RISC)™ [NEWS-OS™]
RA78K/0	○ Note	○
CC78K/0	○ Note	○
ID78K0-NS	○	—
SM78K0	○	—
RX78K/0	○ Note	○
MX78K0	○ Note	○

Note DOS-based software

APPENDIX B. RELATED DOCUMENTS

Device-related documents

Document Name		Document No.	
		Japanese	English
μPD178F048 Preliminary Product Information		U13056J	Planned
μPD178048 Subseries User's Manual		Planned	Planned
78K/0 Series User's Manual - Instruction		U12326J	U12326E
78K/0 Series Instruction Set		U10904J	—
78K/0 Series Instruction Table		U10903J	—
μPD178048 Subseries Special Function Register Table		Planned	—
78K/0 Series Application Note	Fundamentals (I)	U12704J	IEA-1288

Documents on development tools (User's Manuals)

Document Name		Document No.	
		Japanese	English
RA78K0 Assembler Package	Operation	U11802J	U11802E
	Assembly language	U11801J	U11801E
	Structured assembly language	U11789J	U11789E
RA78K Series Structured Assembler Preprocessor		U12323J	EEU-1402
CC78K0 C Compiler	Operation	U11517J	U11517E
	Language	U11518J	U11518E
CC78K0 C Compiler Application Note	Programming Know-How	U13034J	EEA-1208
CC78K Series Library Source File		U12322J	—
IE-78K0-NS		Planned	Planned
IE-178048-NS-EM1		Planned	Planned
SM78K0 System Simulator Windows Based	Reference	U10181J	U10181E
SM78K Series System Simulator	External part user open interface specifications	U10092J	10092E
ID78K0-NS Integrated Debugger PC Based	Reference	U12900J	Planned

Caution The contents of the above documents are subject to change without notice. Be sure to use the latest edition of each document for designing.

Documents on embedded software (User's Manuals)

Document Name		Document No.	
		Japanese	English
78K/0 Series Real-Time OS	Fundamentals	U11537J	U11537E
	Installation	U11536J	U11536E
78K/0 Series OS MX78K0	Fundamentals	U12257J	U12257E

Other related documents

Document Name	Document No.	
	Japanese	English
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535J	C10535E
Quality Grades on NEC Semiconductor Devices	C11531J	C11531E
NEC Semiconductor Device Reliability/Quality Control System	C10983J	C10983E
Guide to Prevent Damage for Semiconductor Devices by Electrostatic Discharge (ESD)	C11892J	C11892E
Semiconductor Device Quality/Reliability Handbook	C12769J	Under preparation
Microcomputer Product Series Guide	U11416J	—

Caution The contents of the above documents are subject to change without notice. Be sure to use the latest edition of each document for designing.

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

Purchase of NEC I^2C components conveys a license under the Philips I^2C Patent Rights to use these components in an I^2C system, provided that the system conforms to the I^2C Standard Specification as defined by Philips.

Regional Information

Some information contained in this document may vary from country to country. Before using any NEC product in your application, please contact the NEC office in your country to obtain a list of authorized representatives and distributors. They will verify:

- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

In addition, trademarks, registered trademarks, export restrictions, and other legal issues may also vary from country to country.

NEC Electronics Inc. (U.S.)
Santa Clara, California
Tel: 408-588-6000
800-366-9782
Fax: 408-588-6130
800-729-9288

NEC Electronics (Germany) GmbH
Duesseldorf, Germany
Tel: 0211-65 03 02
Fax: 0211-65 03 490

NEC Electronics (UK) Ltd.
Milton Keynes, UK
Tel: 01908-691-133
Fax: 01908-670-290

NEC Electronics Italiana s.r.1.
Milano, Italy
Tel: 02-66 75 41
Fax: 02-66 75 42 99

NEC Electronics (Germany) GmbH
Benelux Office
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Tel: 040-2445845
Fax: 040-2444580

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Tel: 01-30-67 58 00
Fax: 01-30-67 58 99

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Spain Office
Madrid, Spain
Tel: 01-504-2787
Fax: 01-504-2860

NEC Electronics (Germany) GmbH
Scandinavia Office
Taeby, Sweden
Tel: 08-63 80 820
Fax: 08-63 80 388

NEC Electronics Hong Kong Ltd.
Hong Kong
Tel: 2886-9318
Fax: 2886-9022/9044

NEC Electronics Hong Kong Ltd.
Seoul Branch
Seoul, Korea
Tel: 02-528-0303
Fax: 02-528-4411

NEC Electronics Singapore Pte. Ltd.
United Square, Singapore 1130
Tel: 65-253-8311
Fax: 65-250-3583

NEC Electronics Taiwan Ltd.
Taipei, Taiwan
Tel: 02-719-2377
Fax: 02-719-5951

NEC do Brasil S.A.
Cumbica-Guarulhos-SP, Brasil
Tel: 011-6465-6810
Fax: 011-6465-6829

J98. 2

The related documents referred to in this publication may include preliminary versions.
However, preliminary versions are not marked as such.

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