AN1645
APPLICATION NOTE

STSR2P/STSR2PM SIMPLIFIES IMPLEMENTATION OF SYNCHRONOUS RECTIFIERS IN FORWARD CONVERTER

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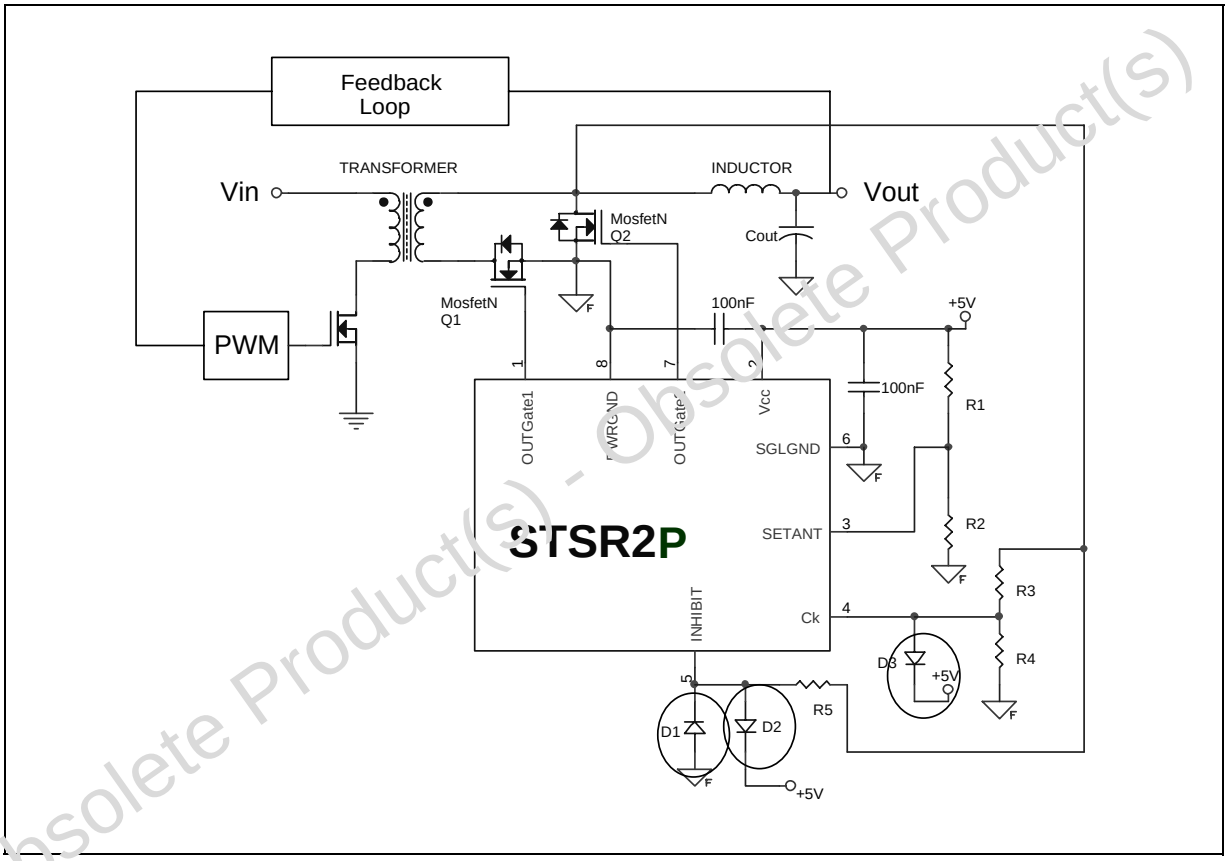
1. ABSTRACT

This paper describes the functionality and the operation of the STSR2P device used as the secondary synchronous rectifier driver in Forward topology switched mode power supplies. A schematic and layout description of a demo board, able to replace diode rectification with synchronous rectification in Forward converters, is shown below.

Figure 1: Typical Application Schematic



2. GENERAL DEVICE DESCRIPTION

The STSR2P Smart Driver IC provides two complementary high current outputs to drive Power Mosfets. The IC is dedicated to properly drive secondary Synchronous Rectifiers in medium power, low output voltage, high efficiency Forward Converters. From a synchronizing clock input, the IC generates two driving signals with a certain dead time between complementary pulses. The adopted transitions

revelation mechanism makes circuit operation independent by the forward magnetic reset technique used, avoiding most of the common problems inherent in self-driven synchronous rectifiers. The IC operation prevents secondary side shoot-through conditions providing proper timing at the outputs turn-off transition. This smart function operates through a fast cycle-after-cycle control logic mechanism based on an internal high frequency oscillator, synchronized by the clock signal. The IC provides a fixed anticipation in turning-off the OUTGate1 with respect to the clock signal transition, while the anticipation in turning-off the OUTGate2 can be set through external components. A special Inhibit function allows the shut-off of one of the two outputs allowing operation during discontinuous conduction mode and preventing the freewheeling mosfet from sinking current from the output.
The STSR2P automatically turns off the outputs when duty-cycle is lower than 13%, while STSR2PM works even at very low duty-cycle values.

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3. PIN CONNECTIONS AND DESCRIPTIONS

The STSR2P is housed in a SO-8 package for SMD assembly. Device pin out is shown in figure 2 and table 1 briefly summarizes the device pin functionality.

Figure 2: Pin Configuration

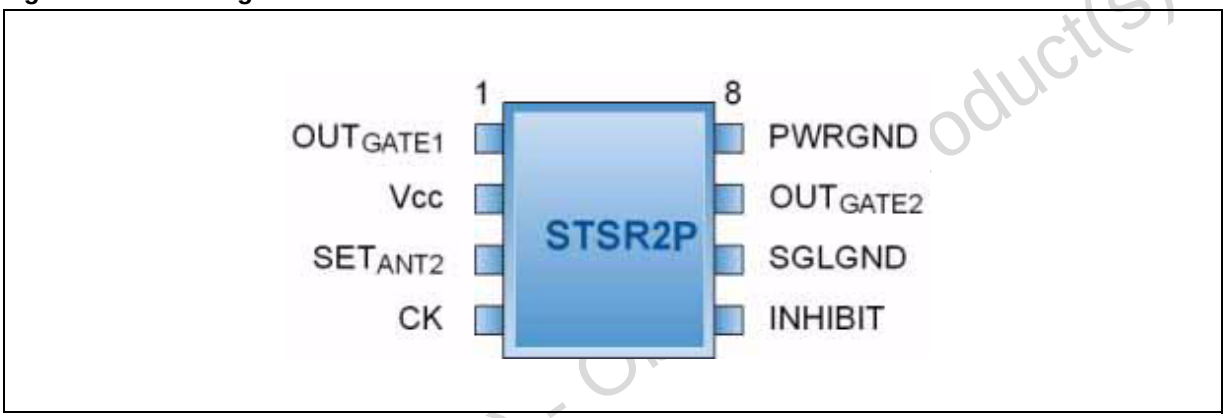
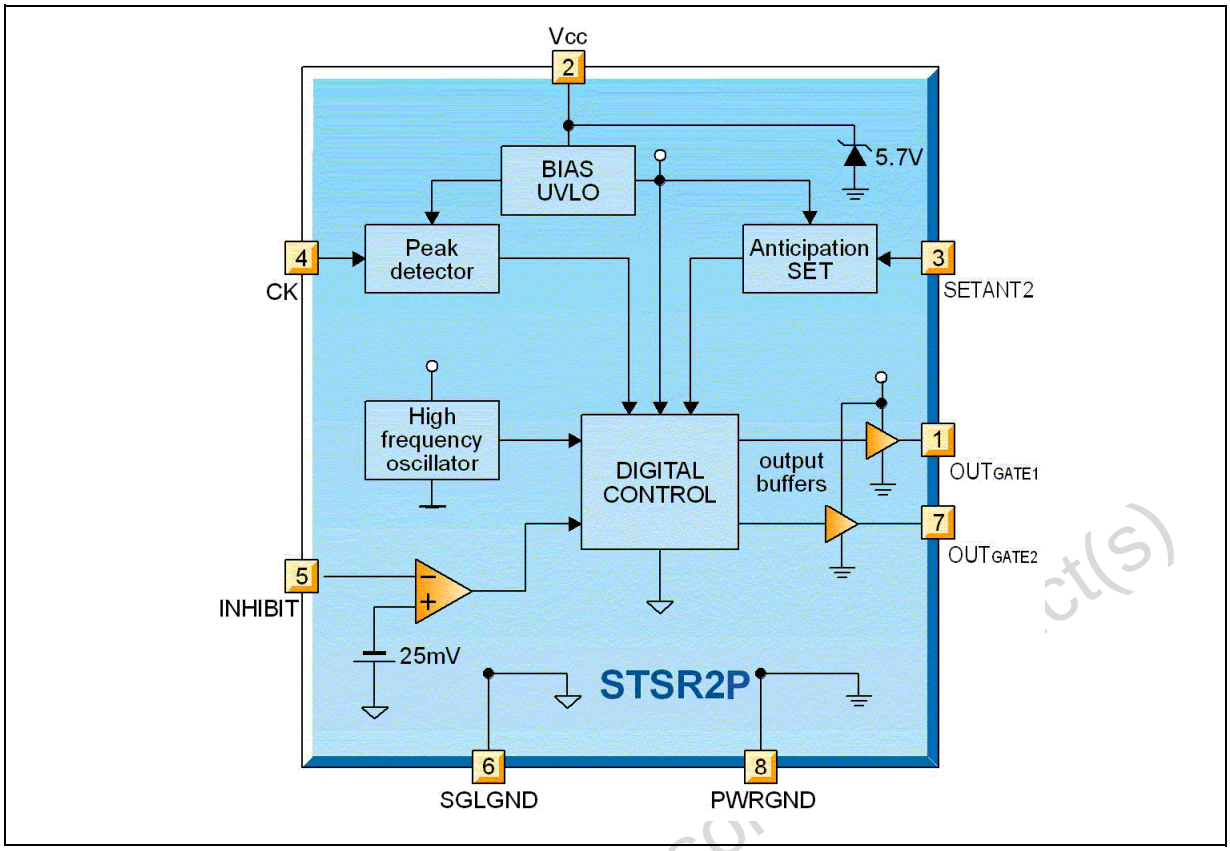


Table 1: Pin Configuration

Pin Number	Pin Name	Pin Function
1	OUTGate1	Output for Forward MOSFET Gate Drive
2	Vcc	Supply input from 4V to 5.5V
3	$SETANT_2$	Sets the anticipation in turning-off the OUT_{GATE2}
4	CK	Synchronization for IC's operation
5	INHIBIT	Discontinuous Mode Detector
6	SGLGND	Reference for all the control logic signals
7	OUTGate2	Output for Freewheeling MOSFET Gate Drive
8	PWRGND	Reference for power signals

Figure 3: Block Schematic



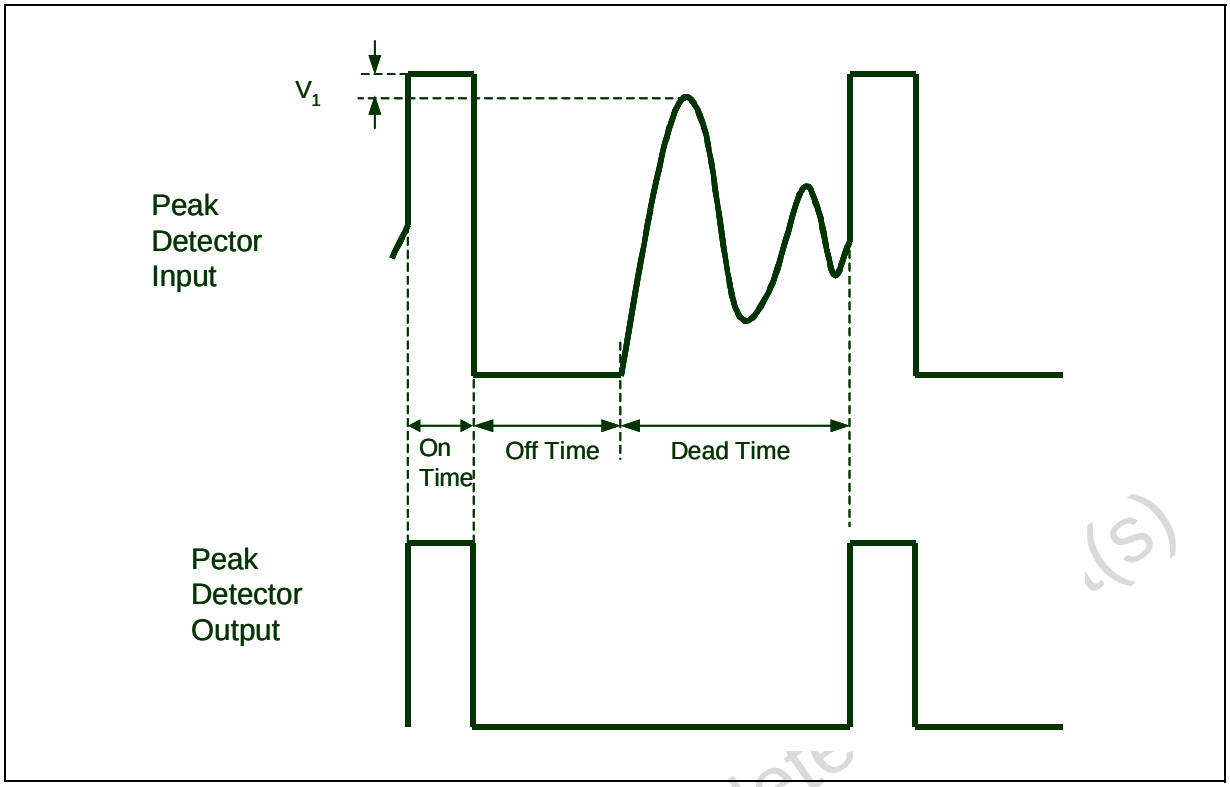
4. SUPPLY VOLTAGE AND UNDER VOLTAGE LOCK-OUT

The supply input range is from 4V to 5.5V. An internal zener diode limits the maximum voltage to 5.7V.
A 100nF ceramic capacitor must be connected to Vcc and SGLGND pin in order to assure a stable supply voltage. This capacitor must be placed very close to the device. Another 100nF capacitor is necessary between Vcc and PWRGND.
Under Voltage Lock Out feature guarantees proper start-up while it avoids undesirable driving during eventual dropping of the supply voltage.
As shown in the Block Diagram, the Vcc voltage also supplies the two output drivers, consequently the maximum driving voltage is 5.5V, so the use of logic gate threshold mosfets is recommended.

5. SYNCHRONIZATION

An innovative feature of the STSR2P is the capability to operate in the secondary side without any synchronization signal coming from the primary side. The IC synchronization is obtained directly from the secondary side using the voltage across the free wheeling mosfet as the information for the switching transitions. The Ck pin is the input for the synchronization signal; the internal threshold is set at 2.8V. As can be seen in figure 3, a Peak Detector is present at the Ck pin. This block is able to distinguish between the primary mosfet switching transitions and the eventual sinusoidal waveform caused by discontinuous mode operation (see figure 4). A wrong synchronization causes wrong driving of the synchronous rectifiers.

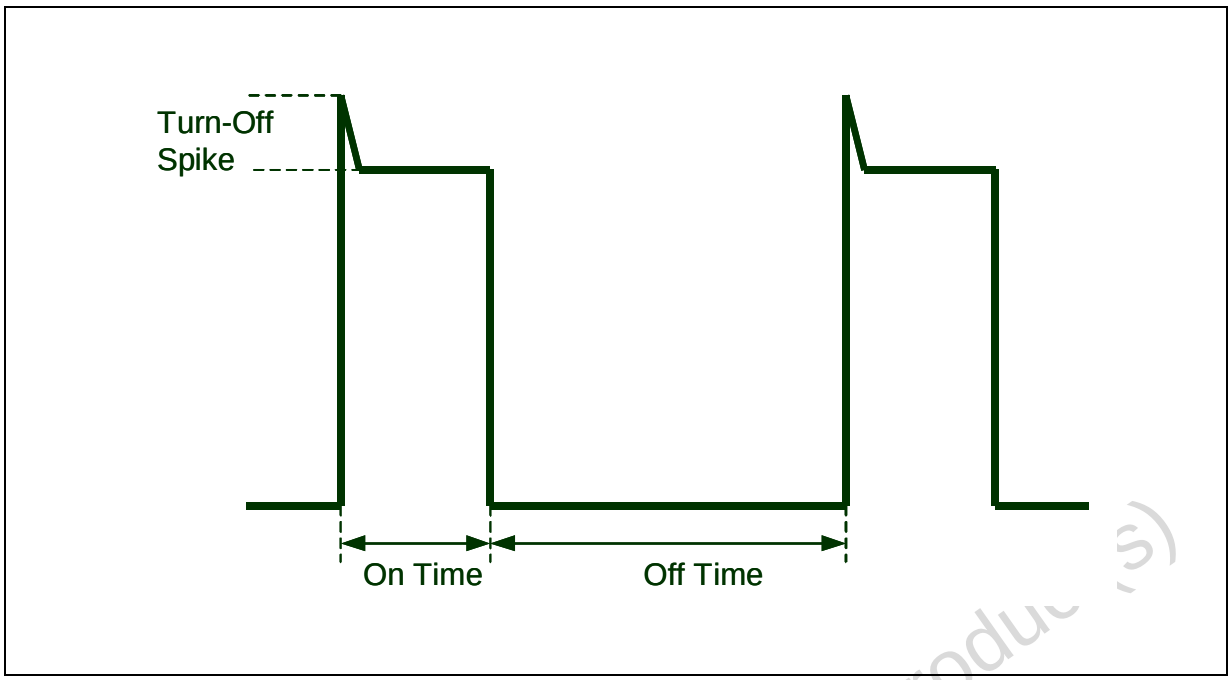
Figure 4: DCM waveform



5.1 Continuous Conduction Mode

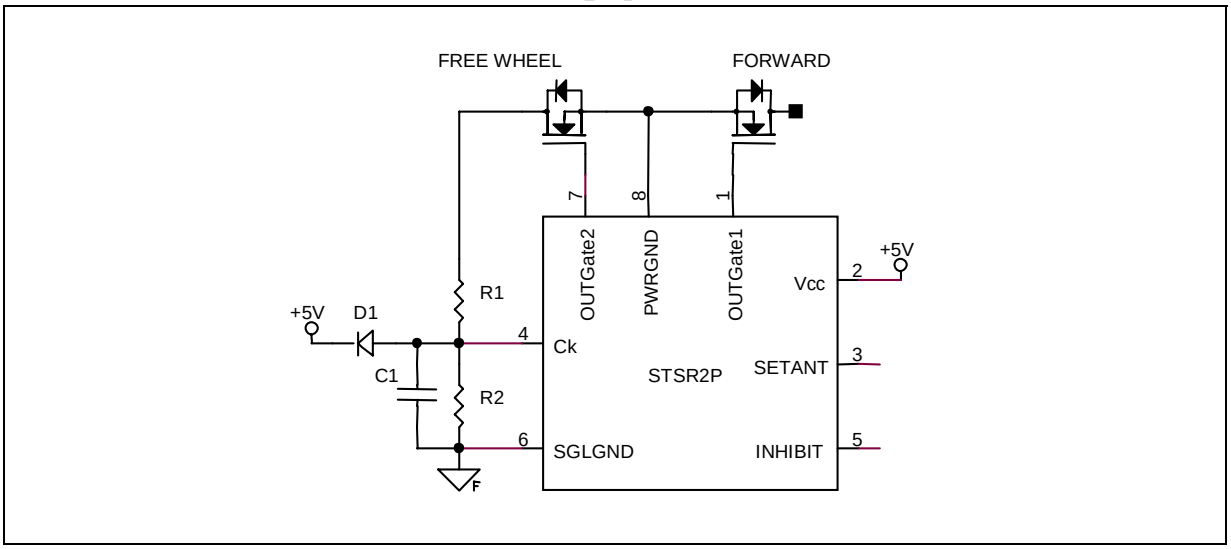
When the converter is working in continuous mode the voltage across the source and drain of the free wheeling mosfet has a square shape. This voltage can be applied to the Ck pin using two different configurations: with a resistor divider (figure 6) or with a diode and pull-up resistor (figure 7). In most cases a spike is present during turn-off of the synchronous mosfet; this spike must be eliminated at the Ck pin in order to avoid false synchronization.
Using the resistor divider, the spike is eliminated by adding a small capacitor (C1) as shown in figure 6.

Figure 5: CCM waveform and Ck circuit



In a typical Forward converter for telecom application, the DC input voltage has a 1:2 variability range (typically 36V-72V). Consequently the secondary winding voltage has also 1:2 variability. The resistor divider can be calculated in order to have about 2.8V at the Ck pin at 36V input; at 72V input, the Ck pin reaches 5.6V. Even if this value is higher than the maximum voltage on the CK pin, it can be accepted limiting the current flowing into the pin to 10mA.

Figure 6: Synchronization with a resistor divider



In case the Forward converter has a higher variability range 1:3 or 1:4, at minimum input voltage, 2.8V must be guaranteed at the Ck pin. At maximum input voltage, the voltage at the Ck pin will be 7.5V or 10V. This voltage exceeds the absolute maximum ratings of the device. If R2 limits the current flowing into the Ck pin to a value below the maximum Ck current value indicated in the datasheet (10mA), the

device can still working properly; otherwise a diode D1 connected to Vcc or a zener diode must be added to protect the device.

Figure 7: Synchronization with a diode and pull-up resistor

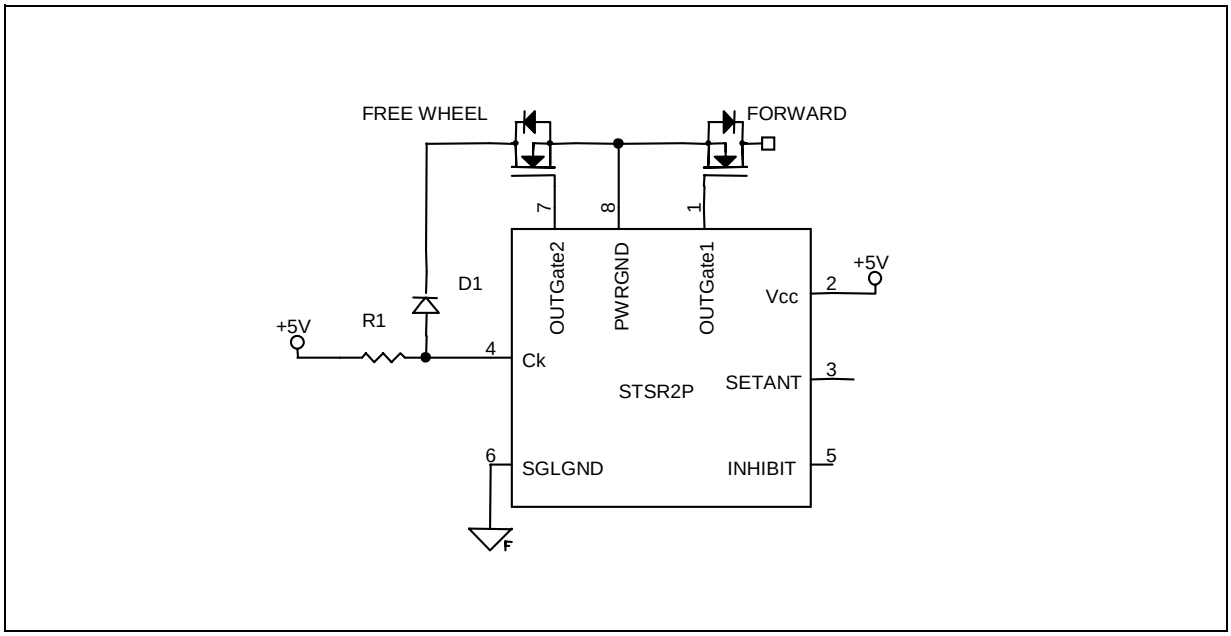
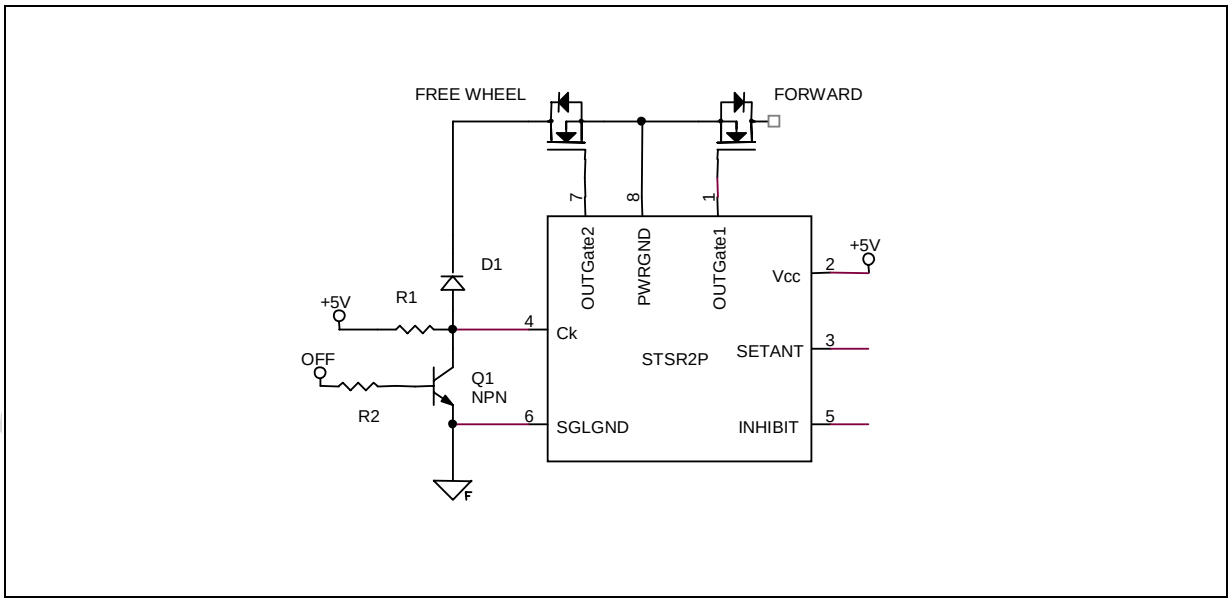


Figure 7 shows the synchronization circuit with diode and pull-up resistor. In this case there is no problem with the turn-off spike and maximum CK pin voltage. This circuit cannot work properly in Discontinuous Mode due to the ringing present in the voltage drain of the synchronous rectifier.

Figure 8: Shut-down circuit



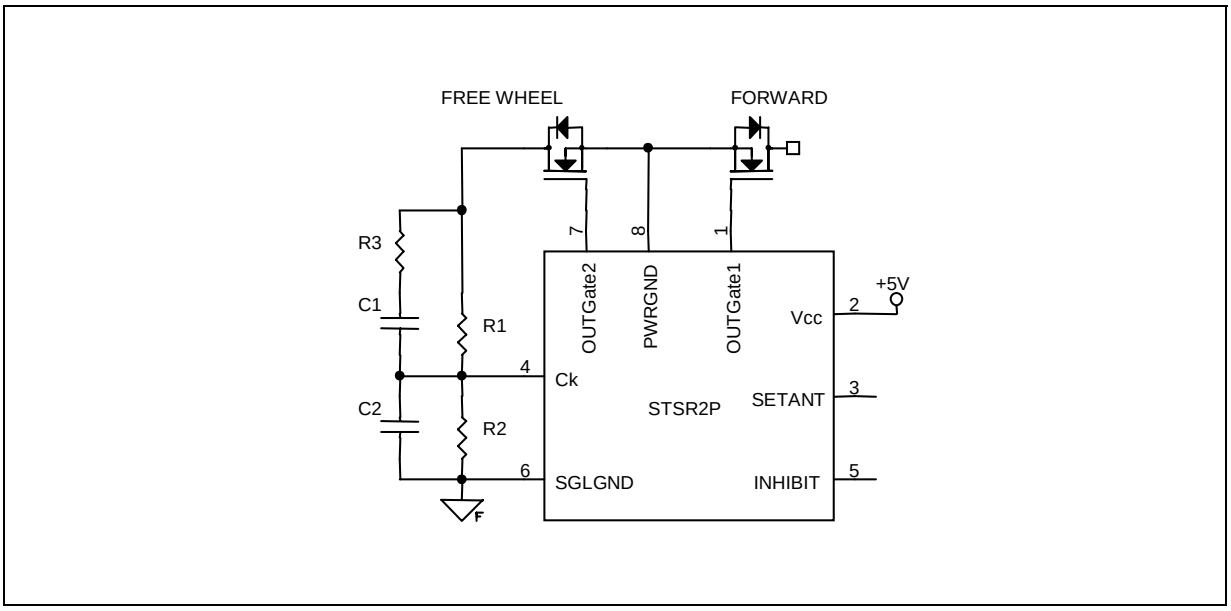
The STSR2P can be easily turned off adding a NPN transistor between Ck and SGLGND. This transistor forces the CK pin to GND when the signal OFF is high. In this condition OUTGate1 and OUTGate2 will be in a low state turning off the Synchronous Mosfets.

Figure 8 shows the turn-off circuit when using a diode and pull-up resistor to synchronize the STSR2P, the same configuration of Q1 and R2 can be used with a resistor divider circuit.

5.2 Discontinuous Conduction Mode

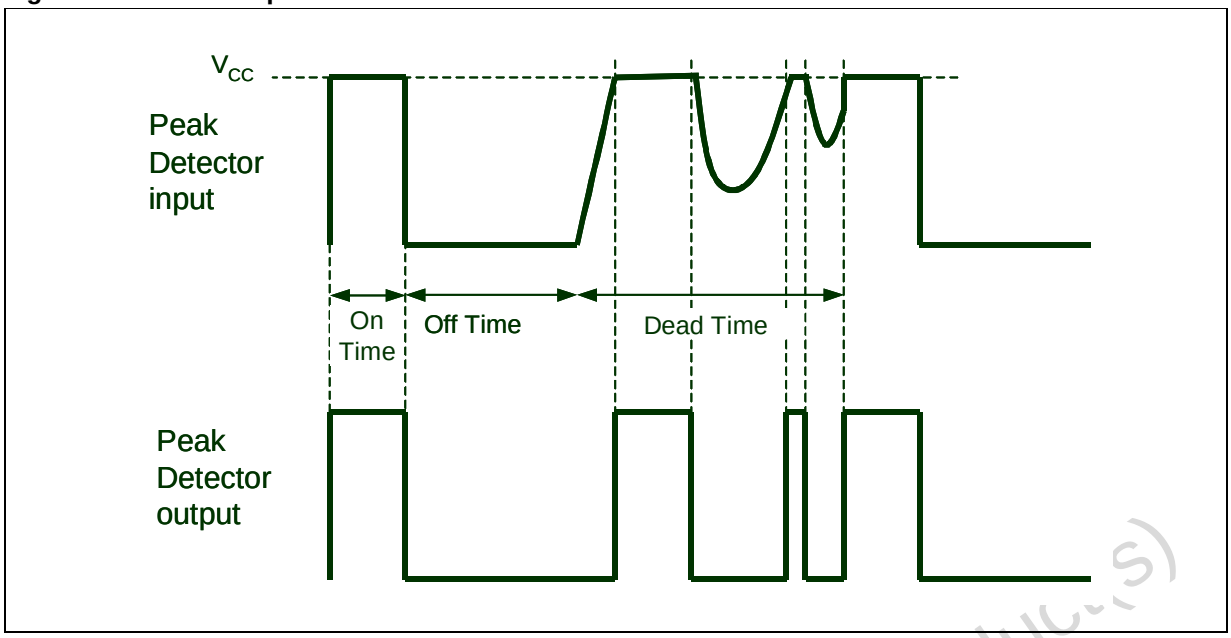
As shown in figure 4, in discontinuous mode operation there can be some problems in detecting the primary switching transitions. The internal peak detector is only able to determine the peak value reached by the signal at the Ck pin, neglecting all signals that have a lower value. A minimum voltage difference V1=400mV between the switching transition waveform and the sinusoidal waveform must be assured in order to allow the Peak Detector to work properly. If the ringing presents almost the same value as the square waveform, it is possible to add a filter circuit to the CK pin in order to obtain a better operation. This circuit is showed in figure 9. R1-R2 and C2 form a low pass filter, which allows a reduction of the ringing amplitude. But R1-R2 and C2 also cause an undesired delay, so the R3 and C1 group reduce this delay during fast switching transitions.

Figure 9: Filter to CK input



As mentioned in the previous paragraph, if the input voltage variability range is higher than 1:2, at high voltage the signal at the CK pin will be clamped. In these conditions, both switching transition waveform and the sinusoidal waveform are clamped and the peak detector is unable to operate correctly (see figure 10). In this case it is possible to use an external signal, which turns off completely the device in no load or light load conditions (figure 8).

Figure 10: DCM clamped



6. INHIBIT OPERATION

One of the differences between diode rectification and synchronous rectification is the possibility for Mosfets to conduct the current in both directions while diodes conduct just in one direction. In discontinuous mode with diode rectification, when the inductor current reaches zero it cannot reverse because the diode does not allow current flowing from cathode to anode. Using mosfets as rectifiers, when the inductor current reaches zero, it continues to decrease becoming negative and flowing from drain to source of the freewheeling mosfet. In this condition the converter works always in continuous mode.

If discontinuous mode operation is required, the freewheeling mosfet must be turned off when the current is zero, consequently the body diode operates as a common rectifier avoiding reversal of the inductor current.

The INHIBIT pin is able to turn off the freewheeling mosfet when its current is approaching zero allowing discontinuous mode operation of the converter.
On the INHIBIT pin, there is an internal comparator with a -25mV threshold. This pin is connected through a resistor to the drain of the freewheeling mosfet. At the beginning of the off time (when Ck goes to low level), $OUTGate_2$ goes high. The INHIBIT voltage is monitored for 250ns: if the voltage on INHIBIT is higher than -25mV, $OUTGate_2$ becomes low; if the voltage on INHIBIT is lower than -25mV, $OUTGate_2$ is kept high until the voltage reaches -25mV. This is because when the freewheeling mosfet is conducting, the voltage on its drain is: Vds= -Rds(on)*Idrain. If Vds is higher than -25mV, it means that the current is decreasing and discontinuous mode is approaching, so $OUTGate_2$ is turned-off allowing operation of the body diode of the mosfet (see figure 11). When the converter is in continuous mode the INHIBIT voltage is always lower than -25mV and $OUTGate_2$ is kept high. The turn off of the freewheeling mosfet occurs when the current is not exactly zero, the remaining amount of current is dependent on $R_{DS(on)}$ of the mosfet.

During transition in which the primary mosfet is turned off, the INHIBIT voltage must fall from high value to -25mV in less than 250ns. The resistor value R26 must be chosen in order to fit this specification.
When the converter operates in parallel with other power supplies, the INHIBIT pin, detecting the voltage across the freewheeling mosfet, also avoids the converter to sink current from the output.
Although the INHBIT pin allows operation in Discontinuous Mode, the -25mV threshold could be sensitive to the ringing present at the SR Mosfet drain (see figure 13), causing incomplete turn on of OUTGate2. This inconvenience can be avoided using the clock signal to provide a negative voltage to the INHIBIT pin acting as a blanking time. This negative voltage can be easily generated with some discrete components as shown in figure 12.

Figure 11: INHIBIT Voltage and Current

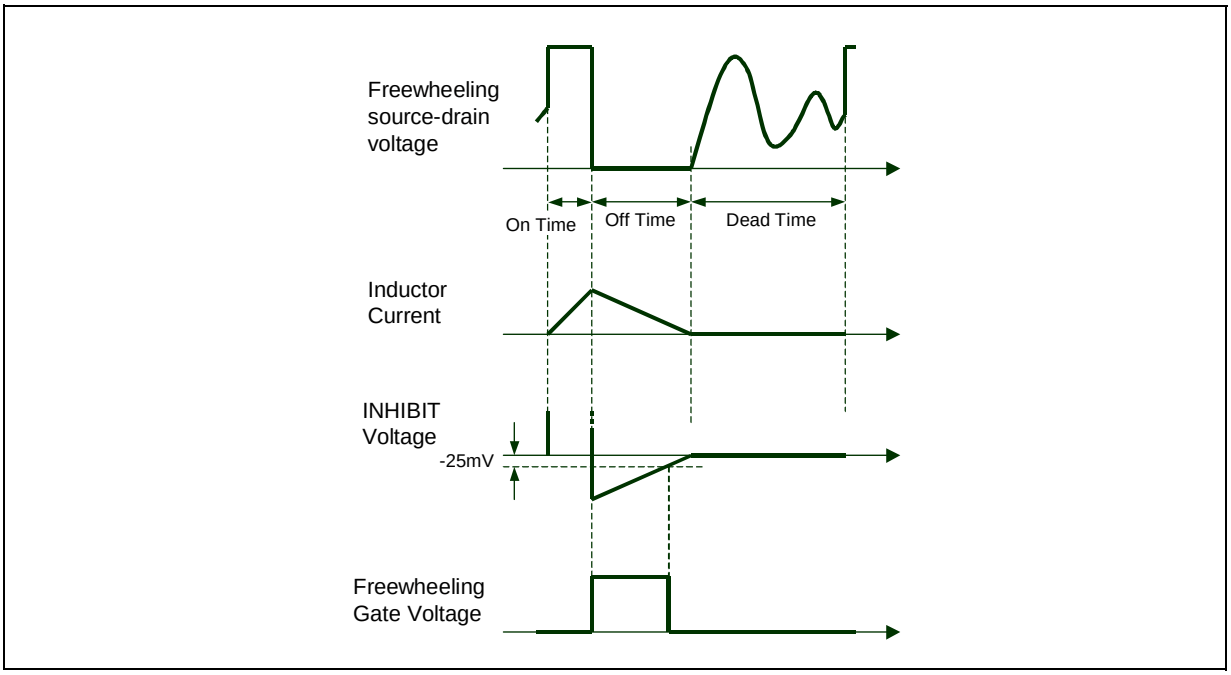
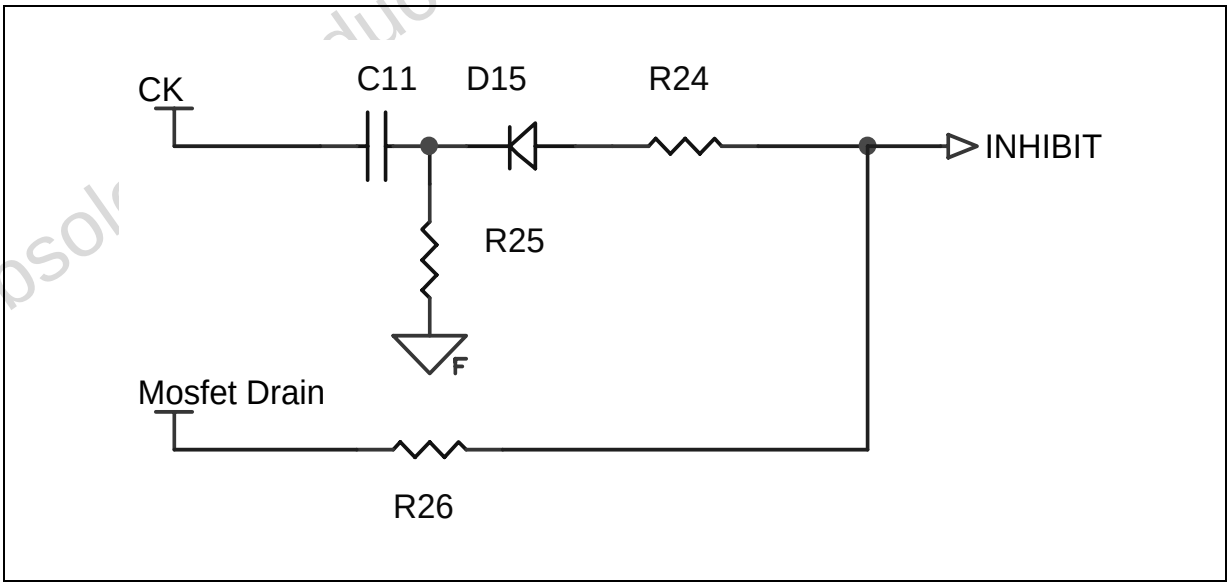
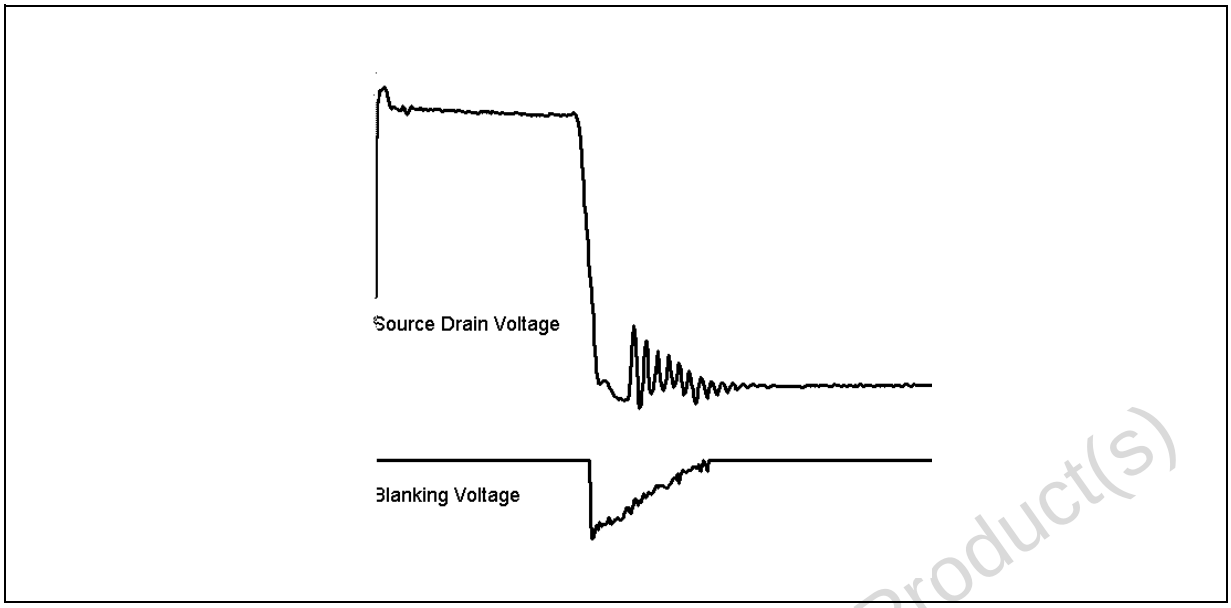


Figure 12: Circuit to provide negative voltage to INHIBIT



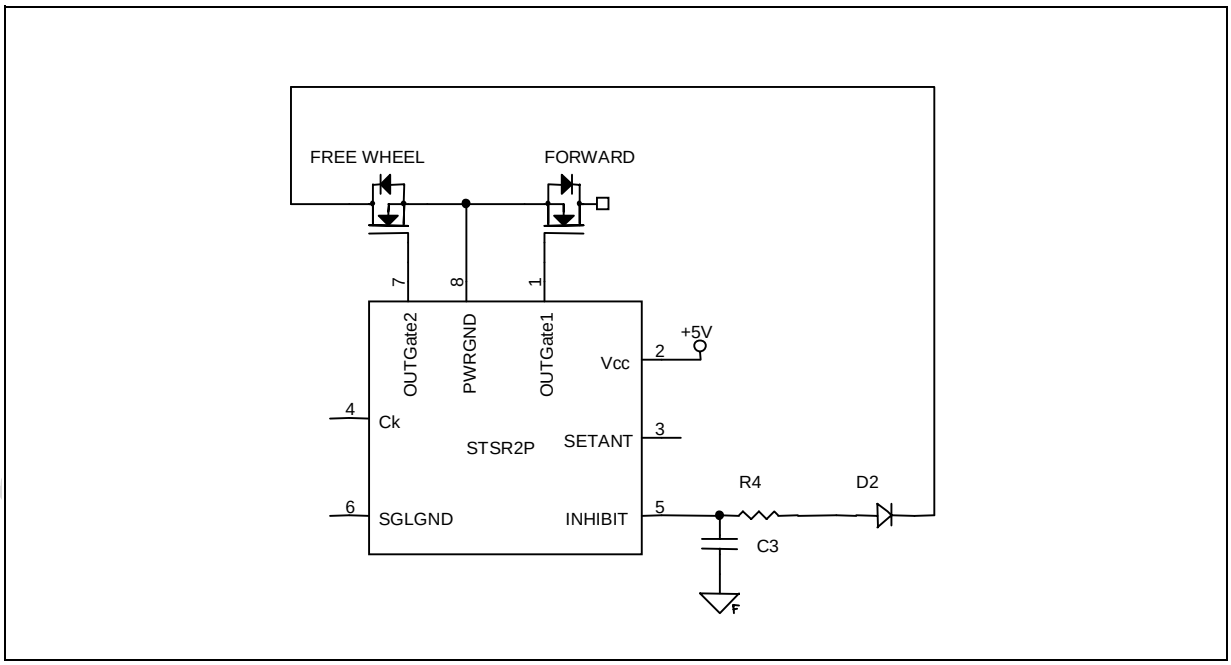
The blanking time value is determined by C11 and R25. This time has to last the necessary time to cover the ringing caused by the primary switch turn off (Figure.13).

Figure 13: Ringing during turn off of the primary switch



Inhibit pin can be totally disabled providing a constant negative voltage between -100mV and -600mV to the pin. A simple circuit which can be used to provide this voltage is showed in figure 14.

Figure 14: Disabling INHIBIT Pin



7. ANTICIPATION

One of the major problems of synchronous rectification is the generation of proper driving signals for the mosfets to avoid cross conduction. Contemporary conduction of the two mosfets must be avoided not only when the two mosfets are both in on state but also when just one is on and the other one is off. In fact it is possible to have a short circuit loop on the secondary side when the current flows through one mosfet that is on and the body diode of the other mosfet.

Referring to figure 15, when the primary Mosfet is turned-on, the voltage Vs tends to go positive. This voltage forward bias the body diode of the Forward mosfet (FR) and, due to some delay in turning-off the Freewheeling mosfet (FW), an unlimited current can flow in the short circuit loop determined by the FW, the body-diode of FR and the secondary winding of the isolation transformer. The value of the short circuit current is only limited by the parasitics of the circuit and eventually by the primary side protection circuits included in the PWM.
In order to avoid this undesired condition, the freewheeling mosfet must be turned off before the primary mosfet is turned on; this means that certain 'anticipation' is needed.
Similar considerations can be made for the transition in which the FR has to be turned-off.

Figure 15: Short circuit in the secondary side

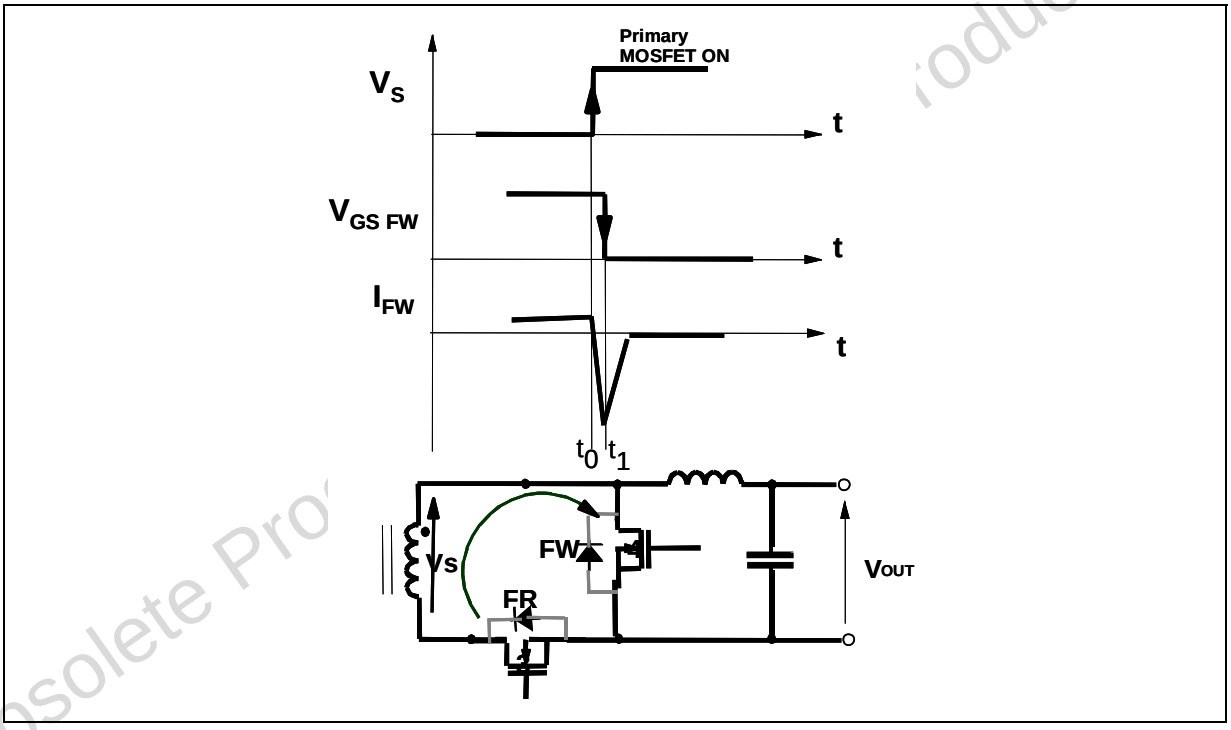


Figure 16 shows the detailed timing of Ck, OUTGate1 and OUTGate2 signals in normal operation. Time intervals tant1 and tant2 provide the required anticipation to avoid any short circuit condition in the secondary side. tant1 value is fixed internally while for tant2 it is possible to choose between three different values using the SETANT2 pin according to the following table.

Table 2: Anticipation values

Parameter		Value	Unit
t_{ant1}	Fixed internally	75	ns
t_{ant2}	$0<SET_{ANT2}<\frac{1}{3}Vcc$	75	ns
	$\frac{1}{3}Vcc<SET_{ANT2}<\frac{2}{3}Vcc$	150	ns
	$\frac{2}{3}Vcc<SET_{ANT2}<Vcc$	225	ns

The voltage on the SET_{ANT2} pin can be obtained using a resistor divider of the supply voltage.

The Digital Control Block generates these anticipations by counting the number of high frequency pulses included within the switching period and the On-time time interval. Due to the digital nature of this system, some bits can be lost during the counting, causing a jitter in the output driving signals (Figure 17). Table 2 shows the average OUTGate1 and OUTGate2 anticipation times.

Figure 16: STSR2P Timing

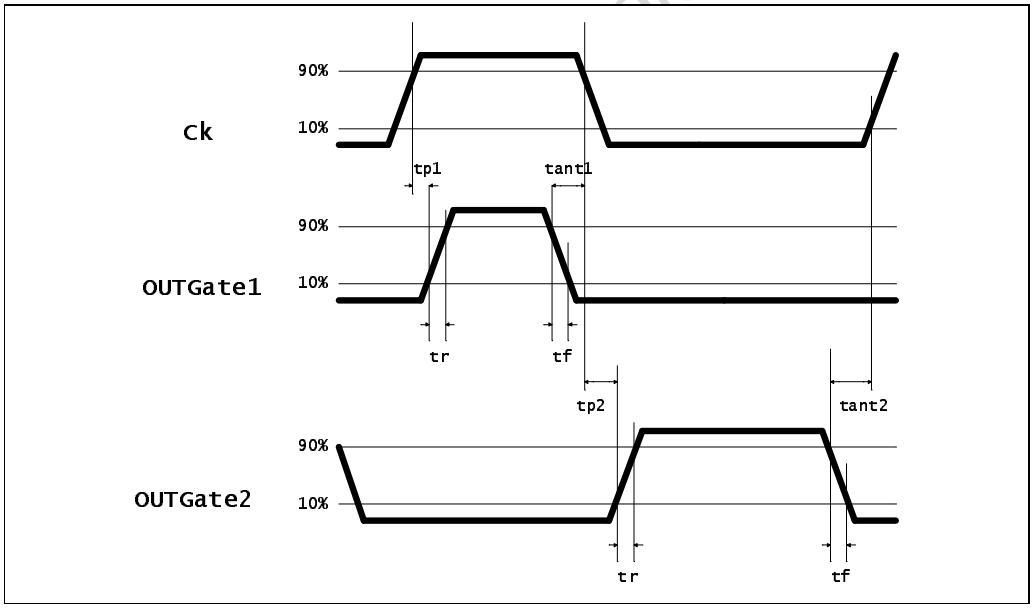
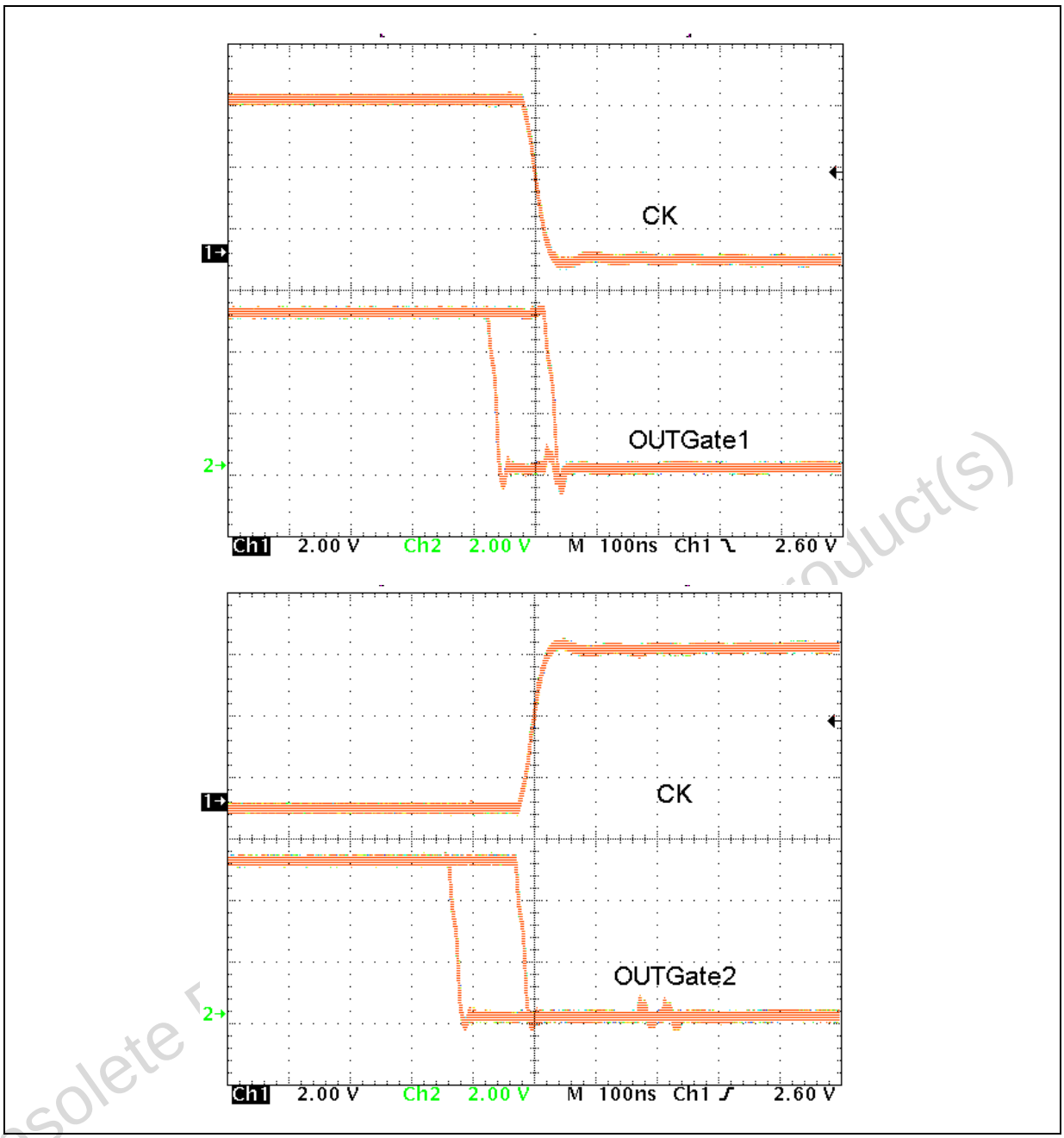


Figure 17: Jitter



8. NO LOAD AND LIGHT LOAD OPERATION

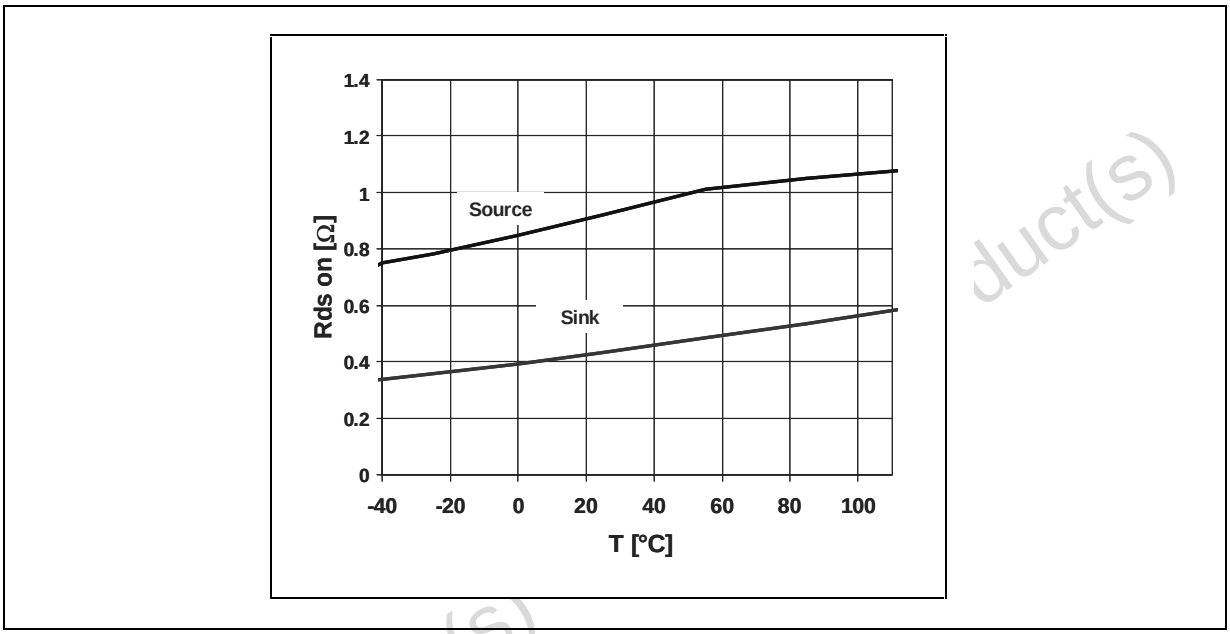
When the duty-cycle is lower than 14%, an internal feature of the STSR2P allows a total shutdown of OUTGate1 and OUTGate2 and of most internal parts of the device, causing a reduction in power consumption. In these conditions the low output current of the converter is carried by the body diode of the mosfets. The IC starts to operate again when the Duty-cycle is higher than 18%, therefore having a 4% of hysteresis. This feature allows correct operation when the primary PWM controller imposes burst mode due to the very light output load.

STSR2PM does not have this function and the two outputs follow the clock input even for very low duty-cycle values.

9. OUTPUT DRIVERS

The two output drivers have a high current capability, being able to source up to 2A and to sink up to 3.5A peak current. Consequently, the two mosfet are switched very quickly, allowing paralleling of several mosfets to reduce conduction losses. The high level driving voltage is equal to Vcc voltage; therefore the device drives properly logic level mosfets.

Figure 18: Rds(on) -sink/source vs Temp



10. TRANSIENT BEHAVIOUR

During very heavy load changes, the duty cycle can vary very fast from a low value to a high value and vice versa in a few switching periods.

The calculation to turn off OUTGate1 is based on On-time, so if the on time is changing very fast, the anticipation time cannot be provided. In any case, STSR2P has a safety feature, which turns off OUTGate1 when the CK input goes low. OUTgate1 will be turned off with a small delay with respect to the Ck input- 30ns max (Figure 19 b).
If the anticipation time for OUTGate2 is based on the calculation of the switching period (frequency) and not on duty cycle, even during fast duty cycle changes the anticipation time is provided correctly, always providing correct driving for the Synchronous Mosfet (Figure 19 c).

Figure 19a: Duty Cycle very fast variation

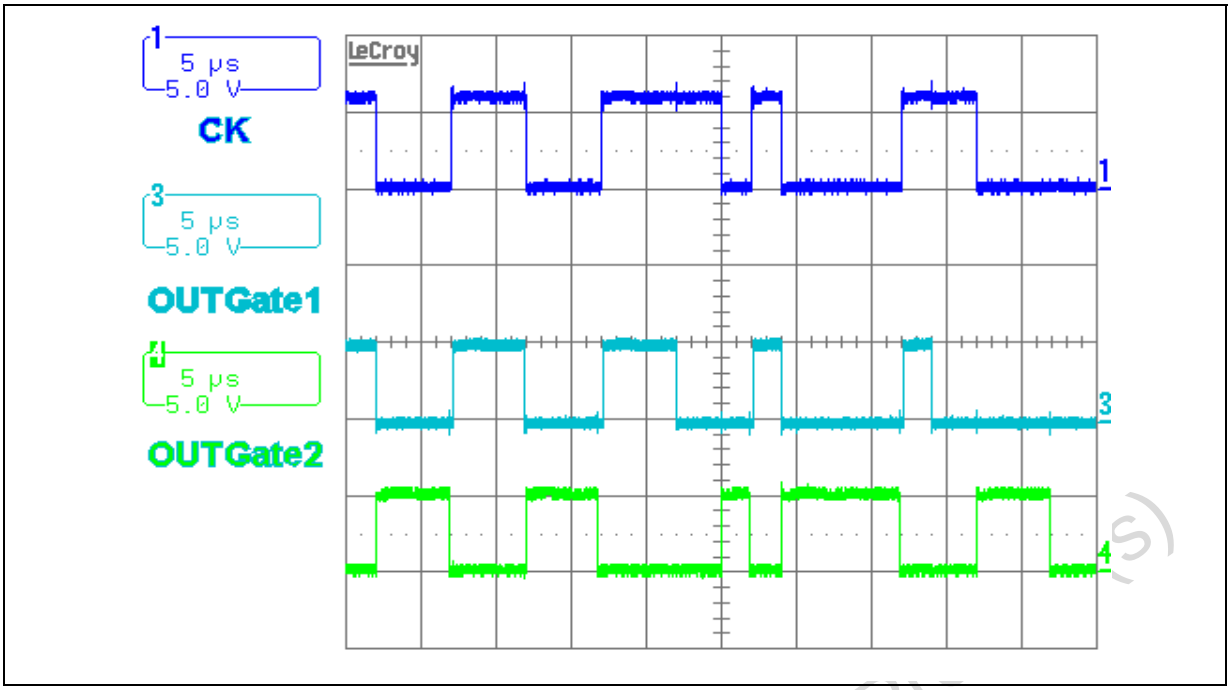


Figure 19b: Duty Cycle very fast variation

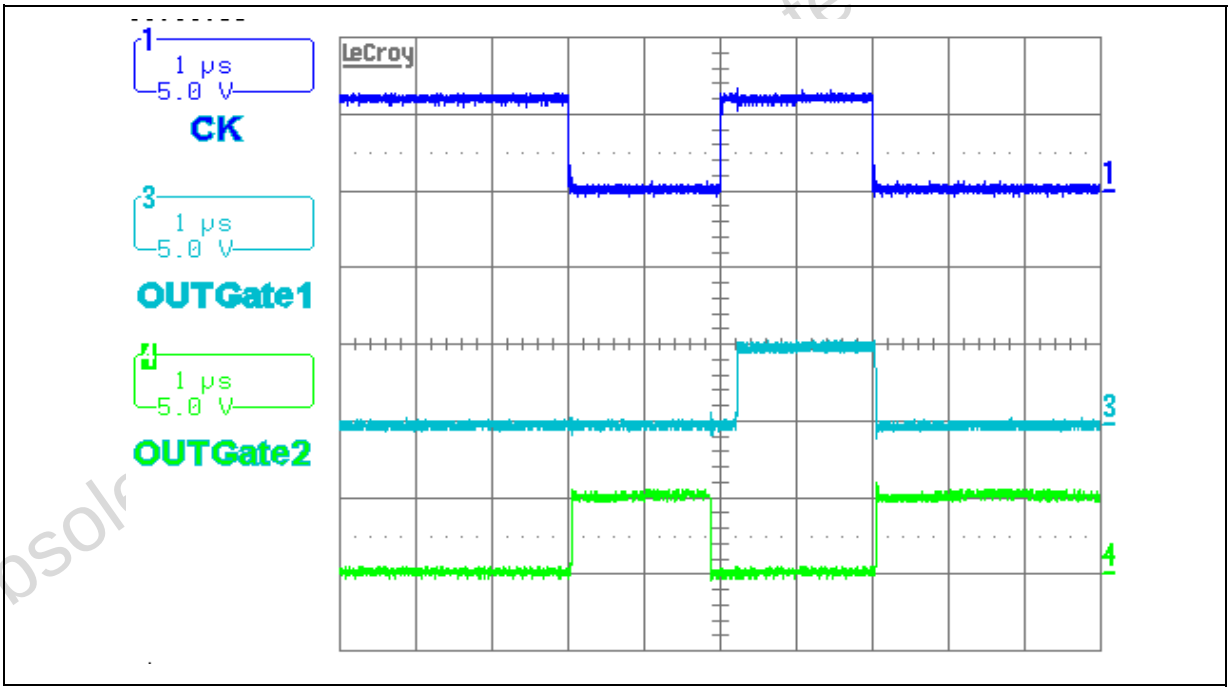


Figure 19c: Duty Cycle very fast variation

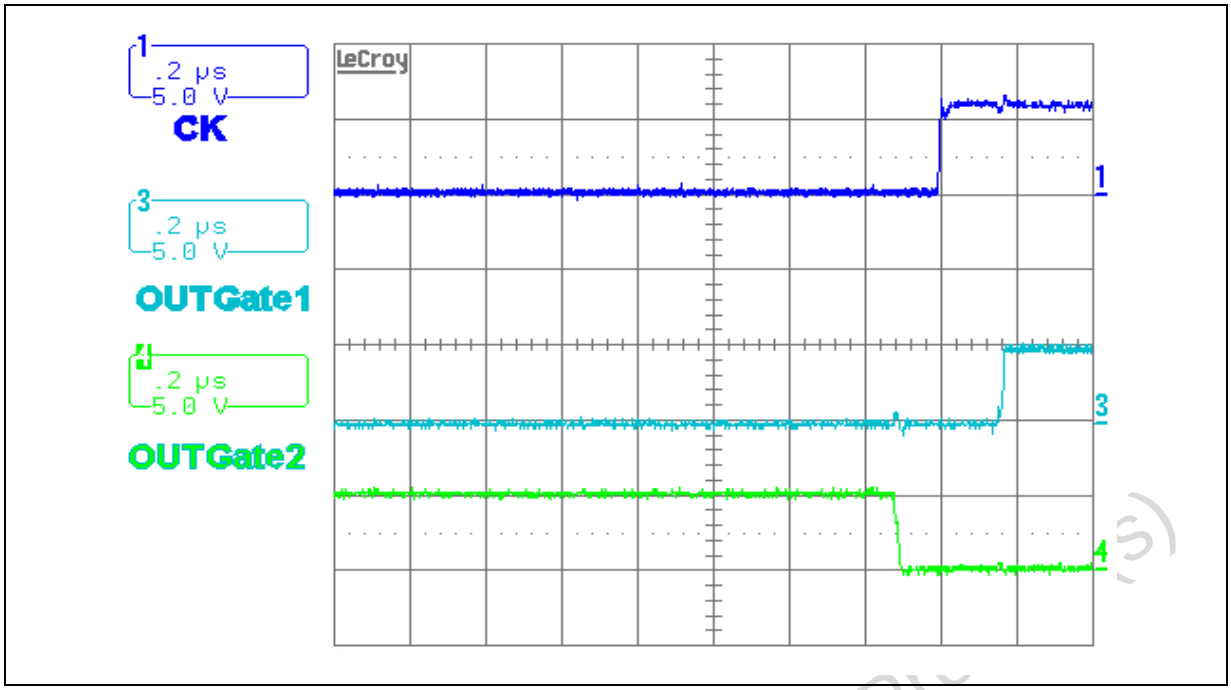


Figure 19-a shows the condition in which the duty cycle passes from 50% to 80% to 20% and back to 50% in four following cycles. In figure 19-b a magnification of OUTGate1 behavior is shown. Turn-off time has very small delay with respect to the clock input. In figure 19-c a magnification of OUTGate2 behavior is shown. Turn-off time maintains the anticipation time even with very strong duty-cycle variation assuring correct driving in heavy load transient conditions.

11. DEMOBOARD DESCRIPTION

The schematic of figure 20 presents a test board for the STSR2P. This board replaces forward and freewheeling diodes in a Forward converter. The board includes all the components needed by the STSR2P to operate. The board allows us to easily pass from diode rectification to synchronous rectification in Forward converter applications. The components inside the dotted boxes, can be chosen to implement different circuit configurations for Synchronization and for Inhibit pin. Table 3 shows a detailed components selection.

Figure 20: Demo board Schematic

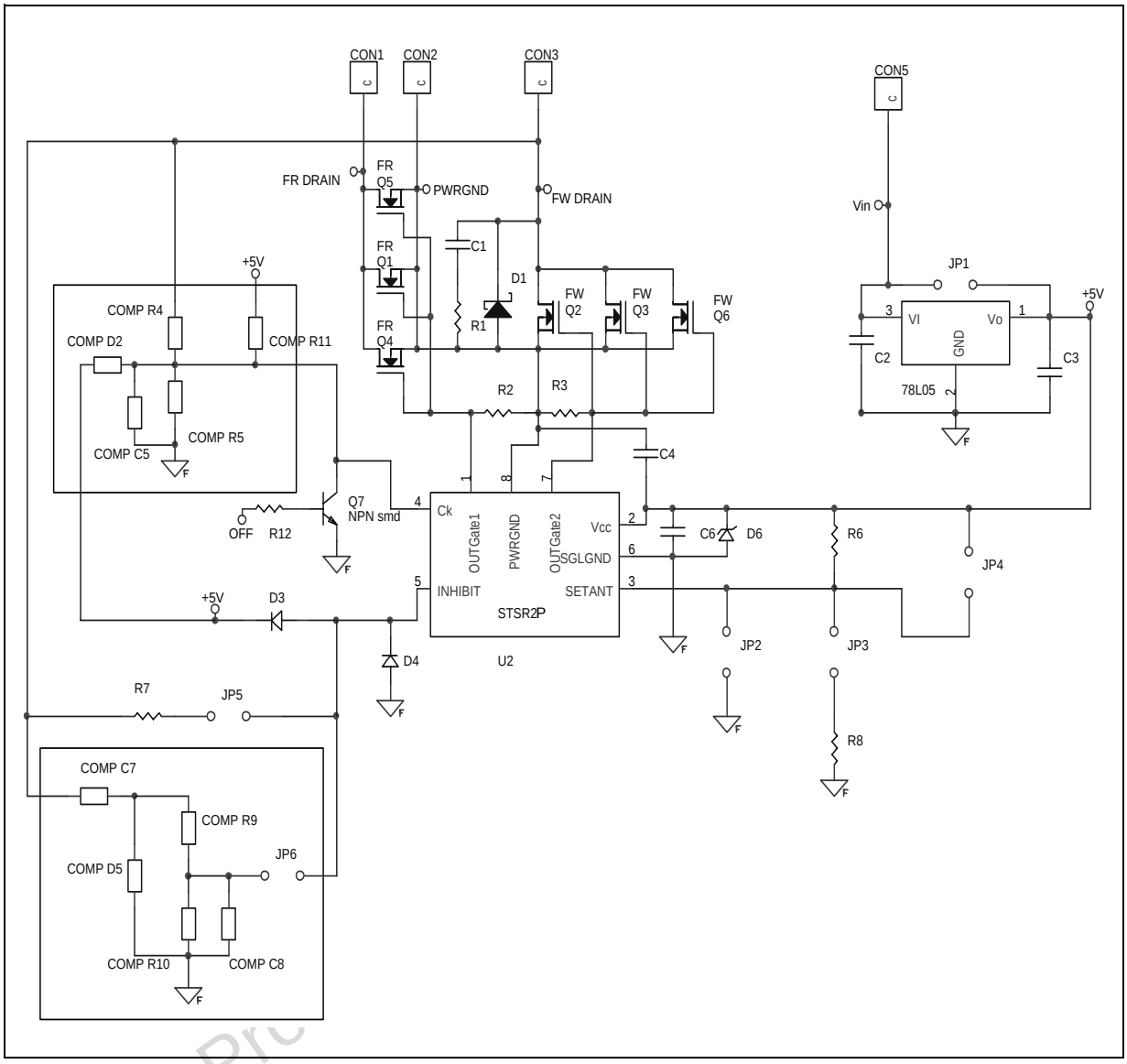


Table 3: Board Components

Component	Note
Supply	
C4, C6	Vcc bypass capacitors (typ: 100nF)
U1	Standard voltage regulator to provide 5V supply voltage (SOT89). Omit this component and close jumper JP1 if +5V is available externally.
C2	78L05 input capacitor (typ: 330nF)
C3	78L05 output capacitor (typ: 100nF)
D6	Zener diode 5.6V
JP1	Close this jumper if a +5V is is available externally

Synchronization		
Q7	Npn Transistor to turn off the device	
R12	Base resistor for Q2	
	Resistor Divider (Fig.6)	**Pull-up resistor (Fig. 7)**
Comp D2	Small signal diode: protects Ck pin from voltages higher than Vcc	Resistor: Pull-up resistor
Comp C5	Capacitor: to acts like an RC filter to eliminate the turn-off voltage spike	Not mounted
Comp R5	Resistor: low side partition resistor	Not mounted
Comp R4	Resistor: high side partition resistor	Diode: small signal diode puts Ck pin to low level when free-wheeling FET is conducting
Comp R11	Not mounted	Not mounted
INHIBIT		
R7	Limits the current flowing into INHIBIT pin when FW Drain voltage is higher than Vcc	
JP5	Close to operate in discontinuous mode condition	
JP6	Close to provide constant negative voltage to Inhibit	
	Blanking Time (Fig.12)	**Disabling (Fig.14)**
Comp C7	Capacitor: Provides the negative voltage to determine the blanking voltage	Small signal diode: blocks the positive voltage on Inhibit pin
Comp D5	Resistor: together with C7 determines the time and voltage value of the blanking circuit	Not mounted
Comp R9	Diode + resistor in series: diode blocks the positive voltage; resistor adds the negative voltage to the Inhibit pin	Resistor: Set the time constant to charge capacitor C8
Comp R10	Not mounted	Not mounted
Comp C8	Not mounted	Capacitor: Filter capacitor to keep constant the voltage on Inhibit
Anticipation		
R6, R8	Resistor divider which provides voltage level to set Anticipation time	
JP4	Sets the maximum anticipation time	
JP3	Sets the medium anticipation time	
JP2	Sets the minimum anticipation time	

Power Section	
Q1-Q5-Q4	Forward Synchronous Mosfets
Q2-Q3-Q6	Freewheeling Synchronous Mosfet
R2, R3	Gate pull down resistors
D1	A Schottky Rectifier in parallel to freewheeling mosfet can increase converter efficiency
C1, R1	A snubber reduces freewheeling turn-off spike

12. BOARD LAYOUT

Any Switch Mode Power Supply requires a good PCB (Printed Circuit Board) design layout in order to achieve maximum performance in terms of system functionality and emitted radiations. Components placing, traces routing and width are the major issues.

Some fundamental rules will be given so that the PCB designer can produce a good layout.

All traces carrying current should be drawn on the PCB as short and thick as possible. This should be done to minimize resistive and inductive parasitic effects, gaining in system efficiency and radiated emissions.

Current return routing is another crucial issue. Signal ground (SGLGND) and power ground (PWRGND) must be routed separately and connected to a single ground point.

The INHIBIT pin, due to the -25mV comparator could be sensitive to layout, so make the INHIBIT connection as short as possible.

As a rule of thumb, traces carrying signal currents should be placed far from traces carrying pulsed currents or quickly swinging voltages avoiding any coupling effect between them.

Figure 21a: Board Layout - Top Components

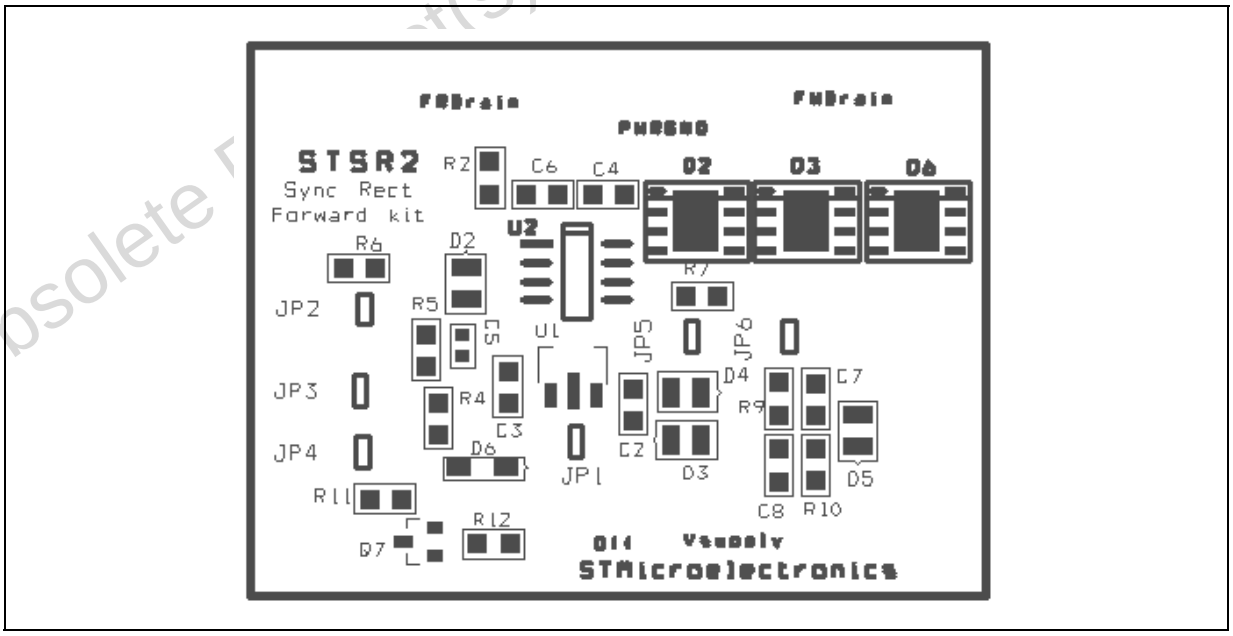


Figure 21b: Board Layout - Top Tracks

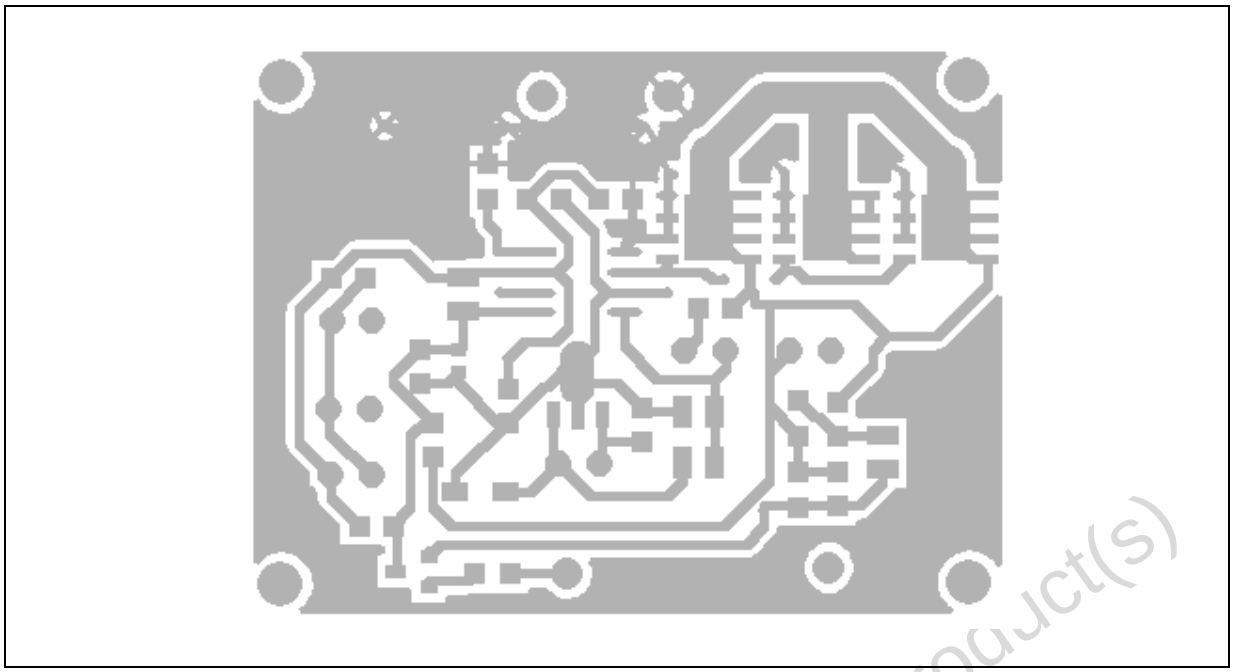


Figure 21c: Board Layout - Bottom Components

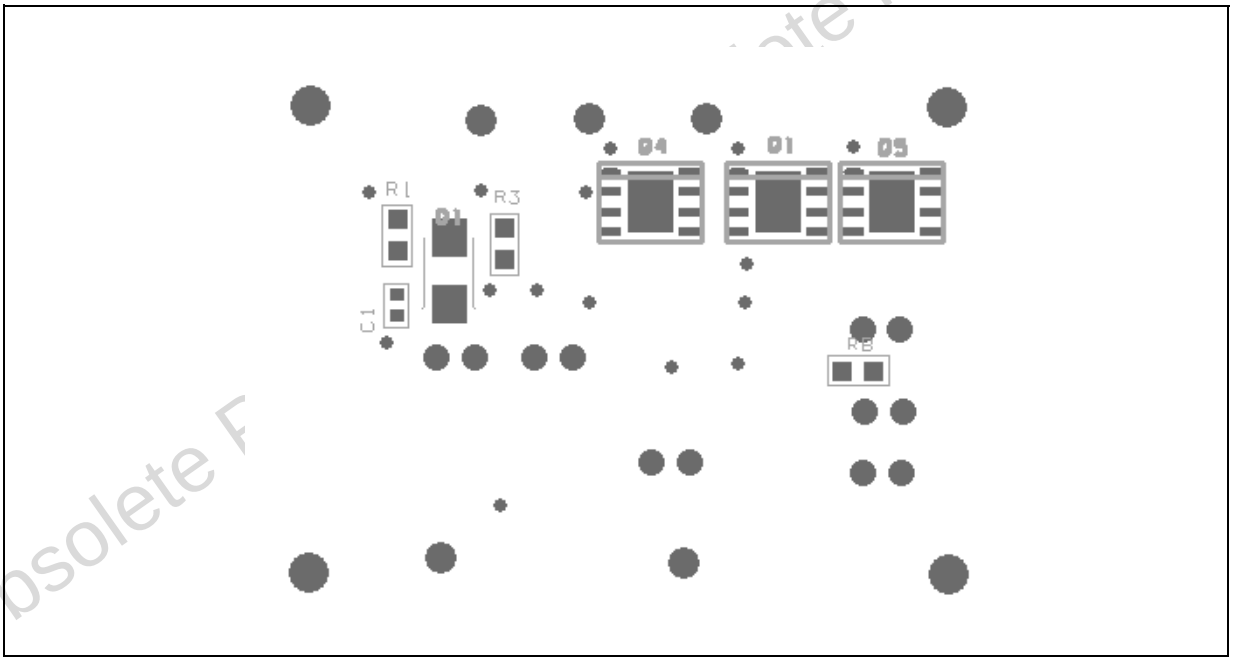
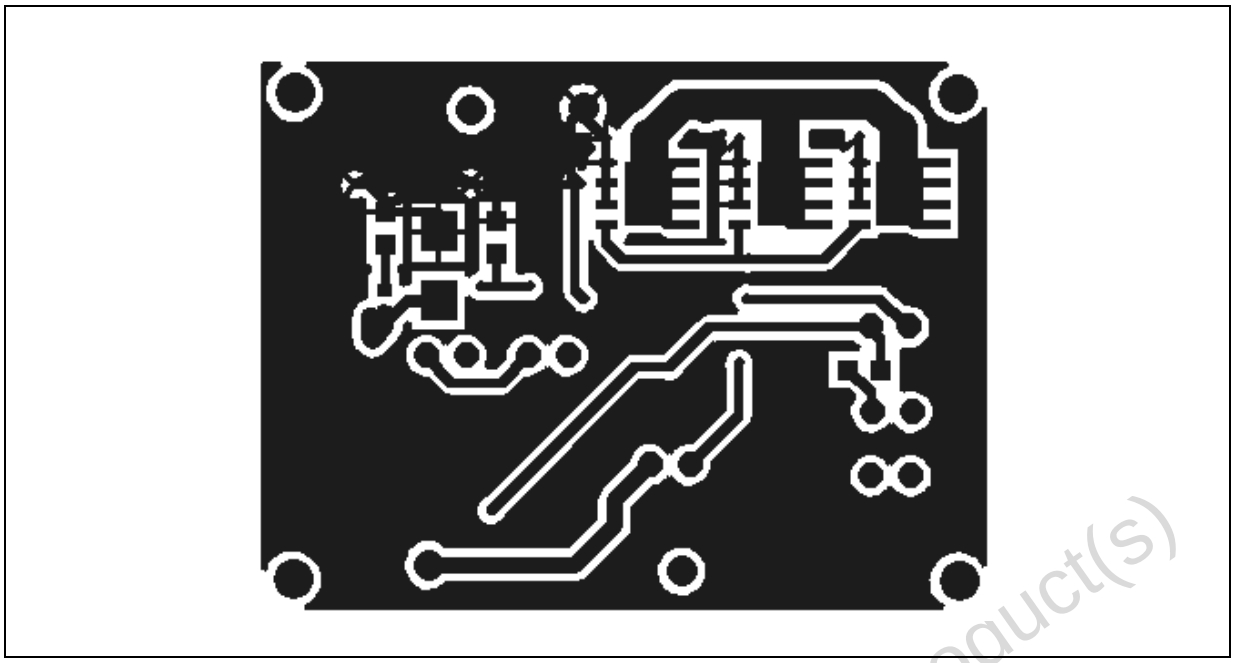


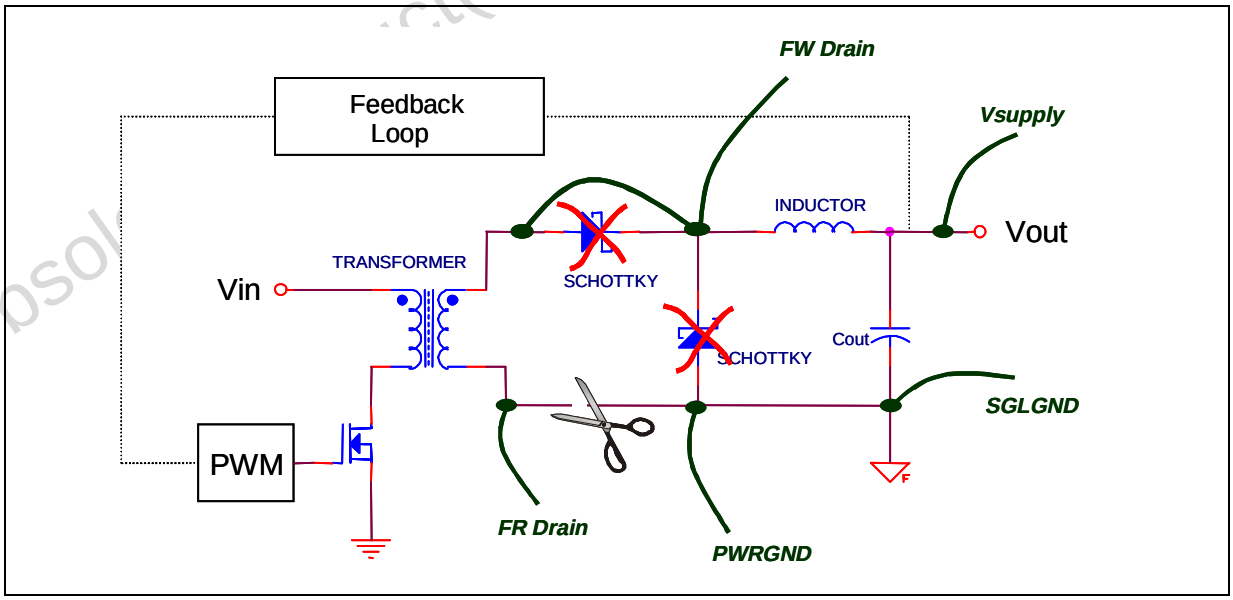
Figure 21d: Board Layout - Bottom Tracks



13. HOW TO USE THE BOARD

The demo board is meant to implement synchronous rectification in a Forward converter. If diodes are mounted on the board, they must be removed. Connect the Demo Board as depicted in figure 22. If Vout is equal or higher than 5V connect Vsupply to Vout (as in the figure). If Vout is lower than 5V, connect Vsupply together with FW Drain. This last configuration is preferable because, even during short circuit conditions, the device drives the two mosfets avoiding body diode conduction and consequently excessive power dissipation.

Figure 22: Connecting the Board to a Forward Converter



15. CONCLUSION

A new device for controlling synchronous rectifiers in high efficiency AC/DC and DC/DC Forward Converters is presented. The device is completely transparent to the primary PWM controller, and it works in the secondary side requiring no interaction with the primary side. The device is able to operate with any kind of topological configuration providing the correct driving signal for the two MOSFETs.
The presented board allows implementation of synchronous rectification in any existing forward converter in an easy and effective way.