AN4121
Application note

Poly-phase demonstration kit with the STPMC1 and STPMS2

Introduction

This application note describes the poly-phase demonstration kit with the STPMC1 and STPMS2.

The STPMC1 is a metering ASSP implemented in an advanced 0.35 µm BCD6 technology.

The STPMC1 device works as an energy calculator in power line systems utilizing a Rogowski coil, current transformer, shunt or Hall current sensors. Used in combination with one or more STPMS2 ICs, it implements all the functions needed in a 1-, 2- or 3-phase energy meter, providing effective measurement of active and reactive energies, V_{RMS}, I_{RMS}, instantaneous voltage and current per phase in 1-, 2- or 3-phase wye and delta services, from 2 to 4 wires.

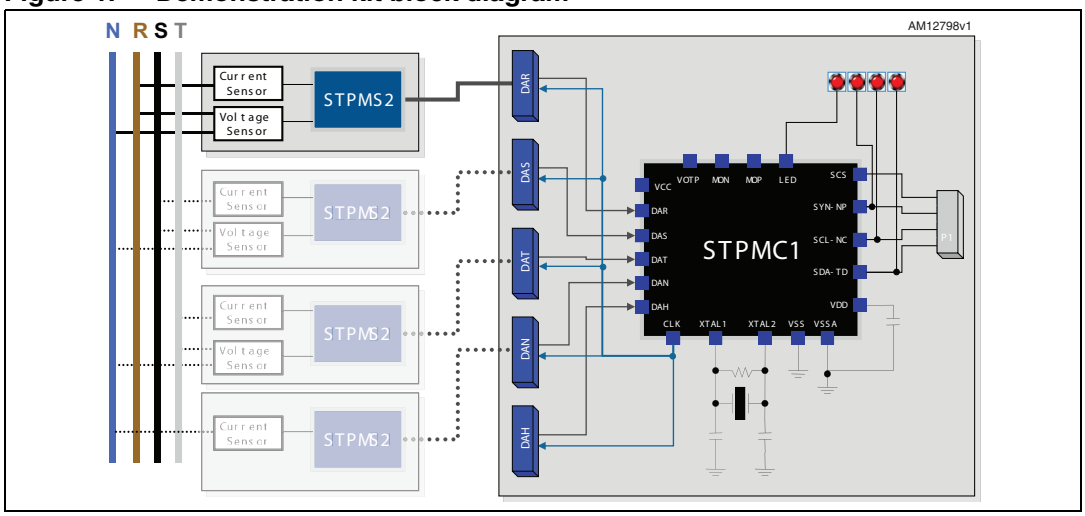
In a standalone configuration, the STPMC1 outputs a pulse train signal having a frequency proportional to the cumulative active power, and it can directly drive a stepper motor, therefore implementing a simple active energy meter.

This device can also be coupled with a microprocessor for multifunction energy meters. In this case, measured data are read at a fixed time interval from the device internal registers by the microcontroller through an SPI interface.

The STPMS2 is an ASSP designed to be the building block for single or multiphase energy meters. It consists of a preamplifier and two 2nd order $\Delta\Sigma$ modulators, band-gap voltage reference, a low-drop voltage regulator and DC buffers in its analog section and clock generator and output multiplexer in its digital section.

The demonstration kit is made up of a main board with the STPMC1 onboard (STEVAL-IPE0010V1), and it can be coupled with up to 5 daughterboards, each having an STPMS2 onboard to sense the voltage and current of each phase (STEVAL-IPE0014V1).

Figure 1. Demonstration kit block diagram



Contents

1 Application description

Poly-phase systems, and particularly three-phase meters, are most commonly used in practical industrial applications, and in a few cases also for domestic use.

The purpose of the STEVAL-IPE0010V1 + STEVAL-IPE0014V1 is STPMC1 and STPMS2 device demonstration but it can also be used as a starting point to design a Class 0.2 accuracy meter for power line systems from 2- to 4-wire delta or wye service.

Each phase is monitored from an independent daughterboard, in which an autonomous power supply provides the supply to the board itself and, once it is connected, also to the motherboard.

In this board, the STPMS2 device senses the phase current through a CT sensor, and the phase voltage through a voltage divider. The presence of a dedicated network reduces, for a large amount, the sampling (aliasing) noise, therefore increasing the meter precision. The STPMS2 outputs a sigma-delta stream sent, together with supply voltage, to the STPMC1 through a card edge connector.

The motherboard receives from the daughterboards the sigma-delta streams that are further elaborated by the STPMC1. This device, from a 4.194 MHz crystal oscillator, provides a common clock with programmable frequency to all the daughterboards.

The motherboard, through a 10-pin flat cable connector (P1 in *Figure 2*), can be interfaced to a microprocessor board to implement advanced metering features (multi-tariff, data management and storage, communication…). It also has stepper motor connectors for a simple energy meter implementation (W2, W5 in *Figure 2*).

The STPMC1 board can also be interfaced to a dedicated GUI through the STPMxx parallel programmer/reader released with the application.

Table 1. Operating conditions

Condition	Value	Unit
V_{NOM}	230	V_{RMS}
I_{NOM}	CT: I_{NOM} = 1	A_{RMS}
I_{MAX}	CT: I_{MAX} = 30	A_{RMS}
f_{LIN}	50/60 ± 10%	Hz
T_{OP}	- 40 / + 85	°C

2 Circuit description

2.1 Motherboard circuit

The motherboard consists of the following sections:

- STPMC1 circuitry
- Connectors.

The schematic of the board is shown in *Figure 2* and in *Figure 3*.

Figure 2. STPMC1 circuitry schematics

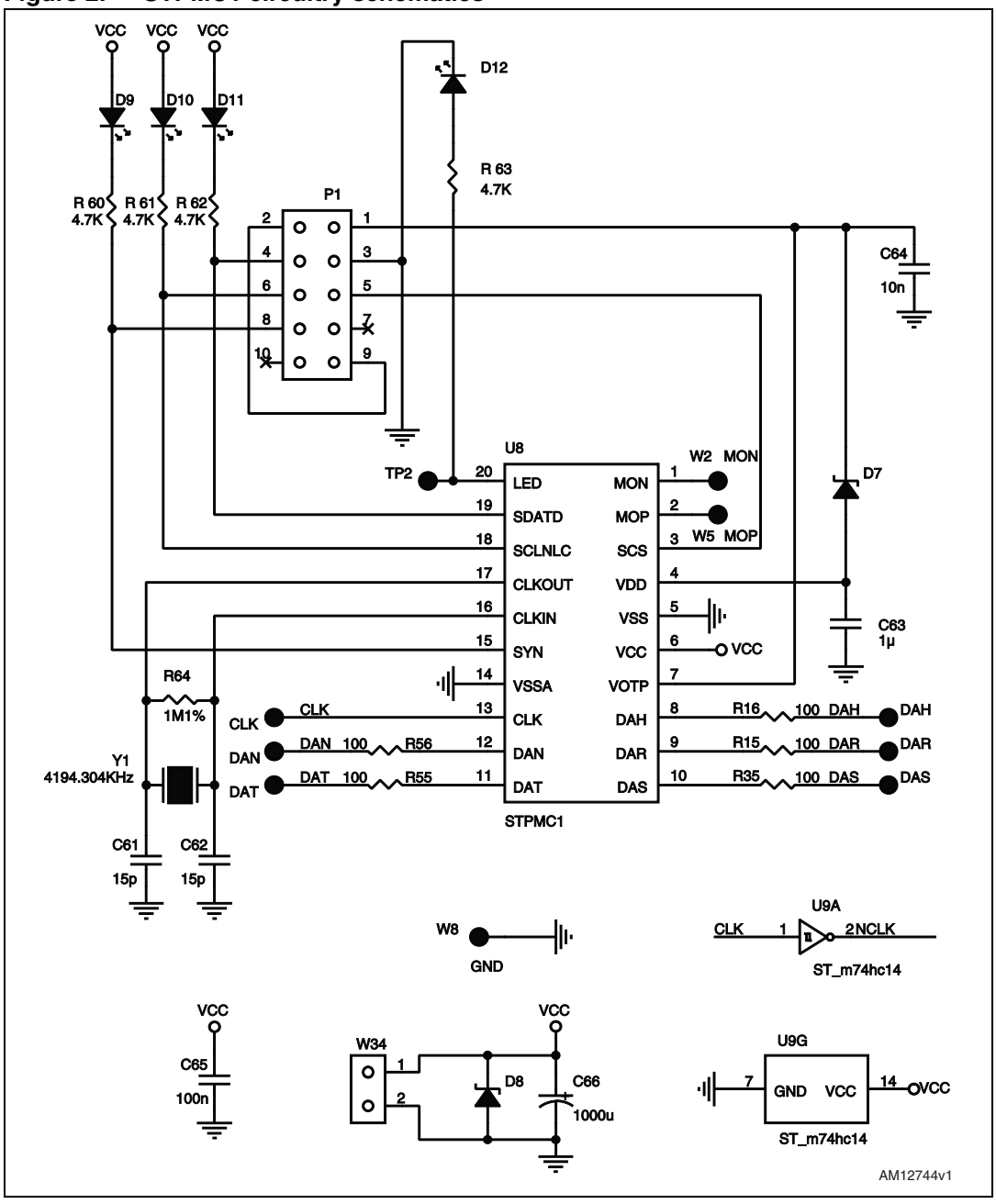
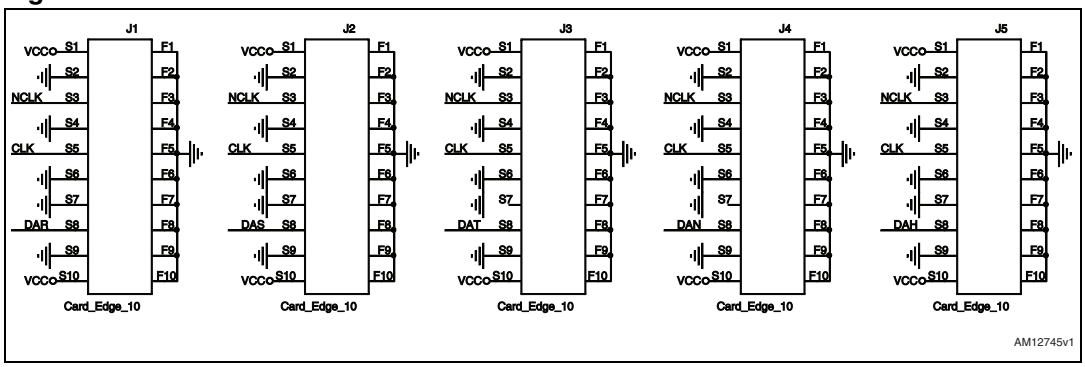


Figure 3. Motherboard connectors schematics



2.2 Daughterboard circuit

This section explains the implementation of each phase network which performs the power measurement.

The schematic can be divided into the following subsets:

- Current sensing circuit (1) or (2)
- Anti-aliasing filter (3)
- Voltage sensing circuit (4).

2.2.1 Current sensing circuit

The STPMS2 has an external current sensing circuit using either a current transformer, in which a burden resistor is used to produce a voltage between CIN and CIP proportional to the current measured, or a shunt resistor, or a Rogowski coil current sensor.

2.2.2 Anti-aliasing filter

The anti-aliasing filter is a low-pass filter. It has a negligible influence on the voltage drop between CIN and CIP, VIN and VIP; its aim is to reduce the distortion caused by the sampling, also called aliasing, by removing the out-of-band frequencies of the input signal before sampling it with the analog-to-digital converter.

Filtering is easily implemented with a resistor-capacitor (RC) single-pole circuit which obtains an attenuation of - 20 dB/dec.

2.2.3 Voltage sensing circuit

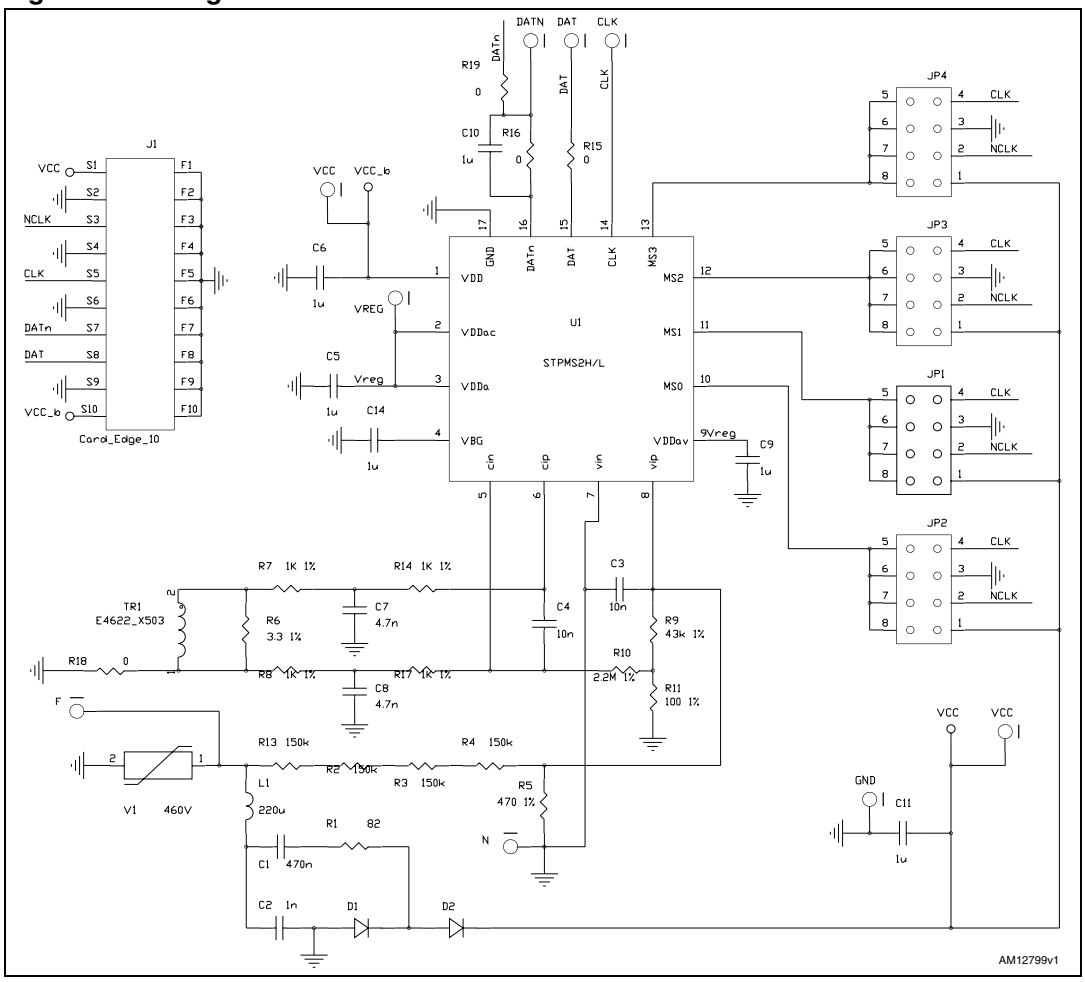
A resistor divider is used as voltage sensor.

The 660 kΩ resistor is separated into four, 2 x 150 kΩ and 2 x 180 kΩ, in-series resistors, which ensure that a high voltage transient does not bypass the resistor. This also reduces the potential across the resistors, thereby decreasing the possibility of arcing. The following resistors are used to implement resistor divider:

- R = R13 + R2 + R3 + R4 = 660 kΩ
- R5 = 470 Ω.

Inductance L1 and capacitor C2 create a filter which prevents electromagnetic interference (EMI).

Figure 4. Daughterboard circuit schematic



2.2.4 Jumper settings

The onboard jumpers JP1 to JP4 allow the setting of the STPMS2 device according to *Table 2*, *Table 3*, *Table 4* and *Table 5* below.

Table 2. Precision mode and input amplifier gain selection

JP1	MS0	Description
1	GND	LPR, amplifier GAIN selection g3 = 32
2 (1)	CLK	LPR, amplifier GAIN selection g0 = 4
3	NCLK	HPR, amplifier GAIN selection g0 = 4
4	VDD	HPR, amplifier GAIN selection g3 = 32

1. Default value.

Table 3. TC of the band-gap reference

JP2	MS1	Description
1	GND	TC = 60 ppm/°C
2 (1)	CLK	Flattest TC = +30 ppm/°C
3	NCLK	TC = +160 ppm/°C
4	VDD	TC = -160 ppm/°C

1. Default value.

Table 4. Control of voltage channel and output signals

JP3	MS2	Description
1 (1)	GND	Voltage channel ON, DATn = ~(DAT =(CLK) ? bsV : bsC)
2	CLK	Voltage channel OFF, DATn = bsCn, DAT = bsC
3	NCLK	Voltage channel OFF, DATn = bsCn, DAT = bsC
4	VDD	Voltage channel ON, DATn = bsC, DAT = bsV

1. Default value.

Table 5. Changing of band-gap voltage reference

JP4	MS3	Description
1 (1)	GND	Hard mode, BIST mode OFF
2	CLK	Soft mode
3	NCLK	Reserved
4	VDD	Hard mode, BIST mode ON

1. Default value.

For further details on device configuration, please refer to its datasheet.

2.3 Clock management network

A 4.194 MHz quartz is used to supply the clock to the STPMC1 device. To set this frequency, internal configuration bits MDIV and FR1 must be kept cleared.

A synchronized clock is provided to all the STPMS2 through pin CLK, whose frequency is programmable through bit HSA to 1.049 MHz or 2.097 MHz.

2.4 Communication with microprocessor

A control board with embedded microprocessor may be connected to connector P1 using 10-wire flat cable. *Table 5* below describes the pinout of the connector.

The STPMC1 has an SPI communication port implemented by four multipurpose pins (SCS, SYN-NP, SDA-TD, SCL-NLC).

In standalone operating mode these multipurpose pins output:

- negative power direction on SYN-NP pin;
- tamper condition detected on SDA-TD pin;
- no load condition detected on SCL-NLC pin.

For this reason these pins are connected to the three LEDs, D9, D10 and D11.

In this configuration, the LED pin outputs a pulse train with frequency proportional to the three-phase power and it is connected to LED D12.

When configured in peripheral operating mode, the SPI port is enabled and some microcontroller based applications can either read internal data records or write the mode and configuration signals by means of dedicated protocol, or reset the device.

By default, the STPMC1 is configured in peripheral mode (configuration bits APL=0).

This also implies the following output settings:

- watchdog reset signal on MON pin;
- zero-crossing (ZCR) on MOP pin;
- programmable energy pulsed output on LED pin.

For further information on STPMC1 programmable bit settings, please refer to the datasheet.

The STPMC1 SPI protocol is explained in detail in a related application note.

Table 6. P1 connector pin description

Pin	Pin name	Functional description
1.	VOTP	Power supply input of +15.0 V during permanent write to OTP cells
2.	---	Not connected
3.	GND	Signal reference level 0 V and power supply return
4.	SDA-TD	SPI interface data
5.	SCS	SPI interface enable
6.	SCL-NLC	SPI interface clock
7.	---	Not connected
8.	SYN-NP	SPI interface signal
9.	---	Not connected
10.	VCC	Power-out of +3.3 or 5 V

Connector P1 is also used in the demonstration phase to connect the measurement module to a PC through the STPM parallel programmer/reader hardware interface.

This allows the user to set temporary and/or permanently the internal STPMC1 registers using a dedicated GUI.

The VOTP pin on the connector P1 is used when a host wants to permanently write some configuration bits in the STPMC1 device. In this case, a +15 V power level must be present on the VOTP. This level must be delivered from the host itself because the module does not have an onboard charge pump.

3 Board layout

3.1 Layout rules for three-phase systems design

Noise rejection is the main issue to work on when a three phase multi-chip approach has been chosen. In this case layout plays a crucial role.

Here are some rules to follow in the layout phase of three-phase systems:

- Component positioning

The components of the measuring section (STPMS2, current sensor, passive components) should be placed using the same layout for each phase. The phases should be placed in a symmetrical scheme. In this way a reduction of the cross talking can be achieved.

The current sensor should be placed very close to the corresponding STPMS2 to minimize the captured noise.

- Component routing

The passive components belonging to the analog input channels must be placed between the sensor and the STPMS2, always respecting a symmetrical scheme.

- Quartz

The crystal network must be placed close to the STPMC1, and a completely symmetrical path from the CLK pin of the STPMC1 to STPMS2 devices must be ensured. A copper plate has been adopted under the crystal both on the TOP and on the BOTTOM side of the PCB.

- Grounding

The STPMS2 device must be grounded by the exposed pad and by pin VSS, ensuring the maximum stability of ground plane by placing vias between the top and bottom ground plane. Analog and digital ground must be separated.

3.2 Motherboard layout

Figure 5. Motherboard top layout

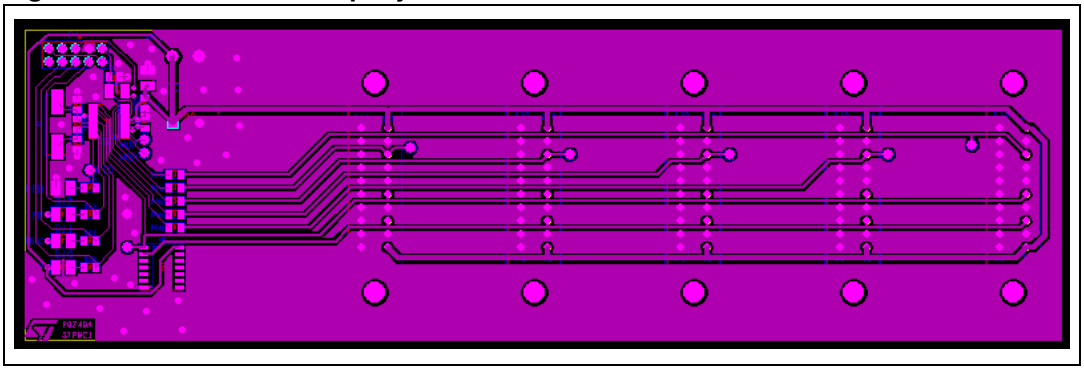
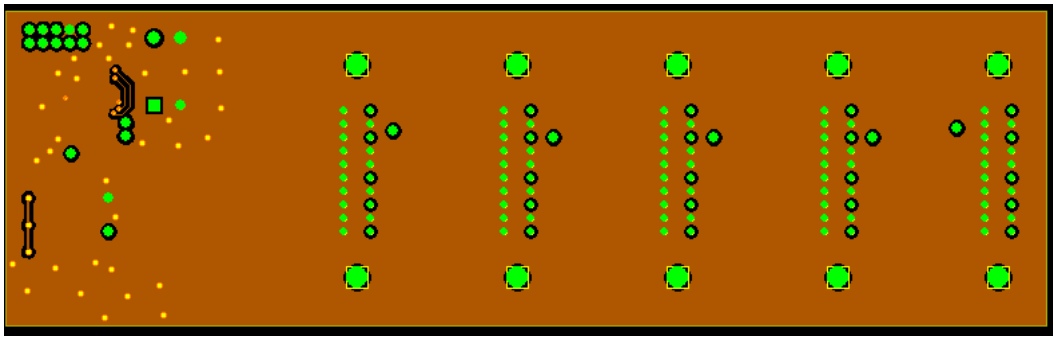


Figure 6. Motherboard bottom layout



3.3 Daughterboard layout

Figure 7. Daughterboard top layout

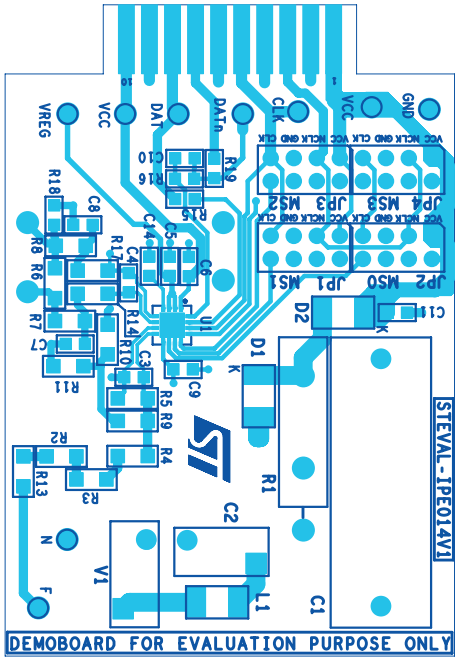
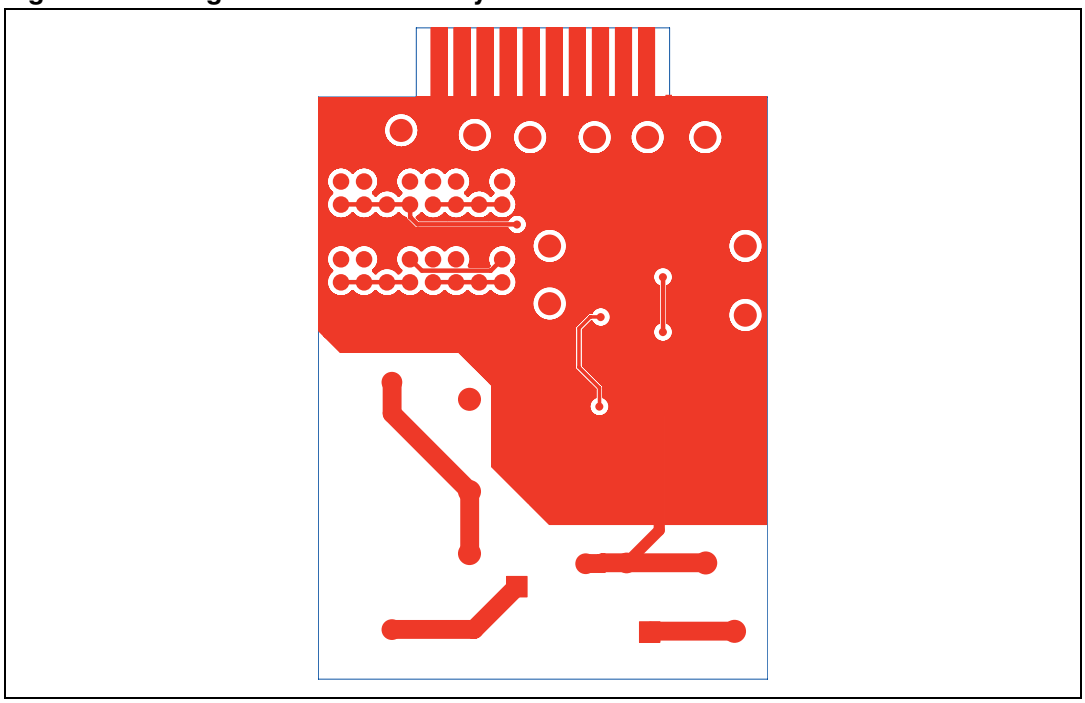


Figure 8. Daughterboard bottom layout



4 Experimental results

The tests have been conducted on a three-phase metering demonstration board with the STPMC1 and three STPMS2Ls considering I_{NOM} = 5 A, V_{NOM} = 230 V, f_{line} = 50 Hz.

Results are referred to the full scale dynamic range of the current channel (“FS” in *Table 7*), which for the sensor selected was ± 37.5%, or as percentage of I_{NOM}.

4.1 Three-phase energy measurement accuracy

4.1.1 Test with symmetrical voltages and balanced load at PF = 1

This three-phase energy measurement has been performed in the following conditions:

$V_R = V_S = V_T = 230\ [V_{RMS}]$

$I_R = I_S = I_T = I\ [A_{RMS}]$

$P_F = 1$

Table 7. Three-phase energy measurement

I [A]	% of I_{NOM} [%]	% of FS [%]	error [%]
22,5	450%	100%	0,097%
16	320%	71%	0,076%
12	240%	53%	0,040%
10	200%	45%	0,035%
8	160%	36%	-0,008%
5	100%	22%	0,027%
2	40%	9%	0,035%
1	20%	4%	-0,065%
0,5	10%	2%	-0,087%
0,25	5%	1%	-0,096%
0,1	2%	0,4%	-0,087%
0,05	1%	0,2%	-0,096%
0,025	0,5%	0,1%	-0,096%
0,01	0,2%	0,04%	-0,352%
0,005	0,1%	0,02%	-0,435%
0,0025	0,05%	0,01%	-0,487%

Figure 9. Graph of experimental results of three-phase energy measurements

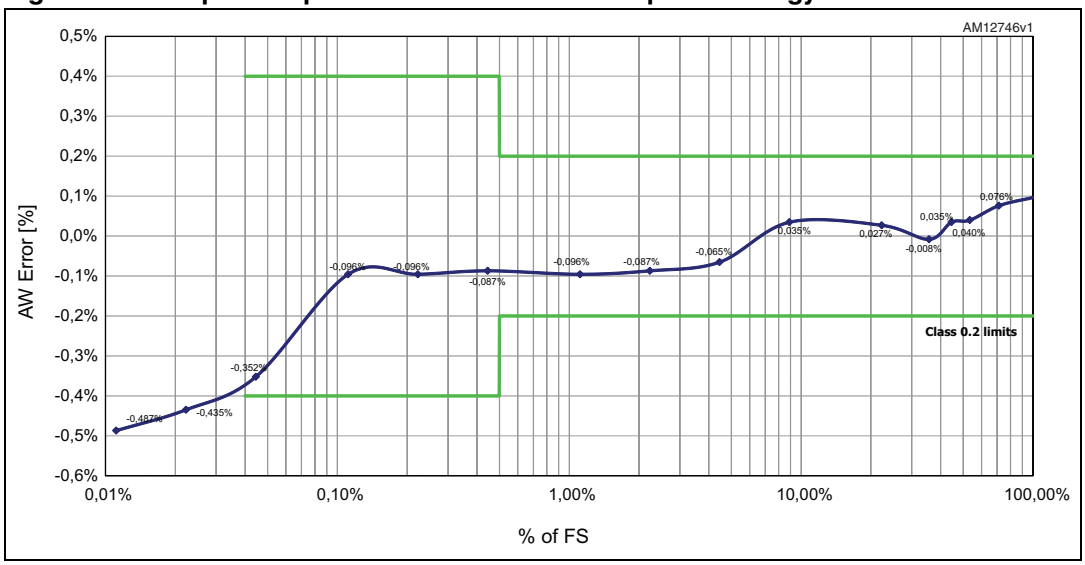


Table 8. Limits for class 0,2 meters: poly-phase meters with symmetrical voltages and balanced loads at PF = 1

I [A]	% of I_{NOM} [%]	error [%]
I_{MAX}	-	± 0,2%
In	100%	± 0,2%
0,05*In	5%	± 0,2%
0,0499*In	4,99%	± 0,4%
0,01*In	1%	± 0,4%

4.1.2 Test with symmetrical voltages and balanced load at PF = 0.5 inductive and PF = 0.8 capacitive

This three-phase energy measurement has been performed in the following conditions:

$V_R = V_S = V_T = 230$ [V_{RMS}]

$I_R = I_S = I_T = I$ [A_{RMS}]

PF = 0.5 ind

PF = 0.8 cap

Table 9. Three-phase energy measurement - PF = 0.5 ind

I [A]	% of I_{NOM} [%]	% of FS [%]	error [%]
12	240%	53%	-0,1932%
10	200%	45%	-0,1449%
8	160%	36%	-0,1087%
5	100%	22%	-0,1484%
2	40%	9%	-0,0971%
1	20%	4%	-0,1507%
0,5	10%	2%	-0,0928%
0,25	5%	1%	-0,0348%
0,1	2%	0,4%	-0,1739%
0,05	1%	0,2%	0,0174%

Table 10. Three-phase energy measurement - PF = 0.8 cap

I [A]	% of I_{NOM} [%]	% of FS [%]	error [%]
12	240%	53%	0,0393%
10	200%	45%	0,0525%
8	160%	36%	0,0861%
5	100%	22%	0,0362%
2	40%	9%	0,0634%
1	20%	4%	0,0435%
0,5	10%	2%	0,0362%
0,25	5%	1%	0,0652%
0,1	2%	0,4%	0,0725%
0,05	1%	0,2%	0,1812%

Figure 10. Graph of experimental results of three-phase energy measurement

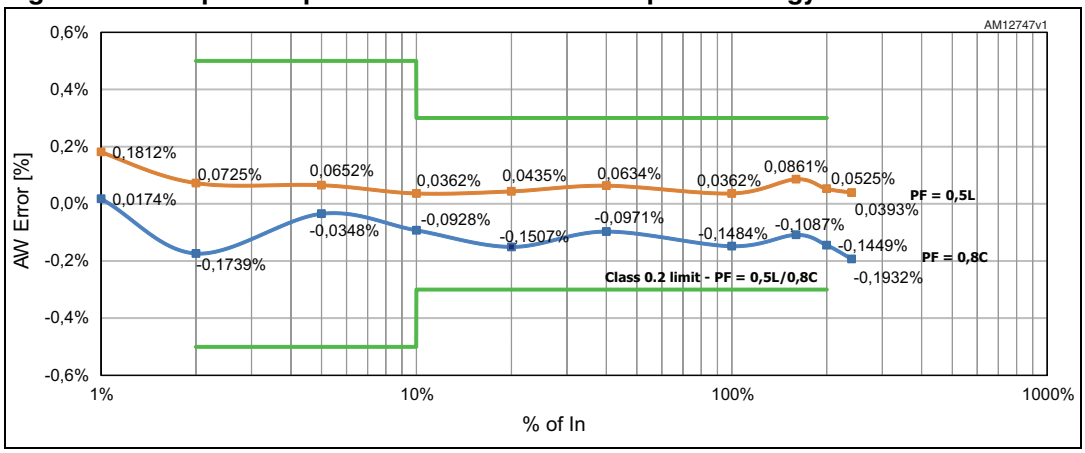


Table 11. Limits for class 0,2 meters: poly-phase meters with symmetrical voltages and balanced loads at PF = 0,5 ind or 0,8 cap

I [A]	% of I_{NOM} [%]	error [%]
I_{MAX}	-	± 0,3%
In	100%	± 0,3%
0,1*In	10%	± 0,3%
0,099*In	9,9%	± 0,5%
0,02*In	5%	± 0,5%

4.2 Typical phase energy measurement accuracy

4.2.1 Test with symmetrical voltages and only one phase load at PF = 1 and PF = 0,5 inductive

This single-phase energy measurement has been performed in the following conditions:

$V_R = V_S = V_T = 230$ [V_{RMS}]

$I_R = I$ [A_{RMS}]

$I_S = I_T = 0$

PF = 1

PF = 0.5 ind

Table 12. Phase energy measurement

I [A]	% of In [%]	error [%]
10	200%	-0,0003%
8	160%	-0,0212%
5	100%	-0,0426%
2	40%	0,1152%
1	20%	-0,0309%
0,5	10%	-0,0348%
0,2	4%	0,1196%

Table 13. Phase energy measurement PF = 0.5 inductive

I [A]	% of In [%]	error [%]
10	200%	-0,2348%
8	160%	-0,2565%
5	100%	-0,2504%
2	40%	-0,1870%
1	20%	-0,2087%
0,5	10%	-0,1217%
0,2	4%	0,0130%

Figure 11. Graph of experimental results of one phase energy measurement

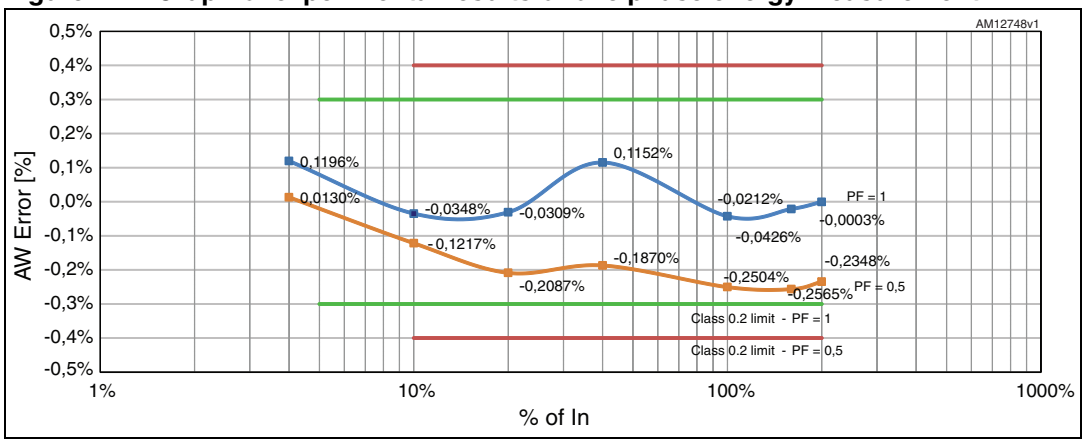


Table 14. Limits for class 0,2 meters: poly-phase meters with symmetrical voltages and only one phase load at PF = 1

I [A]	% of In [%]	error [%]
I_{MAX}	1000%	± 0,3%
0,05*In	5%	± 0,3%

Table 15. Limits for class 0,2 meters: poly-phase meters with symmetrical voltages and only one phase load at PF = 0.5 ind

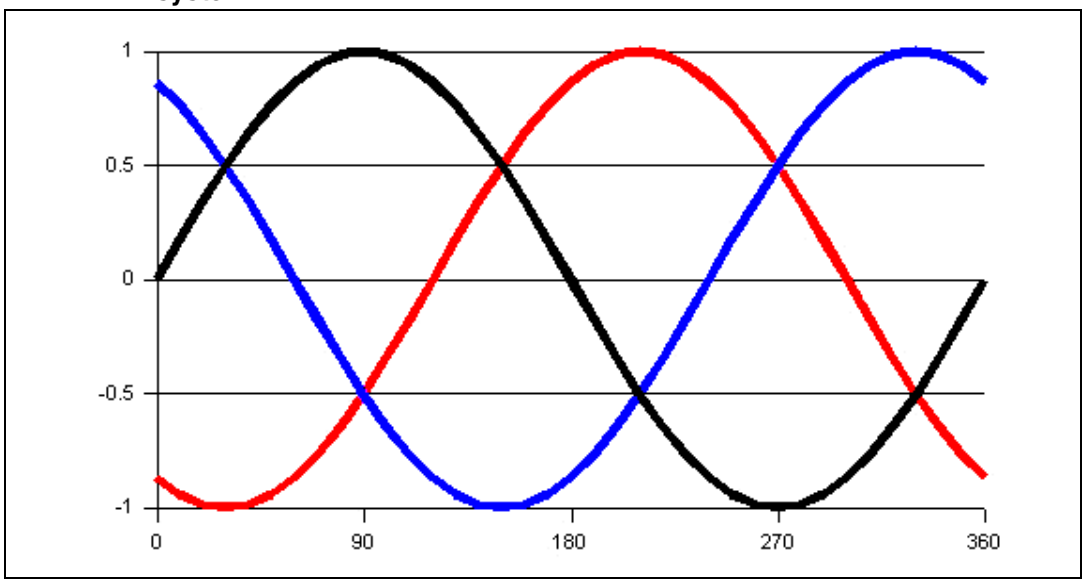
I [A]	% of In [%]	error [%]
I_{MAX}	1000%	± 0,4%
0,1*In	10%	± 0,4%

Appendix A Three-phase systems

Three-phase is a common method of electric power transmission. It is a type of poly-phase system used to power motors and many other devices.

The currents are sinusoidal functions of time, all at the same frequency but with different phases. In a three-phase system the phases are spaced equally, giving a phase separation of 120°. The frequency is typically 50 Hz in Europe and 60 Hz in the US and Canada.

Figure 12. Instantaneous voltage (or current) in one voltage cycle of a three-phase system



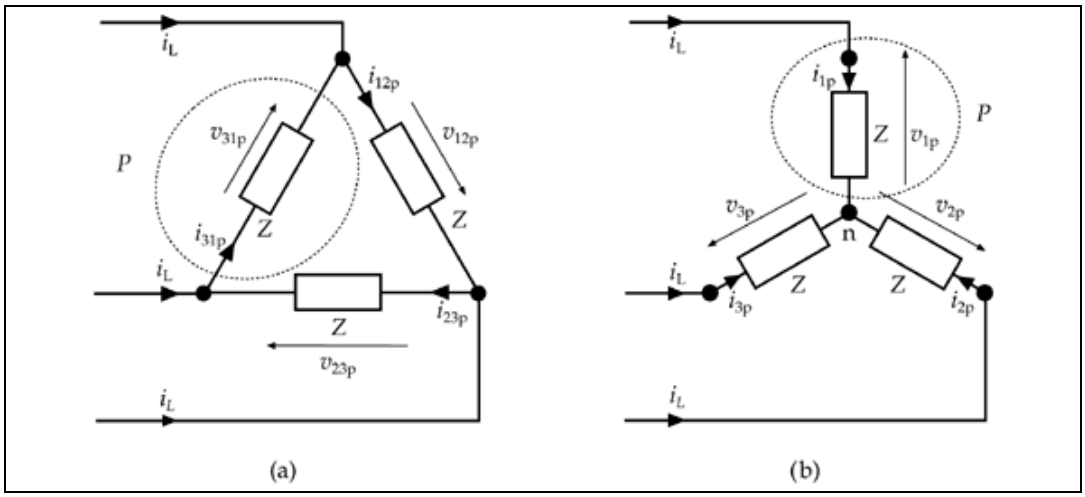
The three phases may be supplied over six wires, with two wires reserved for the exclusive use of each phase. However, they are generally supplied over three or four wires:

- Three-phase, 3-wire delta service which has no neutral and 220 V between phases
- Three-phase, 4-wire delta and wye service which has 220 V between phase-neutral and 380 V phase-phase.

A.1 Power in three-phase AC circuits

Let's assume that the angle between the phase voltage and the phase current is θ, which is equal to the angle of the load impedance. Considering the load configurations given in *Figure 14*, the phase power and the total power can be estimated easily.

Figure 13. Per-phase powers in (a) a delta-connected load and (b) wye-connected load



In the case of *Figure 13*.a, the total active power is equal to three times the power of one phase:

$$P_1 = P_2 = P_3 = P = V_{line} I_{phase} \cos\theta$$

$$P_{Total} = 3P = 3V_{line} I_{phase} \cos\theta$$

Since the line current in the balanced delta-connected loads,

$$I_{line} = \sqrt{3} I_{phase}$$

If this equation is substituted into equation 3.51, the total active load becomes:

Equation 1

$$P_{Total} = \sqrt{3} V_{line} I_{line} \cos\theta$$

In *Figure 13*.b, however, the impedances contain the line currents I_{line} (equal to the phase current, I_{phase}) and the phase voltages:

$$V_{phase} = V_{line} / \sqrt{3}$$

Therefore, the phase active power and the total active power are:

$$P_1 = P_2 = P_3 = P = V_{phase} I_{line} \cos\theta$$

$$P_{Total} = 3P = 3V_{phase} I_{line} \cos\theta$$

If the relationship between the phase voltage and the line voltage is used, the total active power becomes identical to *Equation 1* developed. This means that the total power in any balanced three-phase load (θ- or Y-connected) is given by *Equation 1*.

Similarly, the total reactive and the total apparent power in the three-phase balanced AC circuits can be given by:

$$Q_{Total} = \sqrt{3} V_{line} I_{line} \sin\theta$$

$$S_{Total} = \sqrt{3} V_{line} I_{line}$$

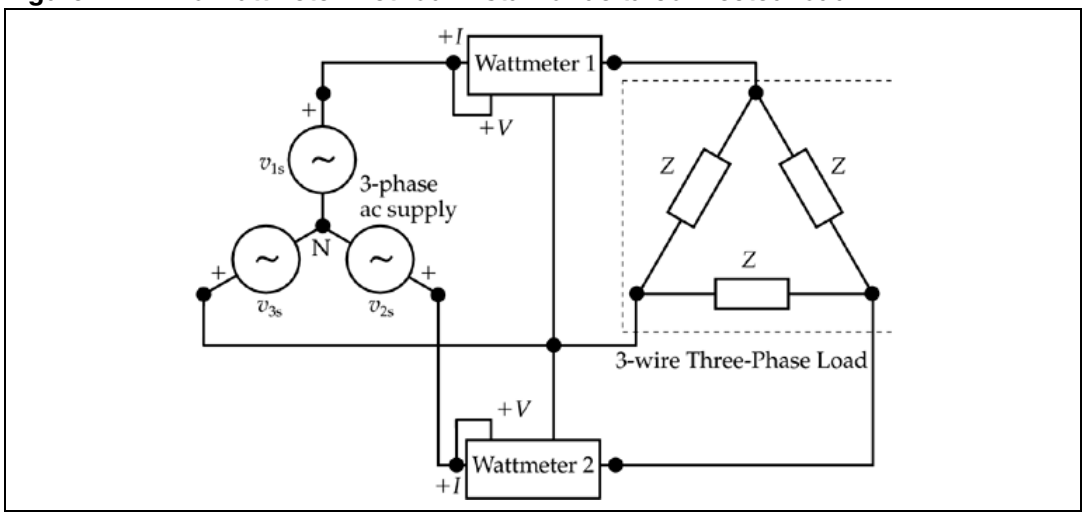
A.2 Power measurement techniques

In the three-phase power systems, one, two, or three wattmeters can be used to measure the total power. A wattmeter may be considered to be a voltmeter and an ammeter combined in the same box, which has a deflection proportional to $V_{rms} I_{rms} \cos\theta$, where θ is the angle between the voltage and current. Hence, a wattmeter has two voltage and two current terminals, which have + or θ polarity signs. Three power measurement methods utilizing the wattmeters are described next, and are applied to the balanced three-phase AC load.

A.2.1 Two-wattmeter method

This method can be used in a three-phase 3-wire balanced or unbalanced load system that may be connected θ or Y. To perform the measurement, two wattmeters are connected as shown in *Figure 14*.

Figure 14. Two-wattmeter method in star- or delta-connected load



In the balanced loads, the sum of the two wattmeter readings gives the total power. This can be proven in a star-connected load mathematically using the power reading of each meter as:

$$P_1 = V_{12}I_1\cos(30° + \theta) = V_{line}I_{line}\cos(30° + \theta)$$

$$P_2 = V_{32}I_3\cos(30° - \theta) = V_{line}I_{line}\cos(30° - \theta)$$

$$P_{Total} = P_1 + P_2 = \sqrt{3}V_{line}I_{line}\cos\theta$$

If the difference of the readings is computed,

$$P_2 - P_1 = V_{line}I_{line}\cos(30° - \theta) - V_{line}I_{line}\cos(30° + \theta) = V_{line}I_{line}\sin\theta$$

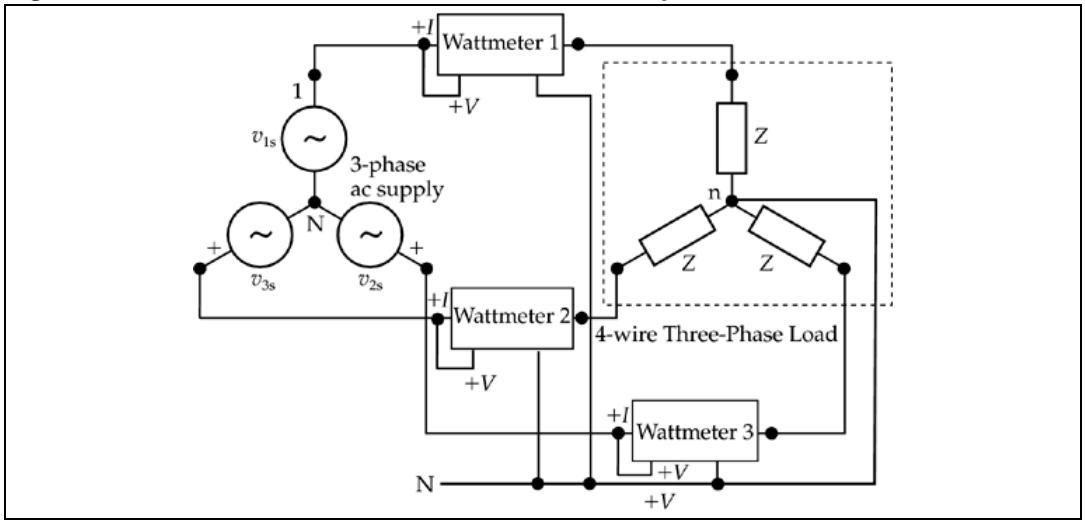
which is $1/\sqrt{3}$ times the total three-phase reactive power. This means that the two-wattmeter method can also indicate the total reactive power in the three-phase loads and also the power factor.

A.2.2 Three-wattmeter method

This method is used in a three-phase four-wire balanced or unbalanced load. The connections are made with one meter in each line as shown in *Figure 15*. In this configuration, the total active power supplied to the load is equal to the sum of the three wattmeter readings.

$$P_{Total} = P_1 + P_2 + P_3$$

Figure 15. The wattmeter connections in the three-phase 4-wire loads



A.2.3 One-wattmeter method

This method is suitable only in three-phase 4-wire balanced loads. The connection of the wattmeter is similar to the drawing given in *Figure 15*. The total power is equal to three times the reading of only one wattmeter that is connected between one phase and the neutral.

Appendix B BOM list

Table 16. Motherboard BOM list

Item	Quantity	Reference	Part	PCB footprint	Description
1	2	C61,C62	15 p	sm_0805	
2	1	C63	1 µ	sm_0805	
3	1	C64	10 n	sm_0805	
4	1	C65	100 n	sm_0805	
5	1	C66	1000 µ	cpcyl1_d500_ls200_040	CAPACITOR AL-RILL 13x22/2M*1000my 25 V
6	2	D7	Diode	sm_d_1206	DIODE PLANAR 1N4148 SOD323*75 V
6	2	D8	Diode_zener	sm_d_1206	DIODE ZENER ZMM SOD 80*5.1 V (3.3 V) G
7	4	D9, D10, D11, D12	Diode_led	PLCC2	SMD LED low current super red P-LCC-2 OSRAM (Distrelec 631039)
8	5	J1, J2, J3, J4, J5	Card_Edge_10	sullins_10_drxi	
9	1	P1	Morsetti_5x2	jumper_5x2_bis	
10	5	R15, R16, R35, R55, R56	100	sm_0805	
11	4	R60, R61, R62, R63	4.7 k	sm_0805	
12	1	R64	1M 1%	sm_0805	
13	1	TP2	TP	TEST_POINT	
14	1	U8	STPMC1	sog_65m_20_w300_l260	
15	1	U9	ST_m74hc14	sog_050_14_w325_l350	
16	1	W2	MON	TEST_POINT	
17	1	W3	DAH	TEST_POINT	
18	1	W4	DAR	TEST_POINT	
19	1	W5	MOP	TEST_POINT	
20	1	W6	DAS	TEST_POINT	
21	1	W7	DAT	TEST_POINT	

Table 16. Motherboard BOM list (continued)

Item	Quantity	Reference	Part	PCB Footprint	Description
22	1	W8	GND	TEST_POINT	
23	1	W9	DAN	TEST_POINT	
24	1	W10	CLK	TEST_POINT	
25	1	W34	Morsetti_2	Morsetti_2	
26	1	Y1	4194.304 kHz	Auris_hc49ussmd	HC-49/US SMD (Distrelec 335026)

Table 17. Daughterboard BOM list

Item	Quantity	Reference	Part	PCB Footprint	Description
1	1	C1	470 n	rad_1250x425_ls1075_037	CAPACITOR X2 12x21x32/11M*470n 275 V K
2	1	C2	1 n	disc_400x200_ls300x100_037	CAPACITOR KER X1/Y2 9X5/3M*1.0N 440/330
3	1	C3	22 n	sm_0603	
4	1	C4	10 n	sm_0603	
5	6	C5, C6, C11, C14	1 µ	sm_0603	
6	1	C12, C13	100 n	sm_0603	
7	4	C7, C8, C9, C10	5 n	sm_0603	
8	2	D1, D2	Diode_rele	sm_1812	DIODE RECTIFIER SMD*600 V 1 A
9	2	JP1, JP2	Morsetti_4x2	jumper_4x2	
10	1	J1	Card_Edge_10	Card_edge_10_mirror	
11	1	L1	220 µ	sm_1812	INDUCTOR VF82423 1812*220myH 0,1 A
12	1	R1	82	rad_725x200_ls300_040	RESISTOR WIRE SFR0518 P5 2W*82R K
13	4	R2, R3, R4, R13	150 k 1%	sm_0603	
14	2	R5, R12	475 1%	sm_0603	
15	1	R6	3.4 1%	sm_0603	
16	2	R7, R8	1 k 1%	sm_0603	
17	1	R9	42.2 k 1%	sm_0603	

Table 17. Daughterboard BOM list (continued)

Item	Quantity	Reference	Part	PCB Footprint	Description
18	1	R10	2.2 M 1%	sm_0603	
19	1	R11	100 1%	sm_0603	
20	2	R14, R17	10	sm_0603	
21	2	R15 or R16, R18	0	sm_0603	
22	1	SH1	170 µ	r_shunt	
23	1	SH2	170 µ	r_shunt_2	
24	1	TR1	E4622_X503	VAC_e4622_x503	
25	1	U1	STPMS2L	mcs_manual_mlp3x3_16_05_pad	
26	1	V1	460 V	disc_450x200_ls300x100_037	VARISTOR MOKS K10*300V
27	1	W1	N	TEST_POINT	
28	1	W2	F	TEST_POINT	
29	1	W3	DAR	TEST_POINT	
30	1	W4	VREG	TEST_POINT	
31	2	W5, W8	VCC	TEST_POINT	
32	1	W6	GND	TEST_POINT	
33	1	W7	CLK	TEST_POINT	

5 Revision history

Table 18. Document revision history

Date	Revision	Changes
06-Nov-2012	1	Initial release.