High-performance Regulator IC Series for PCs

Ultra Low Dropout Linear Regulators for PC Chipsets

BD3508MUV, BD3509MUV

No.09030EAT22

● Description

The BD3508MUV / BD3509MUV ultra low-dropout linear chipset regulator operates from a very low input supply, and offers ideal performance in low input voltage to low output voltage applications. It incorporates a built-in N-MOSFET power transistor to minimize the input-to-output voltage differential to the ON resistance ($R_{ON\ MAX}$=100mΩ/50mΩ) level. By lowering the dropout voltage in this way, the regulator realizes high current output (Iomax=3.0A/4.0A) with reduced conversion loss, and thereby obviates the switching regulator and its power transistor, choke coil, and rectifier diode. Thus, the BD3508MUV / BD3509MUV are designed to enable significant package profile downsizing and cost reduction. An external resistor allows the entire range of output voltage configurations between 0.65 and 2.7V, while the NRCS (soft start) function enables a controlled output voltage ramp-up, which can be programmed to whatever power supply sequence is required.

● Features

1) Internal high-precision reference voltage circuit (0.65V±1%)
2) Built-in VCC under voltage lock out circuit (VCC=3.80V)
3) NRCS (soft start) function reduces the magnitude of in-rush current
4) Internal Nch MOSFET driver offers low ON resistance (65mΩ/28mΩ typ)
5) Built-in current limit circuit (3.0A/4.0A min)
6) Built-in thermal shutdown (TSD) circuit
7) Variable output (0.65～2.7V)
8) Incorporates high-power VQFN020V4040 package: 4.0×4.0×1.0(mm)
9) Tracking function

● Applications

Notebook computers, Desktop computers, LCD-TV, DVD, Digital appliances

● Model Lineup

Maximum output current	Package	VCC=5V
3A	VQFN020V4040	BD3508MUV
4A		BD3509MUV

●Absolute Maximum Ratings (Ta=100℃)

BD3508MUV / BD3509MUV

Parameter	Symbol	Limit		Unit
		BD3508MUV	BD3509MUV	
Input Voltage 1	VCC	6.0 *1		V
Input Voltage 2	VIN	6.0 *1		V
Input Voltage 3	VDD	-	6.0*1	V
Enable Input Voltage	Ven	6.0		V
Power Good Input Voltage	V_{PGOOD}	-	6.0	V
Power Dissipation 1	Pd1	0.34 *2		W
Power Dissipation 2	Pd2	0.70 *3		W
Power Dissipation 3	Pd3	1.21 *4		W
Power Dissipation 4	Pd4	3.56 *5		W
Operating Temperature Range	Topr	-10～+100		℃
Storage Temperature Range	Tstg	-55～+125		℃
Maximum Junction Temperature	Tjmax	+150		℃

*1 Should not exceed Pd.

*2 Reduced by 4mW/℃ for each increase in Ta≧25℃(no heat sink)

*3 1 layer, mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB (Copper foil area : 10.29mm^2)

*4 4 layers, mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB (Copper foil area : 10.29mm^2) , copper foil in each layers.

*5 4 layers, mounted on a board 74.2mm×74.2mm×1.6mm Glass-epoxy PCB (Copper foil area : 5505mm^2) , copper foil in each layers.

●Operating Conditions(Ta=25℃)

Parameter	Symbol	BD3508MUV		BD3509MUV		Unit
		Min	Max	Min	Max	
Input Voltage 1	VCC	4.3	5.5	4.3	5.5	V
Input Voltage 2	VIN	0.75	VCC-1 *6	0.7	VCC-1 *6	V
Input Voltage 3	VDD	-	-	2.7	5.5	V
Output Voltage setting Range	Vo	VFB	2.7	VFB	2.7	V
Enable Input Voltage	Ven	-0.3	5.5	-0.3	5.5	V
NRCS capacity	CNRCS	0.001	1	0.001	1	uF

*6 VCC and VIN do not have to be implemented in the order listed.

★This product is not designed for use in radioactive environments.

●Electrical Characteristics

(Unless otherwise specified, Ta=25℃ VCC=5V Ven=3V VIN=1.8V VDD=3.3V R1=3.9KΩ R2=3.3KΩ)

◎BD3508MUV

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Bias Current	ICC	-	0.7	1.4	mA	
VCC Shutdown Mode Current	IST	-	0	10	uA	Ven=0V
Output Voltage	Vo	-	1.200	-	V	
Maximum Output Current	Io	3.0	-	-	A	
Output Short Circuit Current	Iost	3.0	-	-	A	Vo=0V
Output Voltage Temperature Coefficient	Tcvo	-	0.01	-	%/℃	
Feedback Voltage 1	VFB1	0.643	0.650	0.657	V	
Feedback Voltage 2	VFB2	0.630	0.650	0.670	V	Io=0 to 3A Tj=-10 to 100℃ *7
Line Regulation 1	Reg.l1	-	0.1	0.5	%/V	VCC=4.3V to 5.5V
Line Regulation 2	Reg.l2	-	0.1	0.5	%/V	VIN=1.2V to 3.3V
Load Regulation	Reg.L	-	0.5	10	mV	Io=0 to 3A
Minimum Input-Output Voltage Differential	dVo	-	65	100	mV	Io=1A,VIN=1.2V Tj=-10 to 100℃ *7
Standby Discharge Current	Iden	1	-	-	mA	Ven=0V, Vo=1V
[ENABLE]						
Enable Pin Input Voltage High	Enhi	2	-	-	V	
Enable Pin Input Voltage Low	Enlow	-0.2	-	0.8	V	
Enable Input Bias Current	Ien	-	7	10	uA	Ven=3V
[FEEDBACK]						
Feedback Pin Bias Current	IFB	-100	0	100	nA	
[NRCS]						
NRCS Charge Current	Inrcs	14	20	26	uA	Vnrcs=0.5V
NRCS Standby Voltage	VSTB	-	0	50	mV	Ven=0V
[UVLO]						
VCC Under voltage Lock out Threshold Voltage	VccUVLO	3.5	3.8	4.1	V	VCC:Sweep-up
VCC Under voltage Lock out Hysteresis Voltage	Vcchys	100	160	220	mV	VCC:Sweep-down
[AMP]						
Gate Source Current	I_{GSO}	-	1.6	-	mA	V_{FB}=0, V_{GATE}=2.5V
Gate Sink Current	I_{GSI}	-	4.7	-	mA	V_{FB}=VCC, V_{GATE}=2.5V

*7 Design Guarantee

●Electrical Characteristics

(Unless otherwise specified, Ta=25℃ VCC=5V Ven=3V VIN=1.5V VDD=3.3V R1=3.9KΩ R2=3.6KΩ)

◎BD3509MUV

Parameter	Symbol	Limit			Unit	Condition
		Min.	Typ.	Max.		
Bias Current	ICC	-	1.1	2.0	mA	
VCC Shutdown Mode Current	IST	-	0	10	uA	Ven=0V
Output Voltage	Vo	-	1.25	-	V	
Maximum Output Current	Io	4.0	-	-	A	
Output Voltage Temperature Coefficient	Tcvo	-	0.01	-	%/℃	
Feedback Voltage 1	VFB1	0.643	0.650	0.657	V	
Feedback Voltage 2	VFB2	0.637	0.650	0.663	V	Io=0 to 4A Tj=-10 to 100℃ *7
Line Regulation 1	Reg.I1	-	0.1	0.5	%/V	VCC=4.3V to 5.5V
Line Regulation 2	Reg.I2	-	0.1	0.5	%/V	VIN=1.2V to 3.3V
Load Regulation	Reg.L	-	0.5	10	mV	Io=0 to 4A
Minimum Input-Output Voltage Differential	dVo	-	28	50	mV	Io=1A,VIN=1.25V Tj=-10 to 100℃ *7
Standby Discharge Current	Iden	1	-	-	mA	Ven=0V, Vo=1V
[ENABLE]						
Enable Pin Input Voltage High	Enhi	2	-	-	V	
Enable Pin Input Voltage Low	Enlow	-0.2	-	0.8	V	
Enable Input Bias Current	Ien	-	7	10	uA	Ven=3V
[FEEDBACK]						
Feedback Pin Bias Current	IFB	-100	0	100	nA	
[NRCS]						
NRCS Charge Current	Inrcs	14	20	26	uA	Vnrcs=0.5V
NRCS Standby Voltage	VSTB	-	0	50	mV	Ven=0V
[UVLO]						
VCC Under voltage Lock out Threshold Voltage	VccUVLO	3.5	3.8	4.1	V	VCC:Sweep-up
VCC Under voltage Lock out Hysteresis Voltage	Vcchys	100	160	220	mV	VCC:Sweep-down
[AMP]						
Gate Source Current	I_{GSO}	-	10	-	mA	V_{FB}=0, V_{GATE}=2.5V
Gate Sink Current	I_{GSI}	-	18	-	mA	V_{FB}=VCC, V_{GATE}=2.5V
[PGOOD Block]						
Threshold voltage	V_{THPG}	-	0.585	-	V	FB voltage
Ron	R_{PG}	-	0.1	-	kΩ	

*7 Design Guarantee

●Reference Data

BD3508MUV

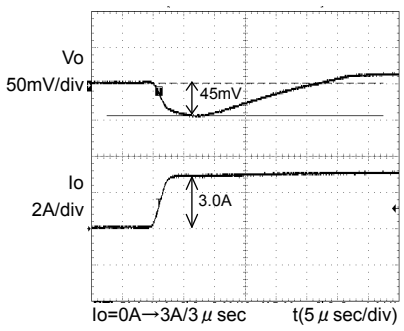


Fig.1 Transient Response
(0→3A)
Co=150 μ F × 2, CFB=0.01uF

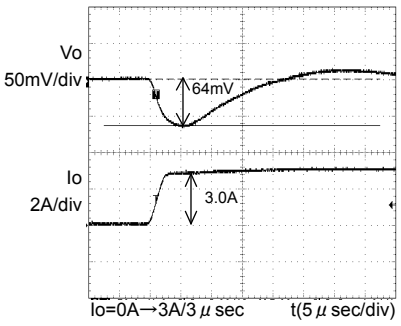


Fig.2 Transient Response
(0→3A)
Co=150 μ F

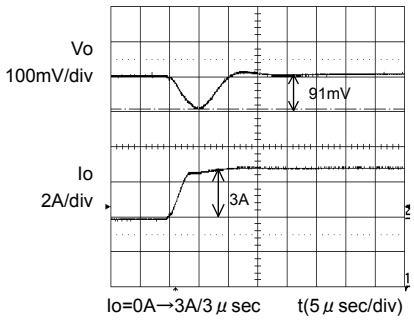


Fig.3 Transient Response
(0→3A)
Co=47 μ F, CFB=0.01uF

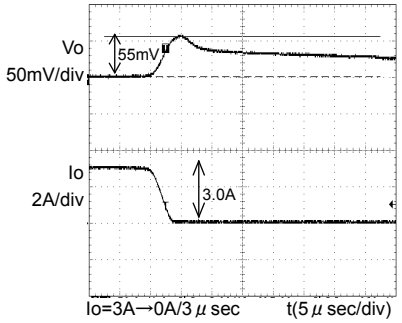


Fig.4 Transient Response
(3→0A)
Co=150 μ F × 2

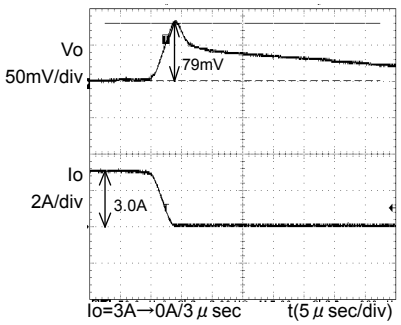


Fig.5 Transient Response
(3→0A)
Co=150 μ F

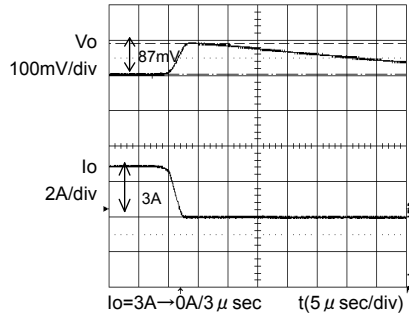


Fig.6 Transient Response
(3→0A)
Co=47 μ F

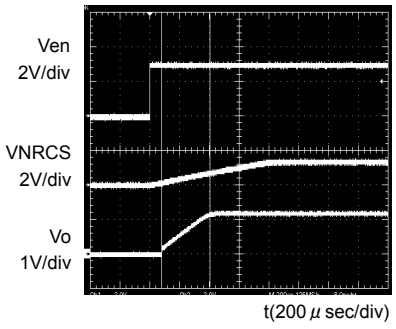


Fig.7: Waveform at output start

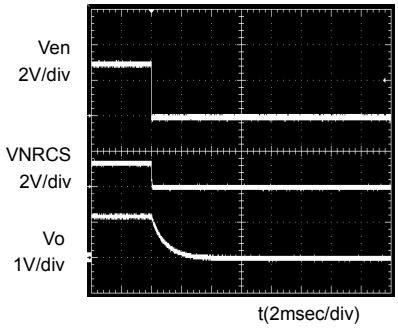


Fig.8 Waveform at output OFF

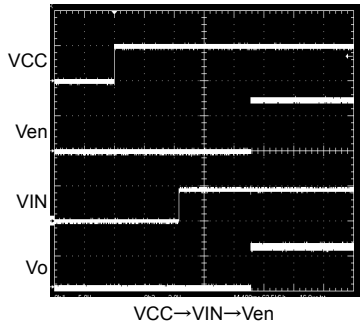


Fig.9 Input sequence

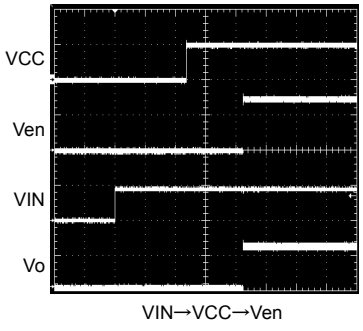


Fig.10 Input sequence

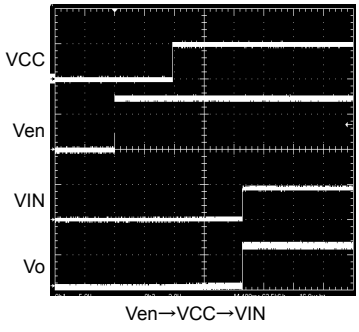


Fig.11 Input sequence

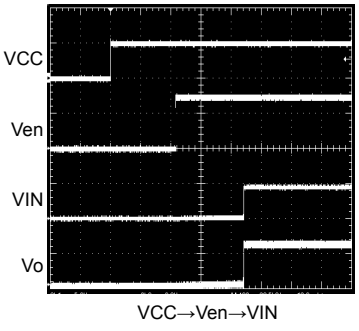


Fig.12 Input sequence

●Reference Data

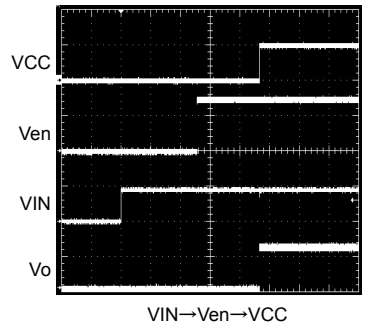


Fig.13 Input sequence

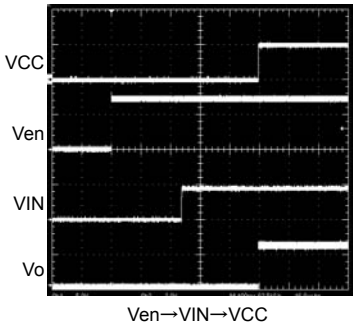


Fig.14 Input sequence

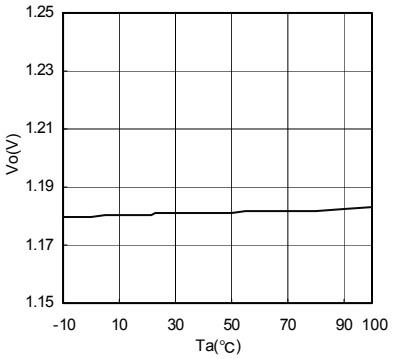


Fig.15 Tj-Vo (Io=0mA)

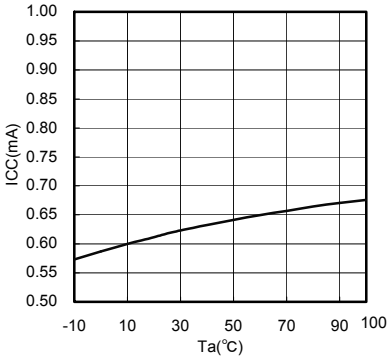


Fig.16 Tj-ICC

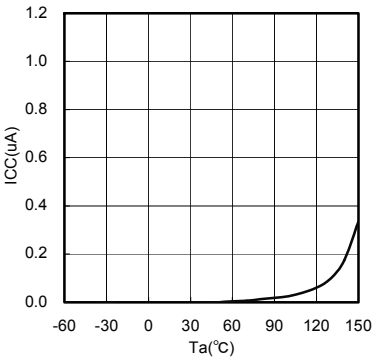


Fig.17 Tj-ISTB

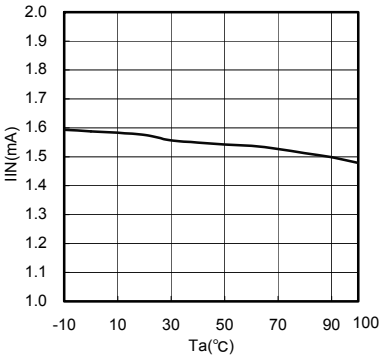


Fig.18 Tj-IIN

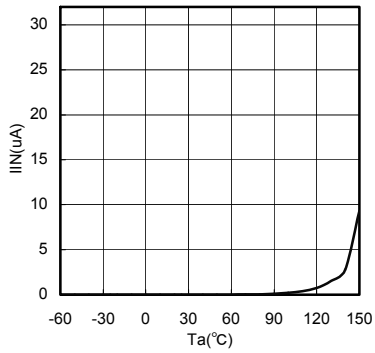


Fig.19 Tj-IINSTB

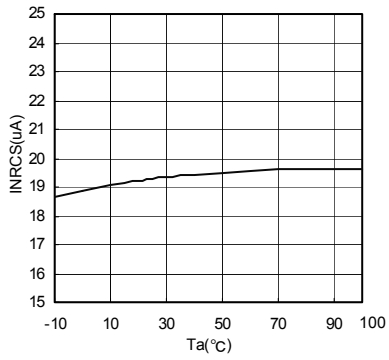


Fig.20 Tj-INRCS

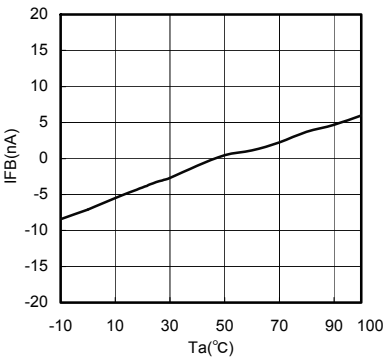


Fig.21 Tj-IFB

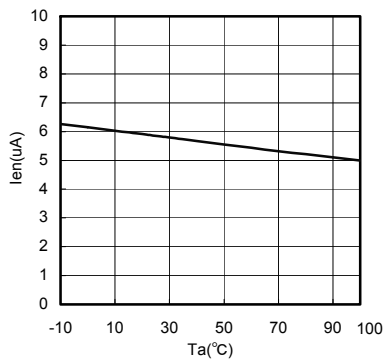


Fig.22 Tj-Ien

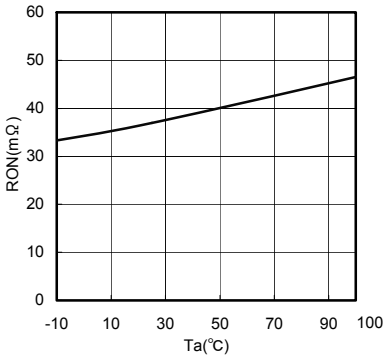


Fig.23 Tj-RON
(Vcc=5V/Vo=1.2V)

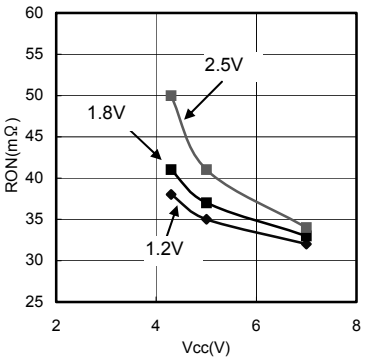


Fig.24 Vcc-RON

●Reference Data

BD3509MUV

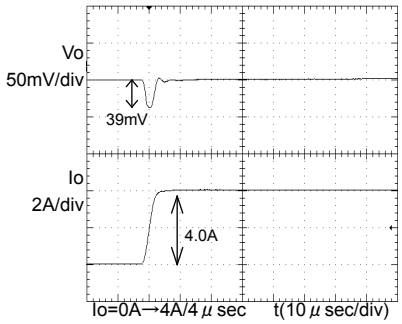


Fig.25 Transient Response
(0→4A)
Co=22 μ F

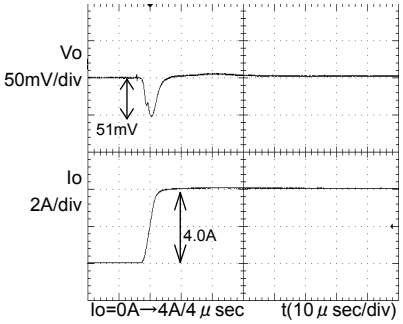


Fig.26 Transient Response
(0→4A)
Co=100 μ F

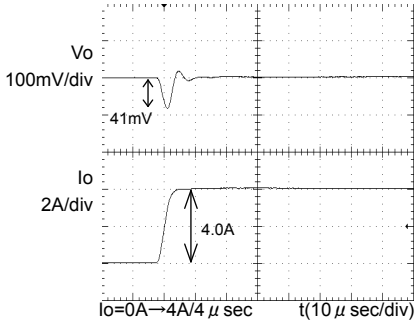


Fig.27 Transient Response
(0→4A)
Co=47 μ F

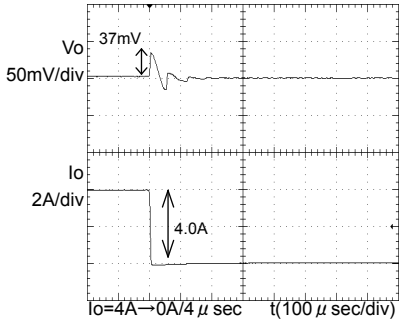


Fig.28 Transient Response
(4→0A)
Co=22 μ F, C_{FB}=0.01 μ F

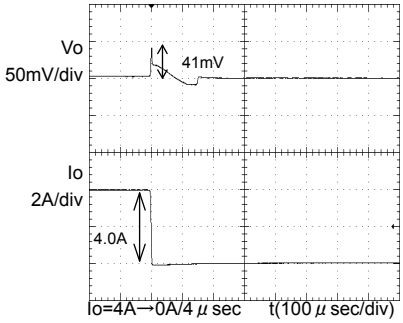


Fig.29 Transient Response
(4→0A)
Co=100 μ F

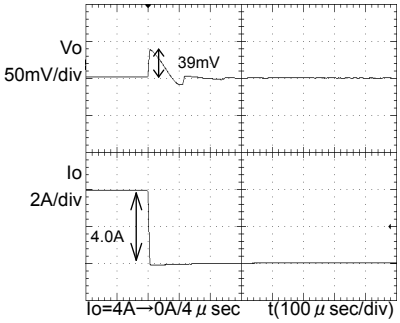


Fig.30 Transient Response
(4→0A)
Co=47 μ F, C_{FB}=0.01 μ F

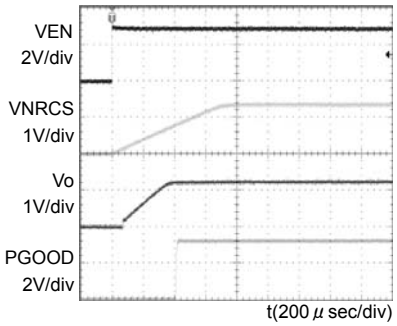


Fig.31: Waveform at output start

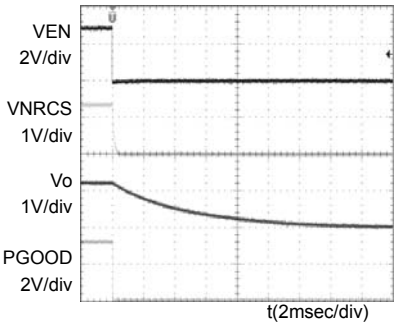


Fig.32 Waveform at output
OFF

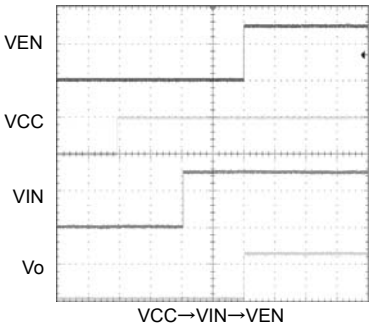


Fig.33 Input sequence

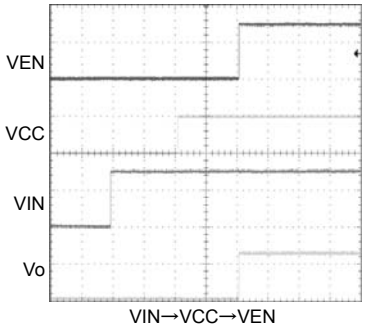


Fig.34 Input sequence

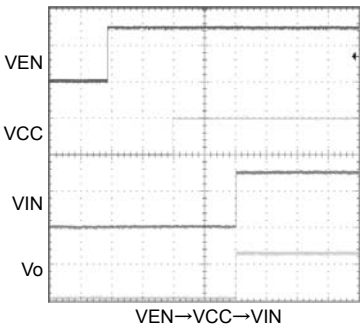


Fig.35 Input sequence

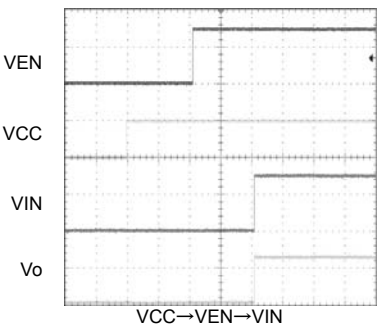


Fig.36 Input sequence

●Reference Data

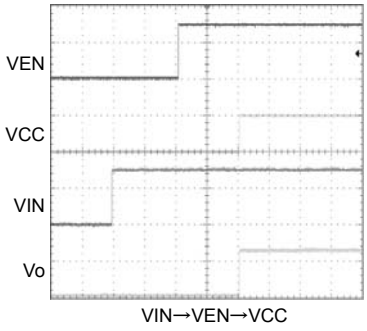


Fig.37 Input sequence

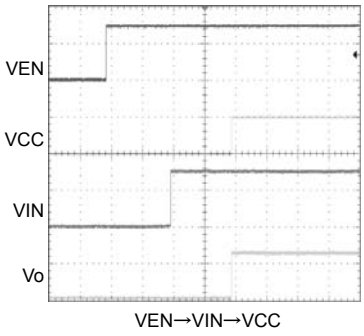


Fig.38 Input sequence

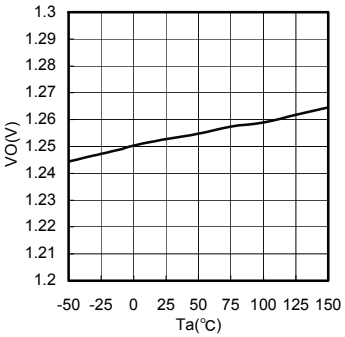


Fig.39 Tj-Vo (Io=0mA)

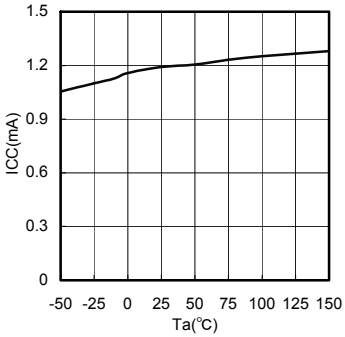


Fig.40 Tj-ICC

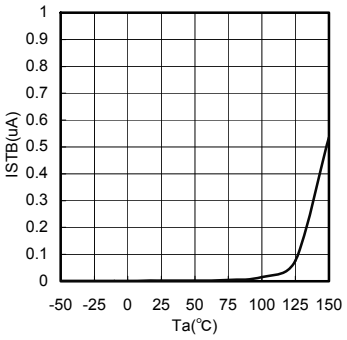


Fig.41 Tj-ISTB

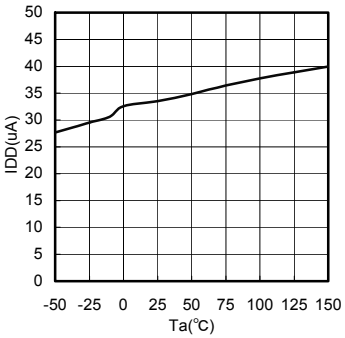


Fig.42 Tj-IDD

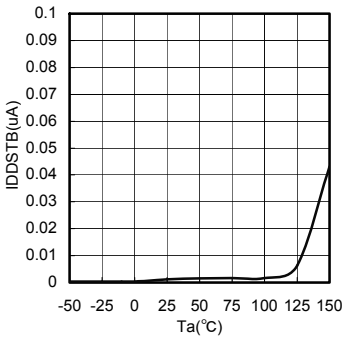


Fig.43 Tj-IDDSTB

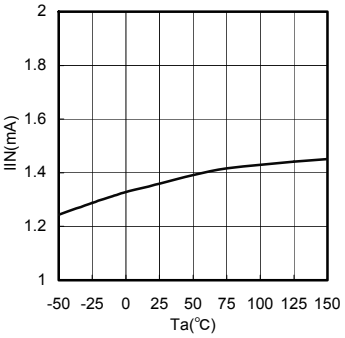


Fig.44 Tj-IIN

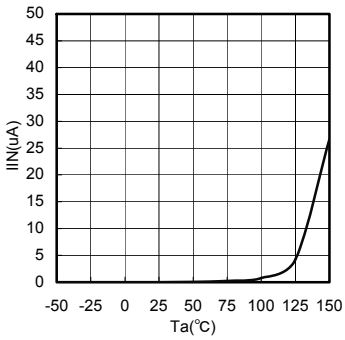


Fig.45 Tj-IINSTB

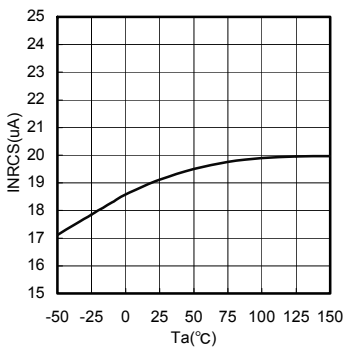


Fig.46 Tj-INRCS

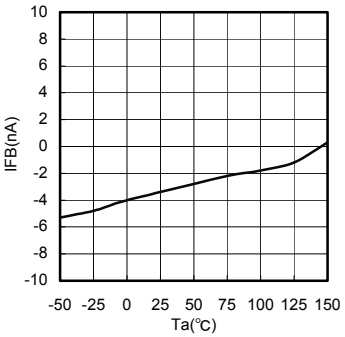


Fig.47 Tj-IFB

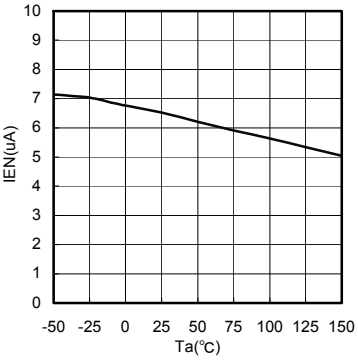


Fig.48 Tj-Ien

●Reference Data

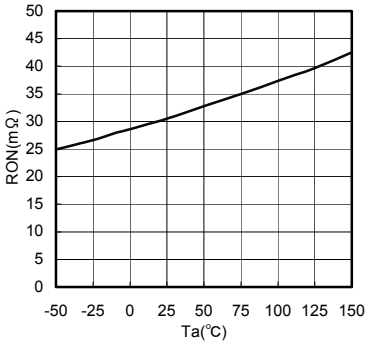


Fig.49 Tj-RON
(Vcc=5V/Vo=1.2V)

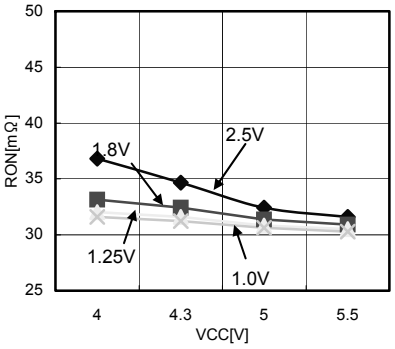
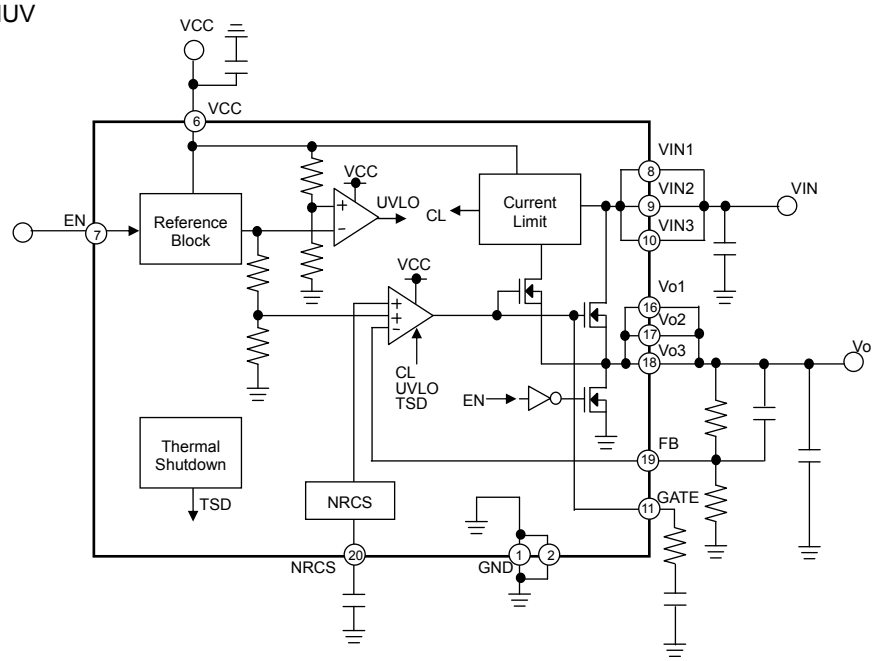


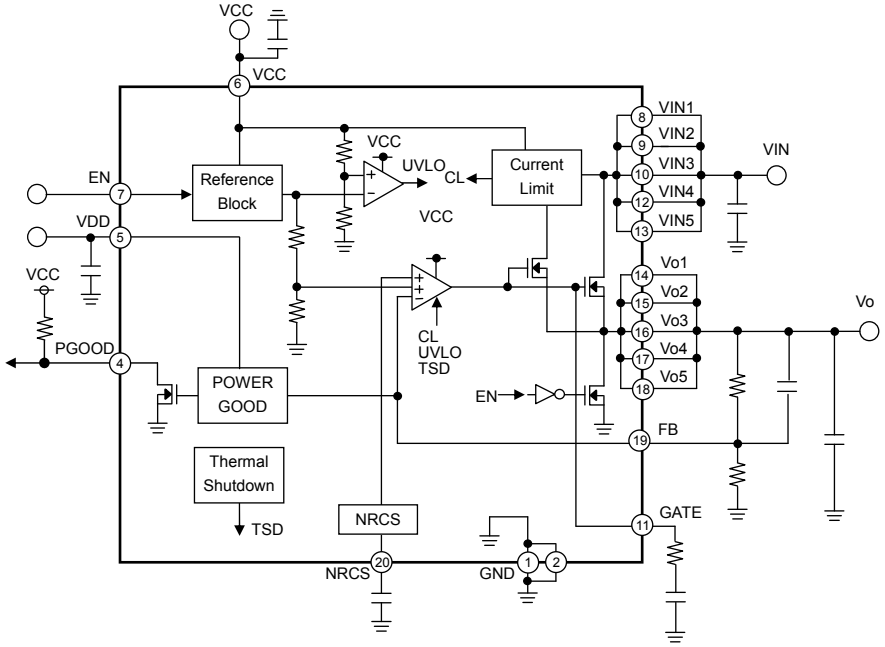
Fig.50 Vcc-RON

●Block Diagram

BD3508MUV

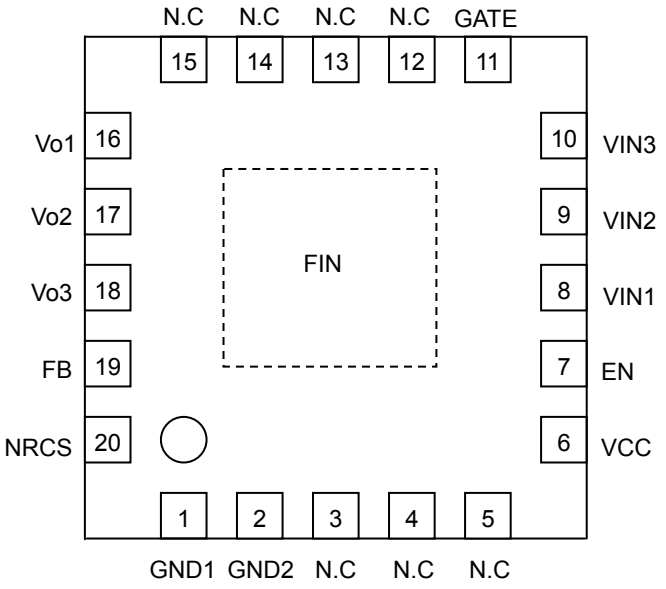


BD3509MUV

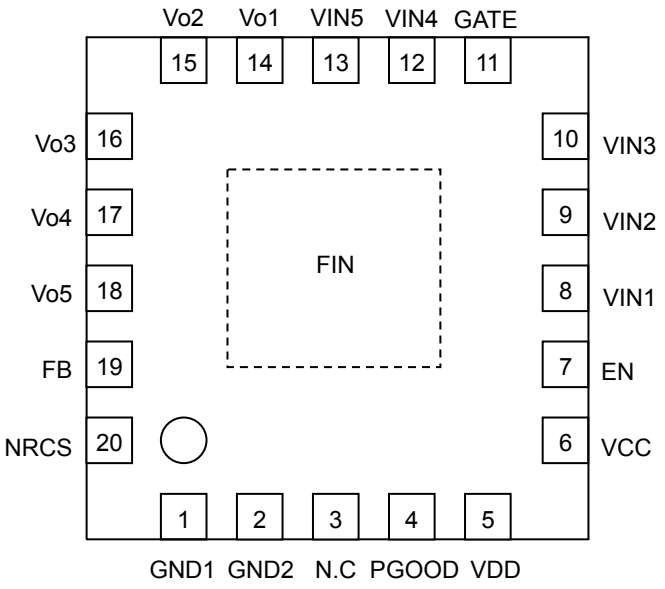


●Pin Layout

BD3508MUV



BD3509MUV



●Pin Function Table

BD3508MUV

PIN No.	PIN Name	PIN Function
1	GND1	Ground pin 1
2	GND2	Ground pin 2
3	N.C.	No connection (empty) pin *
4	N.C.	No connection (empty) pin *
5	N.C.	No connection (empty) pin *
6	VCC	Power supply pin
7	EN	Enable input pin
8	VIN1	Input pin 1
9	VIN2	Input pin 2
10	VIN3	Input pin 3
11	GATE	Gate pin
12	N.C.	No connection (empty) pin *
13	N.C.	No connection (empty) pin *
14	N.C.	No connection (empty) pin *
15	N.C.	No connection (empty) pin *
16	Vo1	Output voltage pin 1
17	Vo2	Output voltage pin 2
18	Vo3	Output voltage pin 3
19	FB	Reference voltage feedback pin
20	NRCS	In-rush current protection (NRCS) capacitor connection pin
reverse	FIN	Connected to heatsink and GND

* Please short N.C to the GND。

BD3509MUV

PIN No.	PIN Name	PIN Function
1	GND1	Ground pin 1
2	GND2	Ground pin 2
3	N.C.	No connection (empty) pin *
4	PGOOD	Power Good pin
5	VDD	Power supply pin
6	VCC	Power supply pin
7	EN	Enable input pin
8	VIN1	Input pin 1
9	VIN2	Input pin 2
10	VIN3	Input pin 3
11	GATE	Gate pin
12	VIN4	Input pin 4
13	VIN5	Input pin 5
14	Vo1	Output voltage pin 1
15	Vo2	Output voltage pin 2
16	Vo3	Output voltage pin 3
17	Vo4	Output voltage pin 4
18	Vo5	Output voltage pin 5
19	FB	Reference voltage feedback pin
20	NRCS	In-rush current protection (NRCS) capacitor connection pin
reverse	FIN	Connected to heatsink and GND

* Please short N.C to the GND

●Operation of Each Block

・AMP

This is an error amp that functions by comparing the reference voltage (0.65V) with Vo to drive the output Nch FET (Ron=50mΩ). Frequency optimization helps to realize rapid transit response, and to support the use of functional polymer output capacitors. AMP input voltage ranges from GND to 2.7V, while the AMP output ranges from GND to VCC. When EN is OFF, or when UVLO is active, output goes LOW and the output NchFET switches OFF.

・EN

The EN block controls the regulator ON/OFF pin by means of the logic input pin. In OFF position, circuit voltage is maintained at 0μA, thus minimizing current consumption at standby. The FET is switched ON to enable discharge of the NRCS pin Vo, thereby draining the excess charge and preventing the load IC from malfunctioning. Since no electrical connection is required (such as between the VCC pin and the ESD prevention Di), module operation is independent of the input sequence.

・UVLO

To prevent malfunctions that can occur when there is a momentary decrease in VCC supply voltage, the UVLO circuit switches output OFF, and, like the EN block, discharges the NRCS Vo. Once the UVLO threshold voltage (TYP3.80V) is exceeded, the power-on reset is triggered and output begins.

・CURRENT LIMIT

With output ON, the current limit function monitors internal IC output current against the parameter value. When current exceeds this level, the current limit module lowers the output current to protect the load IC. When the overcurrent state is eliminated, output voltage is restored at the parameter value.

・NRCS

The soft start function is realized by connecting an NRCS pin external capacitor to the target ground. Output ramp-up can be set for any period up to the time the NRCS pin reaches VFB (0.65V). During startup, the NRCS pin serves as the 20μA (TYP) constant current source and charges the externally connected capacitor.

・TSD (Thermal Shut Down)

The shutdown (TSD) circuit automatically switches output OFF when the chip temperature gets too high, thus serving to protect the IC against “thermal runaway” and heat damage. Because the TSD circuit is provided to shut down the IC in the presence of extreme heat, in order to avoid potential problems with the TSD, it is crucial that the Tj (max) parameter not be exceeded in the thermal design.

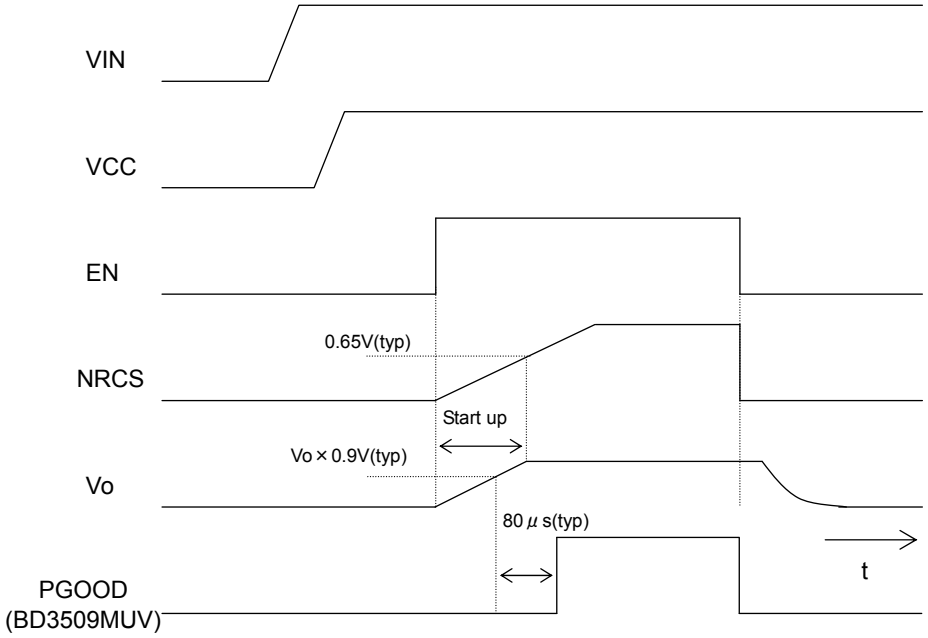
・VIN

The VIN line is the major current supply line, and is connected to the output NchFET drain. Since no electrical connection (such as between the VCC pin and an ESD protective Di) is necessary, VIN operates independent of the input sequence. However, since there is an output NchFET body Di between VIN and Vo, a VIN-Vo electric (Di) connection is present. Note, therefore, that when output is switched ON or OFF, reverse current may flow to the VIN from Vo.

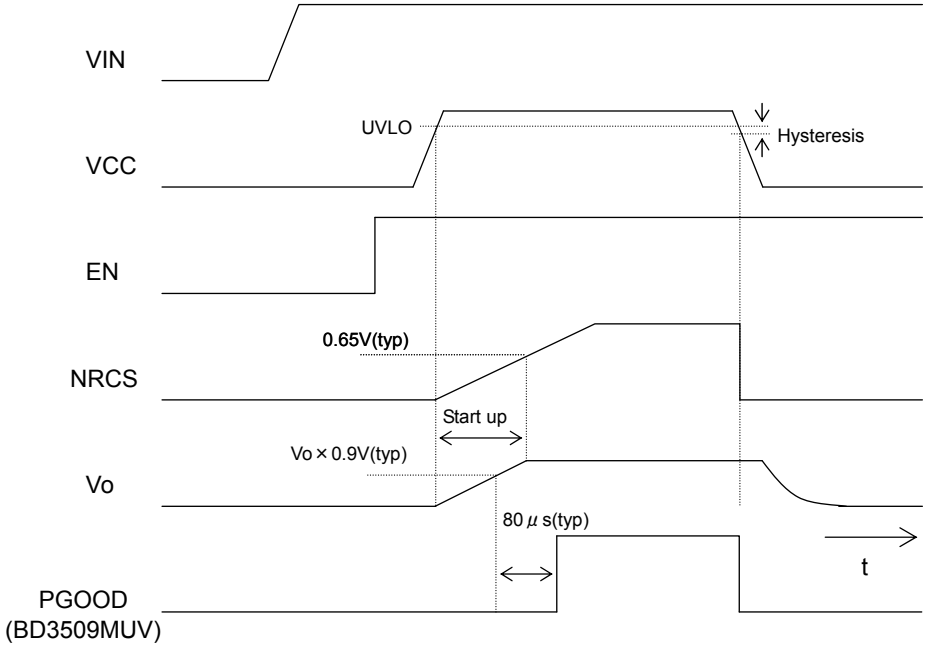
・PGOOD (BD3509MUV)

This is the monitor pin for output voltage (Vo). It is used through the pull-up resistance (100kΩ). PGOOD pin judges the voltage High or Low (FB Voltage 0.585V typ. : threshold voltage).

●Timing Chart

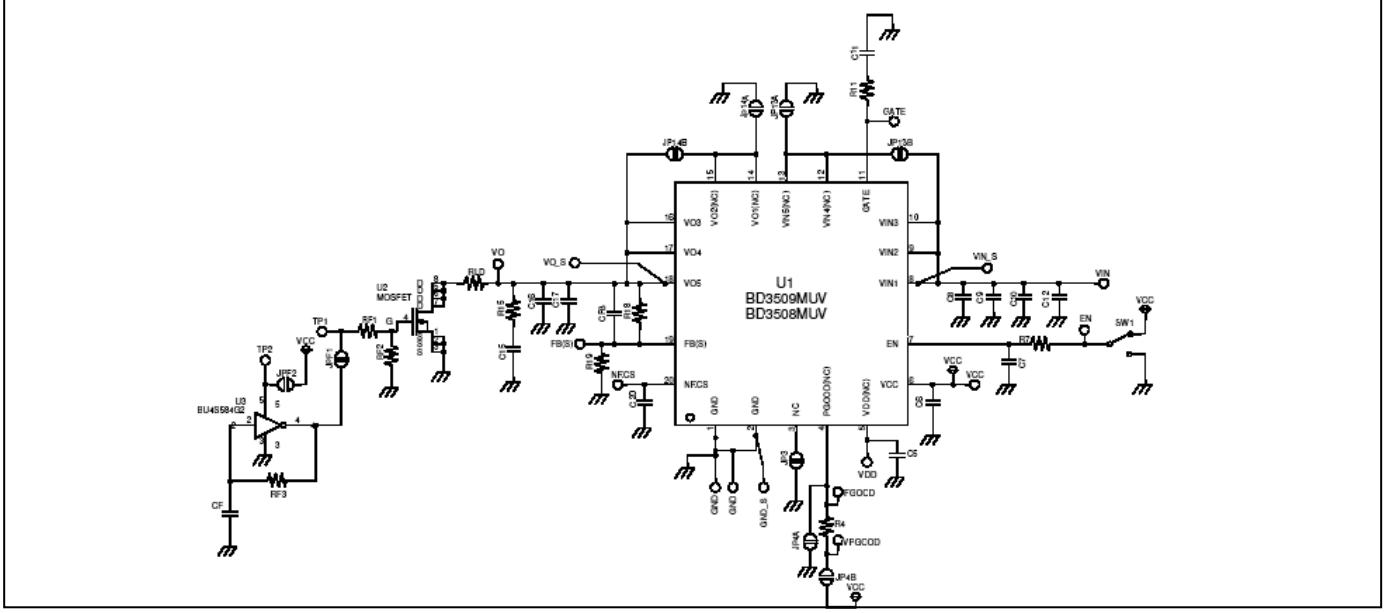


VCC ON/OFF



●Evaluation Board

■ **BD3509MUV Evaluation Board Schematic**



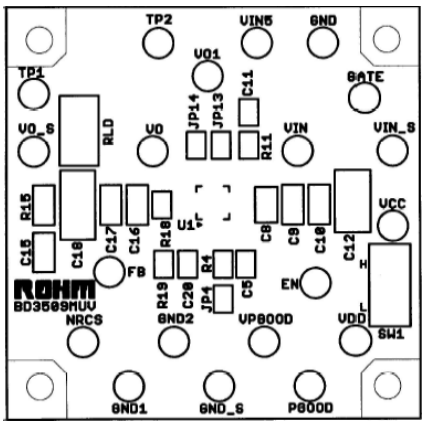
■ **BD3509MUV Evaluation Board Standard Component List**

Component	Rating	Manufacturer	Product Name
U1	-	ROHM	BD3509MUV
C5	0.1uF	MURATA	GRM155F11E104ZD
C6	1uF	MURATA	GRM188B11A105KD
C8	10uF	MURATA	GRM21BB10J106KD
C16	22uF	KYOCERA	**CM316W5R226K06AT**
C20	0.01uF	MURATA	GRM188B11H103KD

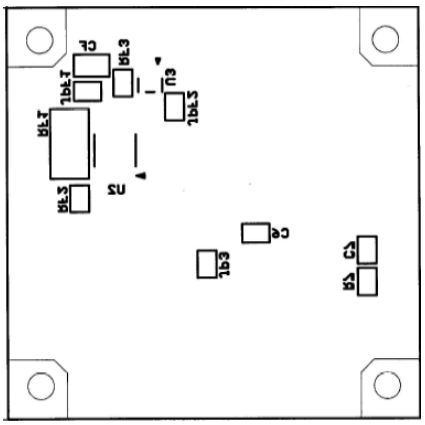
Component	Rating	Manufacturer	Product Name
R4	100kΩ	ROHM	MCR03EZPF1003
R7	0Ω	-	Jumper
R8	3.6k	ROHM	MCR03EZPF3601
R9	3.9kΩ	ROHM	MCR03EZPF3901
JP13	0Ω	-	Jumper
JP14	0Ω	-	Jumper

■ **BD3509MUV Evaluation Board Layout**

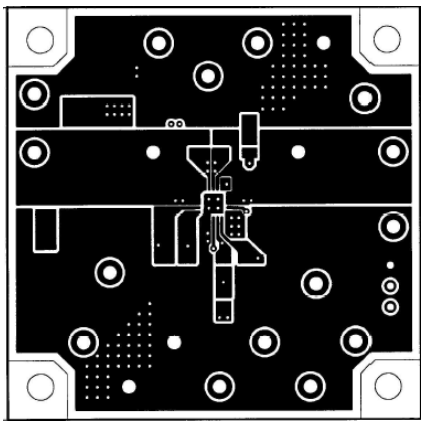
Silk Screen (Top)



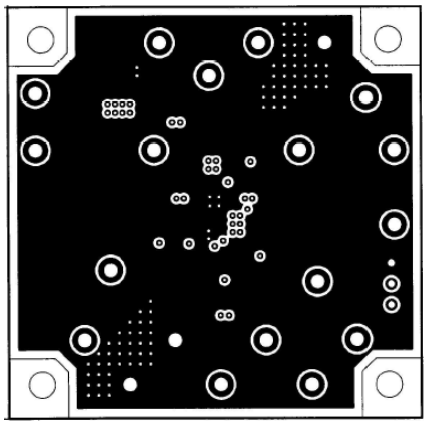
Silk Screen (Bottom)



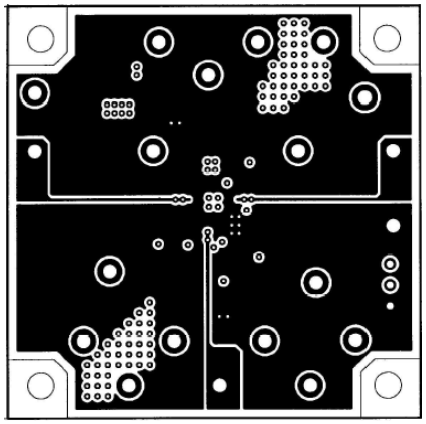
TOP Layer



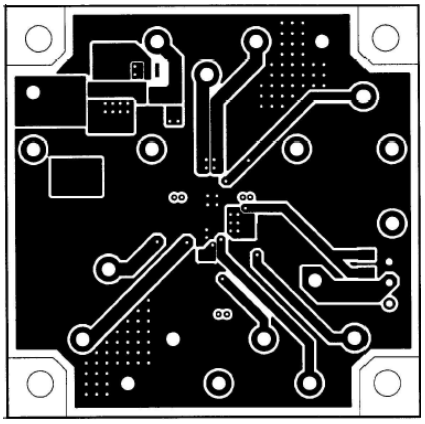
Middle Layer_1



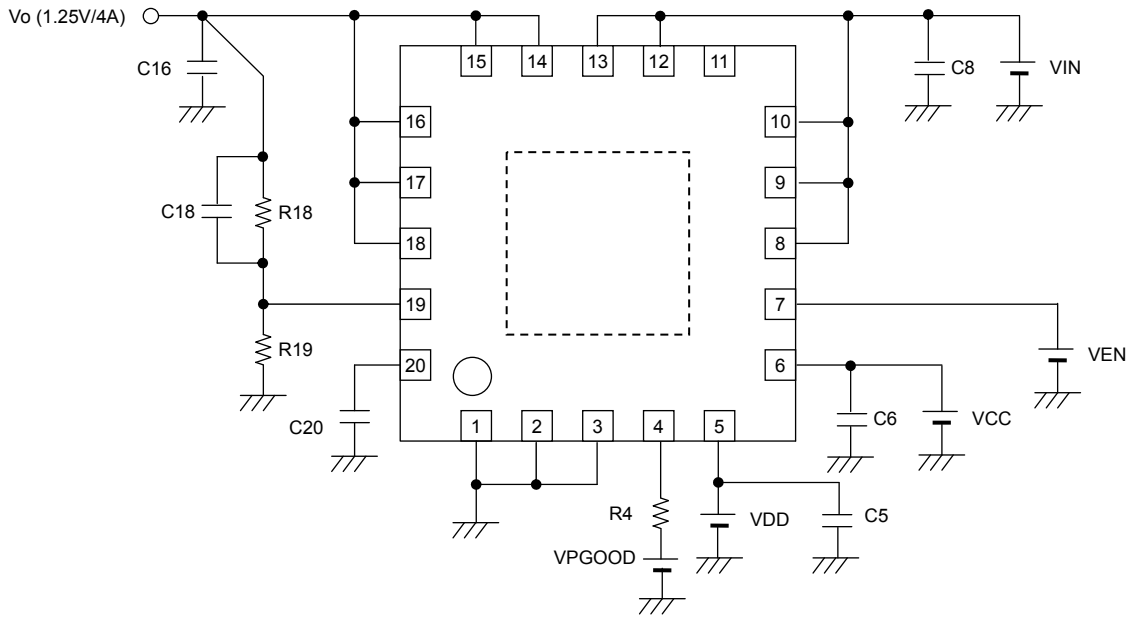
Middle Layer_2



Bottom Layer



●Recommended Circuit Example



Component	Recommended Value	Programming Notes and Precautions
R1/R2	3.6k/3.9k	IC output voltage can be set with a configuration formula using the values for the internal reference output voltage (V_{FB}) and the output voltage resistors (R1, R2). Select resistance values that will avoid the impact of the V_{FB} current (±100nA). The recommended total resistance value is 10KΩ.
R4	100k	This is the pull-up resistance for open drain pin. It is recommended to set the value about 100kΩ.
C16	22uF	To assure output voltage stability, please be certain the Vo1, Vo2, and Vo3 pins and the GND pins are connected. Output capacitors play a role in loop gain phase compensation and in mitigating output fluctuation during rapid changes in load level. Insufficient capacitance may cause oscillation, while high equivalent series reisistance (ESR) will exacerbate output voltage fluctuation under rapid load change conditions. While a 47μF ceramic capacitor is recomended, actual stability is highly dependent on temperature and load conditions. Also, note that connecting different types of capacitors in series may result in insufficient total phase compensation, thus causing oscillation. In light of this information, please confirm operation across a variety of temperature and load conditions.
C6	1uF	The input capacitor reduces the output impedence of the voltage supply source connected to the VCC. When the output impedence of this power supply increases, the input voltage (VCC) may become unstable. This may result in the output voltage oscillation or lowering ripple rejection. A low ESR 1uF capacitor with minimal susceptibility to temperature is preferable, but stability depends on power supply characteristics and the substrate wiring pattern. Please confirm operation across a variety of temperature and load conditions.
C8	10uF	Input capacitors reduce the output impedance of the voltage supply source connected to the (VIN) input pins. If the impedance of this power supply were to increase, input voltage (VIN) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 10uF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C5	0.1uF	Input capacitors reduce the output impedance of the voltage supply source connected to the (VDD) input pins. If the impedance of this power supply were to increase, input voltage (VDD) could become unstable, leading to oscillation or lowered ripple rejection function. While a low-ESR 0.1uF capacitor with minimal susceptibility to temperature is recommended, stability is highly dependent on the input power supply characteristics and the substrate wiring pattern. In light of this information, please confirm operation across a variety of temperature and load conditions.
C20	0.01uF	The Non Rush Current on Startup (NRCS) function is built into the IC to prevent rush current from going through the load (VIN to Vo) and impacting output capacitors at power supply start-up. Constant current comes from the NRCS pin when EN is HIGH or the UVLO function is deactivated. The temporary reference voltage is proportionate to time, due to the current charge of the NRCS pin capacitor, and output voltage start-up is proportionate to this reference voltage. Capacitors with low susceptibility to temperature are recommended, in order to assure a stable soft-start time.
C18	0.01uF	This component is employed when the C16 capacitor causes, or may cause, oscillation. It provides more precise internal phase correction.

●Heat Loss

Thermal design should allow operation within the following conditions. Note that the temperatures listed are the allowed temperature limits, and thermal design should allow sufficient margin from the limits.

1. Ambient temperature Ta can be no higher than 100 ℃.
2. Chip junction temperature (Tj) can be no higher than 150℃.

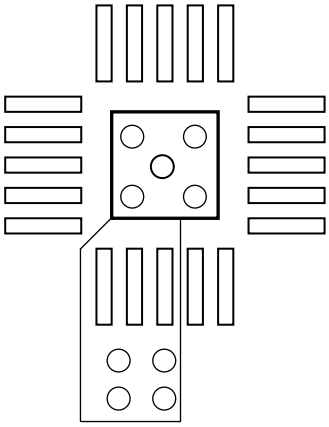
Chip junction temperature can be determined as follows:

① Calculation based on ambient temperature (Ta)
Tj=Ta+ θ j-a × W

＜Reference values＞

θ j-a: VQFN020V4040	367.6℃/W	Bare (unmounted) IC
	178.6℃/W	4-layer substrate (bottom layer surface copper foil area 10.29mm^2)
	103.3℃/W	4-layer substrate (bottom layer surface copper foil area 10.29mm^2)
	35.1℃/W	4-layer substrate (top layer copper foil area 5505mm^2)
	Substrate size: 74.2 × 74.2 × 1.6mm^3 (substrate with thermal via)	

It is recommended to layout the VIA for heat radiation in the GND pattern of reverse (of IC) when there is the GND pattern in the inner layer (in using multiplayer substrate). This package is so small (size: 4.2mm × 4.2mm) that it is not available to layout the VIA in the bottom of IC. Spreading the pattern and being increased the number of VIA like the figure below). enable to get the superior heat radiation characteristic. (This figure is the image. It is recommended that the VIA size and the number is designed suitable for the actual situation.).



Most of the heat loss that occurs in the BD3509MUV is generated from the output Nch FET. Power loss is determined by the total VIN-Vo voltage and output current. Be sure to confirm the system input and output voltage and the output current conditions in relation to the heat dissipation characteristics of the VIN and Vo in the design. Bearing in mind that heat dissipation may vary substantially depending on the substrate employed (due to the power package incorporated in the BD3509MUV) make certain to factor conditions such as substrate size into the thermal design.

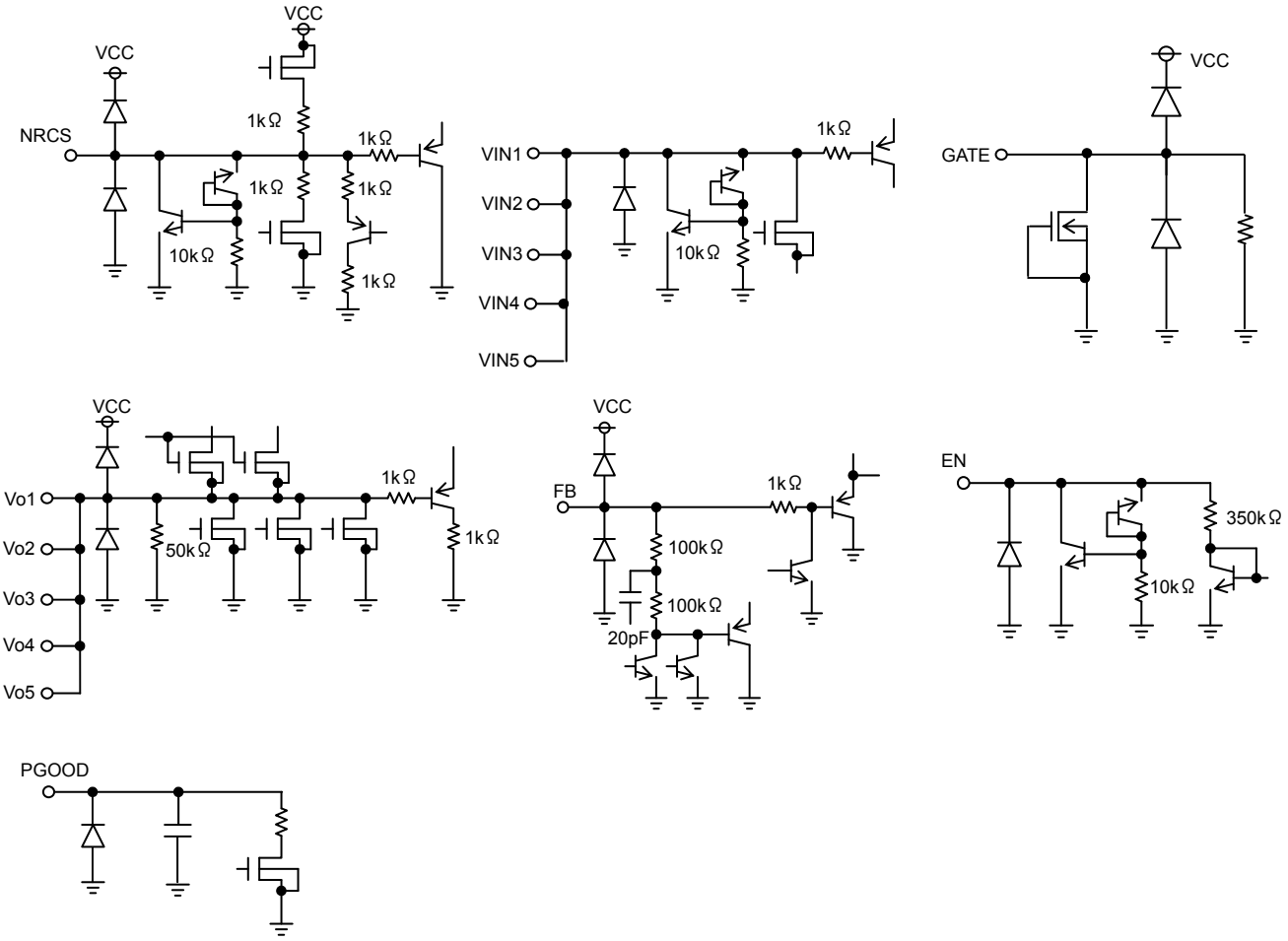
$$\text{Power consumption (W)} = \{ \text{Input voltage (VIN)- output voltage (Vo)} \} \times \text{Io (Ave)}$$

Example) VIN=1.5V, Vo=1.25V, Io(Ave) = 4A

$$\text{Power consumption (W)} = \{ 1.5\text{(V)}-1.2\text{(V)} \} \times 4.0\text{(A)}$$

$$= 1.0\text{(W)}$$

●Input-Output Equivalent Circuit Diagram



●Operation Notes

1. Absolute maximum ratings

An excess in the absolute maximum ratings, such as supply voltage, temperature range of operating conditions, etc., can break down the devices, thus making impossible to identify breaking mode, such as a short circuit or an open circuit. If any over rated values will expect to exceed the absolute maximum ratings, consider adding circuit protection devices, such as fuses.

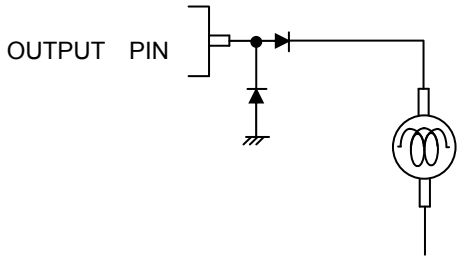
2. Connecting the power supply connector backward

Connecting of the power supply in reverse polarity can damage IC. Take precautions when connecting the power supply lines. An external direction diode can be added.

3. Output pin

In the event that load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is requested to insert a protection diode.

(Example)



4. GND voltage

The potential of GND pin must be minimum potential in all operating conditions.

5. Thermal design

Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.

6. Inter-pin shorts and mounting errors

Use caution when positioning the IC for mounting on printed circuit boards. The IC may be damaged if there is any connection error or if pins are shorted together.

7. Actions in strong electromagnetic field

Use caution when using the IC in the presence of a strong electromagnetic field as doing so may cause the IC to malfunction.

8. ASO

When using the IC, set the output transistor so that it does not exceed absolute maximum ratings or ASO.

9. Thermal shutdown circuit

The IC incorporates a built-in thermal shutdown circuit (TSD circuit). The thermal shutdown circuit (TSD circuit) is designed only to shut the IC off to prevent thermal runaway. It is not designed to protect the IC or guarantee its operation. Do not continue to use the IC after operating this circuit or use the IC in an environment where the operation of this circuit is assumed.

	TSD on temperature [°C] (typ.)	Hysteresis temperature [°C] (typ.)
BD3508MUV / BD3509MUV	175	15

10. Testing on application boards

When testing the IC on an application board, connecting a capacitor to a pin with low impedance subjects the IC to stress. Always discharge capacitors after each process or step. Always turn the IC's power supply off before connecting it to or removing it from a jig or fixture during the inspection process. Ground the IC during assembly steps as an antistatic measure. Use similar precaution when transporting or storing the IC.

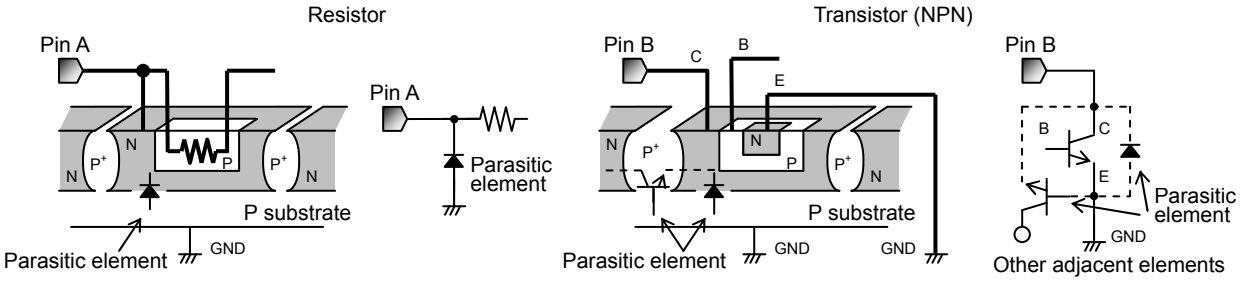
11. Regarding input pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of these P layers with the N layers of other elements, creating a parasitic diode or transistor. For example, the relation between each potential is as follows:

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.

When GND > Pin B, the P-N junction operates as a parasitic transistor.

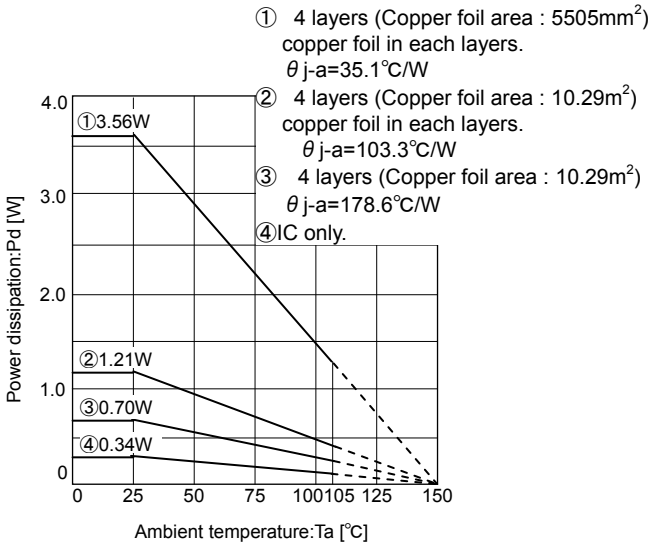
Parasitic diodes can occur inevitable in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, methods by which parasitic diodes operate, such as applying a voltage that is lower than the GND (P substrate) voltage to an input pin, should not be used.



12. Ground Wiring Pattern

When using both small signal and large current GND patterns, it is recommended to isolate the two ground patterns, placing a single ground point at the ground potential of application so that the pattern wiring resistance and voltage variations caused by large currents do not cause variations in the small signal ground voltage. Be careful not to change the GND wiring pattern of any external components, either.

● Heat Dissipation Characteristics

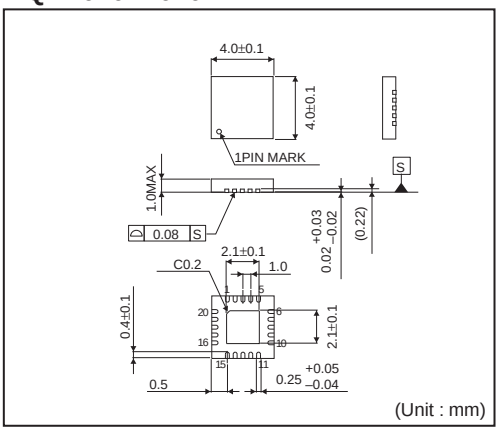


● **Ordering part number**

B	D	3	5	0	8	M	U	V	-	E	2

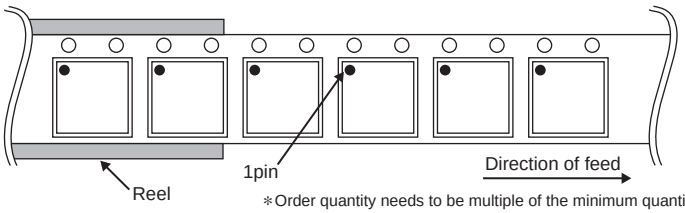
Part No.	Part No. 3508 3509	Package MUV: VQFN020V4040	Packaging and forming specification E2: Embossed tape and reel

VQFN020V4040



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Notes

No copying or reproduction of this document, in part or in whole, is permitted without the consent of ROHM Co.,Ltd.

The content specified herein is subject to change for improvement without notice.

The content specified herein is for the purpose of introducing ROHM's products (hereinafter "Products"). If you wish to use any such Product, please be sure to refer to the specifications, which can be obtained from ROHM upon request.

Examples of application circuits, circuit constants and any other information contained herein illustrate the standard usage and operations of the Products. The peripheral conditions must be taken into account when designing circuits for mass production.

Great care was taken in ensuring the accuracy of the information specified in this document. However, should you incur any damage arising from any inaccuracy or misprint of such information, ROHM shall bear no responsibility for such damage.

The technical information specified herein is intended only to show the typical functions of and examples of application circuits for the Products. ROHM does not grant you, explicitly or implicitly, any license to use or exercise intellectual property or other rights held by ROHM and other parties. ROHM shall bear no responsibility whatsoever for any dispute arising from the use of such technical information.

The Products specified in this document are intended to be used with general-use electronic equipment or devices (such as audio visual equipment, office-automation equipment, communication devices, electronic appliances and amusement devices).

The Products specified in this document are not designed to be radiation tolerant.

While ROHM always makes efforts to enhance the quality and reliability of its Products, a Product may fail or malfunction for a variety of reasons.

Please be sure to implement in your equipment using the Products safety measures to guard against the possibility of physical injury, fire or any other damage caused in the event of the failure of any Product, such as derating, redundancy, fire control and fail-safe designs. ROHM shall bear no responsibility whatsoever for your use of any Product outside of the prescribed scope or not in accordance with the instruction manual.

The Products are not designed or manufactured to be used with any equipment, device or system which requires an extremely high level of reliability the failure or malfunction of which may result in a direct threat to human life or create a risk of human injury (such as a medical instrument, transportation equipment, aerospace machinery, nuclear-reactor controller, fuel-controller or other safety device). ROHM shall bear no responsibility in any way for use of any of the Products for the above special purposes. If a Product is intended to be used for any such special purpose, please contact a ROHM sales representative before purchasing.

If you intend to export or ship overseas any Product or technology specified herein that may be controlled under the Foreign Exchange and the Foreign Trade Law, you will be required to obtain a license or permit under the Law.

ROHM SEMICONDUCTOR

Thank you for your accessing to ROHM product informations.
More detail product informations and catalogs are available, please contact us.

ROHM Customer Support System

http://www.rohm.com/contact/