

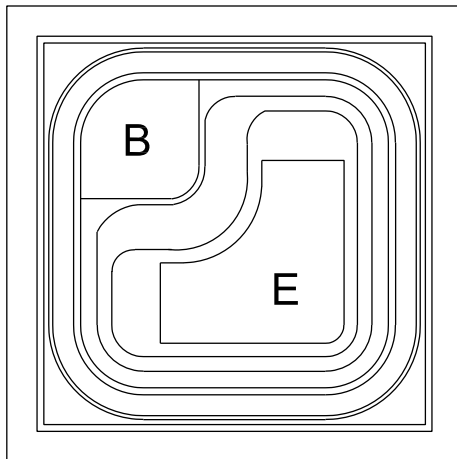
**PROCESS CP388X**  
**Small Signal Transistor**  
NPN - Low Noise Amplifier Transistor Chip



**PROCESS DETAILS**

Process	EPITAXIAL PLANAR
Die Size	13 x 13 MILS
Die Thickness	5.9 MILS
Base Bonding Pad Area	3.9 x 3.9 MILS
Emitter Bonding Pad Area	5.4 x 5.4 MILS
Top Side Metalization	Al-Si - 17,000Å
Back Side Metalization	Au - 12,000Å

**GEOMETRY**



BACKSIDE COLLECTOR R0

**GROSS DIE PER 5 INCH WAFER**

102,852

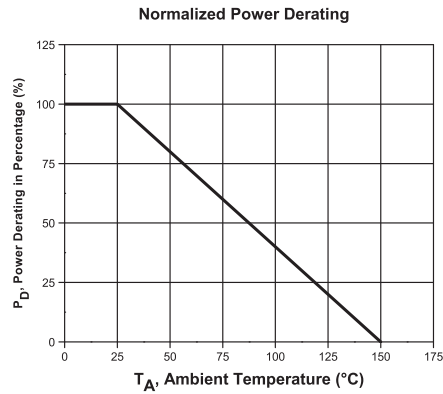
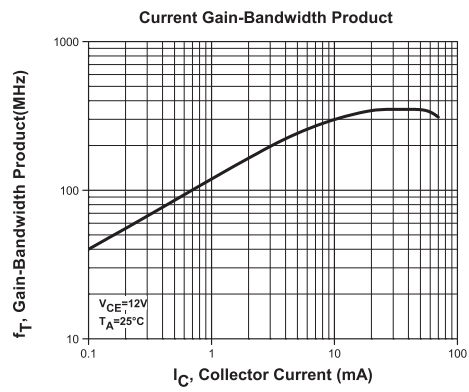
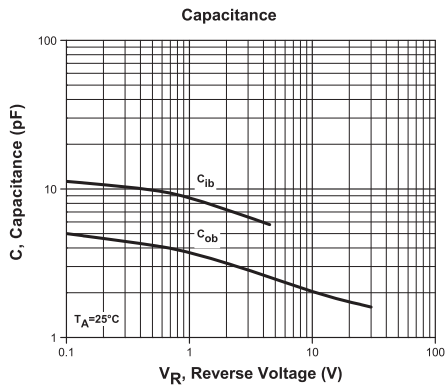
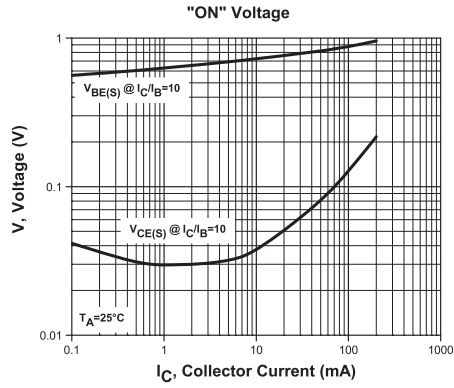
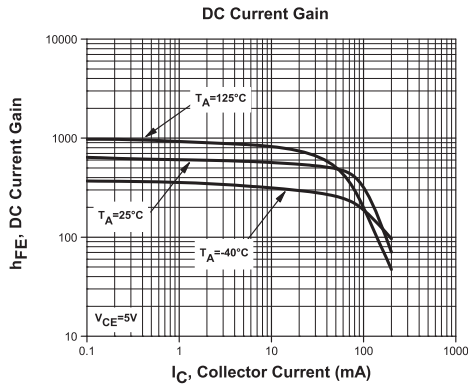
**PRINCIPAL DEVICE TYPES**

CMKT5089M10  
CMST5089  
2N4104

R2 (29-April 2010)

# PROCESS CP388X

## Typical Electrical Characteristics



R2 (29-April 2010)