Integrated Device Technology, Inc.

128K/256K BYTE CMOS SECONDARY CACHE MODULE FOR THE INTEL™ i486™

IDT7MP6085
IDT7MP6087

FEATURES:

- 128K/256K byte pin-compatible secondary cache modules
- Uses the IDT71589 32K x 9 CacheRAM™ with burst counter and self-timed write
- Matches all timing and signals of the i486™ processor
- 80 lead FR-4 SIMM (Single In-line Memory Module)
- Single 5V (±5%) power supply
- Multiple GND pins and decoupling capacitors for maximum noise immunity
- Inputs/outputs directly TTL-compatible

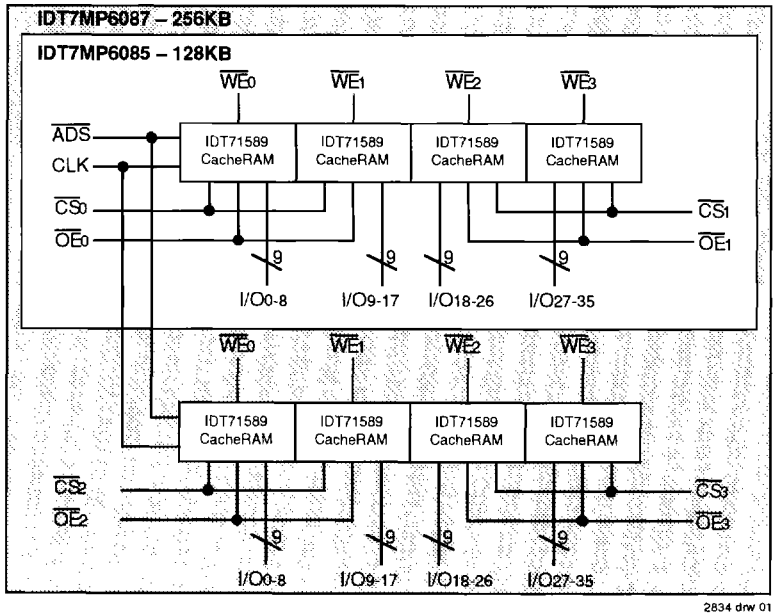
DESCRIPTION:

The IDT7MP6085/7MP6087 are pin-compatible secondary cache modules. The IDT7MP6085 is a 128KB cache, and the IDT7MP6087 is a 256KB cache. The IDT7MP6087 uses eight IDT71589 32K x 9 CacheRAMs in plastic SOJs, mounted on two sides of a multilayer epoxy laminate (FR-4) substrate with gold-plated leads, while the IDT7MP6085 uses four IDT71589s on one side of the same substrate. Extremely high speeds are achieved using IDT's high-performance, high-reliability CMOS technology. This module is designed to facilitate the implementation of the highest performance secondary caches for the i486.

The IDT7MP6085/7MP6087 contain a full set of write data and address registers. These registers are combined with the internal write abort logic to allow the processor to generate a self-timed write based upon a decision which can be left until the end of the write cycle. An internal burst address counter accepts the first cycle address from the processor and then cycles through the adjacent four locations using the i486's burst refill sequence on appropriate rising edges of the system clock. For more details, please consult the IDT71589 datasheet.

The SIMM package allows 80 leads to be placed on a package 4.65 inches long by 0.56 inches tall. The IDT7MP6085 is 0.21 inches thick and the IDT7MP6087 is 0.35 inches thick. All inputs and outputs of the IDT7MP6085/7MP6087 are TTL-compatible and operate from a single 5V power supply.

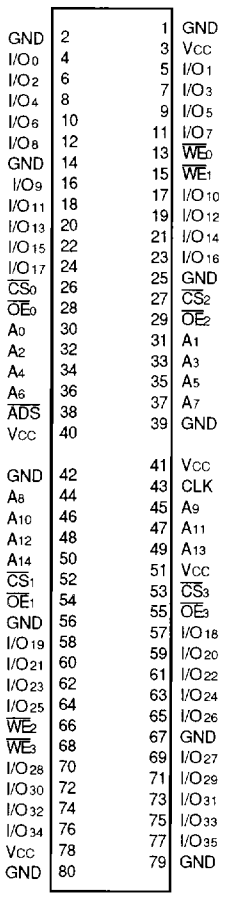
FUNCTIONAL BLOCK DIAGRAM



2834 drw 01

The IDT logo is a registered trademark and CacheRAM is a trademark of Integrated Device Technology, Inc.
All others are trademarks of their respective companies

PIN CONFIGURATION



2834 drw 02

SIMM
TOP VIEW

PIN NAMES

A0–A14	Address Inputs
I/O0–I/O35	Data Input/Output
$\overline{CS}_{0-3}$	Word Chip Select/Count Enable
$\overline{WE}_{0-3}$	Byte Write Enables
$\overline{OE}_{0-3}$	Word Output Enables
ADS	Address Status
CLK	System Clock
GND	Ground
VCC	Power

2834 tbl 01

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Value	Unit
VTERM	Terminal Voltage with Respect to GND	–0.5 to +7.0	V
TA	Operating Temperature	0 to +70	°C
TBIAS	Temperature Under Bias	–10 to +85	°C
TSTG	Storage Temperature	–55 to +125	°C
IOUT	DC Output Current	50	mA

NOTE: 2834 tbl 02

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	5.0V ± 5%

2834 tbl 03

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	4.75	5.0	5.25	V
GND	Supply Voltage	0	0	0.0	V
VIH	Input High Voltage	2.2	—	6.0	V
VIL	Input Low Voltage	–0.5(1)	—	0.8	V

NOTE: 2834 tbl 04

1. VIL = –3.0V for pulse width less than 5ns.

CAPACITANCE(1)

(TA = +25°C, f = 1.0 MHz)

Symbol	Parameter(1)	Condition	7MP6085/7 Max.	Unit
CIN	Input Capacitance ($\overline{CS}$, $\overline{OE}$, $\overline{WE}$)	VIN = 0V	20	pF
CIN	Input Capacitance (Address, CLK, $\overline{ADS}$)	VIN = 0V	42/70	pF
CI/O	I/O Capacitance	VOUT = 0V	13/20	pF

NOTE: 2834 tbl 05

1. This parameter is guaranteed by design but not tested.

TRUTH TABLE[1]

CLK	Previous $\overline{ADS}$	$\overline{ADS}$	Address	$\overline{WE}$	$\overline{CS}$	$\overline{OE}$	I/O	Function
↑	H	L	Valid Input	X	X	—	—	Preset Address Counter
↑	X	H	—	—	—	—	—	Ignore External Address Pins
↑	L	X	—	—	—	—	—	Ignore External Address Pins
↑	X	H	—	—	L	—	—	Sequence Address Counter
↑	L	X	—	—	L	—	—	Sequence Address Counter
↑	X	H	—	—	H	—	—	Suspend Address Sequencing
↑	L	X	—	—	H	—	—	Suspend Address Sequencing
—	—	—	—	—	—	H	High-Z	Outputs Disabled
—	—	—	—	H	—	L	$DATA_{OUT}$	Read
↑	X	H	—	L	L	H	$DATA_{IN}$	Write
↑	L	X	—	L	L	H	$DATA_{IN}$	Write
—	—	—	—	L	L	L	—	Not Allowed

2834 tbl 06

NOTE:
1. H = HIGH, L = LOW, X = Don't Care, "–" = Unrelated, High-Z = High-impedance.

DC ELECTRICAL CHARACTERISTICS[1]

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	Min.	7MP6085/7 Max.	Unit
$\|I_{LI}\|$	Input Leakage Current (Address, CLK, $\overline{ADS}$)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	40/80	µA
$\|I_{LI}\|$	Input Leakage Current ($\overline{CS}$, $\overline{OE}$)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	—	20	µA
$\|I_{LI}\|$	Input Leakage Current (Data, $\overline{WE}$)	V_{CC} = 5.5V, V_{IN} = 0V to V_{CC}	–	10/20	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CS}$ = V_{IH}, V_{OUT} = 0V to V_{CC}, V_{CC} = Max.	—	10/20	µA
V_{OL}	Output Low Voltage	I_{OL} = 8mA, V_{CC} = Min.	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = –4mA, V_{CC} = Min.	2.4	—	V

2834 drw 07

NOTE:
1. Specifications apply to both the IDT7MP6085 and IDT7MP6087 unless otherwise noted.

7

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V ± 5%, T_A = 0°C to 70°C)

Symbol	Parameter	Test Condition	IDT7MP6085	IDT7MP6087	Unit
I_{CC1}	Operating Power Supply Current	$\overline{CS} \le V_{IL}$ Outputs Open V_{CC} = Max., f = 0[1]	520	1040	mA
I_{CC2}	Dynamic Operating Current	$\overline{CS} \le V_{IL}$ Outputs Open V_{CC} = Max., f = f_{MAX}[1]	960	1920	mA

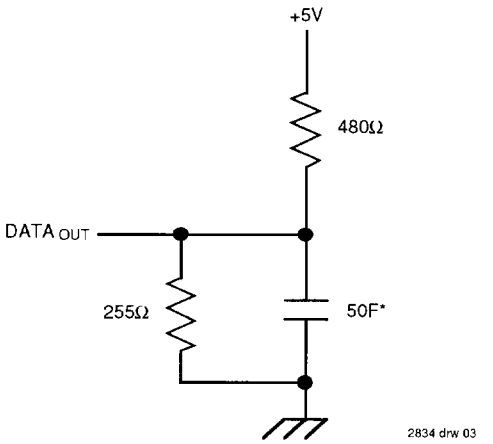
2834 tbl 08

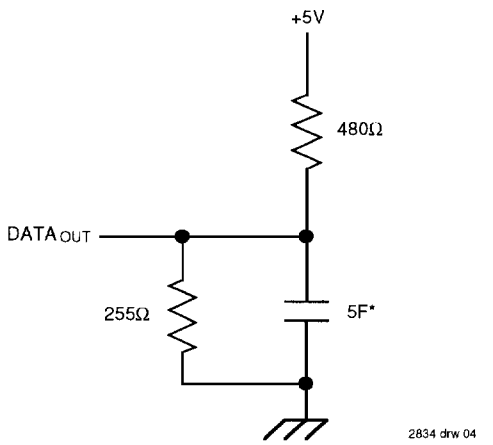
NOTE:
1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycles of $1/t_{RC}$. f = 0 means no input lines change.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	See Figures 1 & 2

2834 tbl 09





*including scope and jig

Figure 1. Output Load

Figure 2. Output Load (for tOHZ, tCHZ, tOLZ and tCLZ)

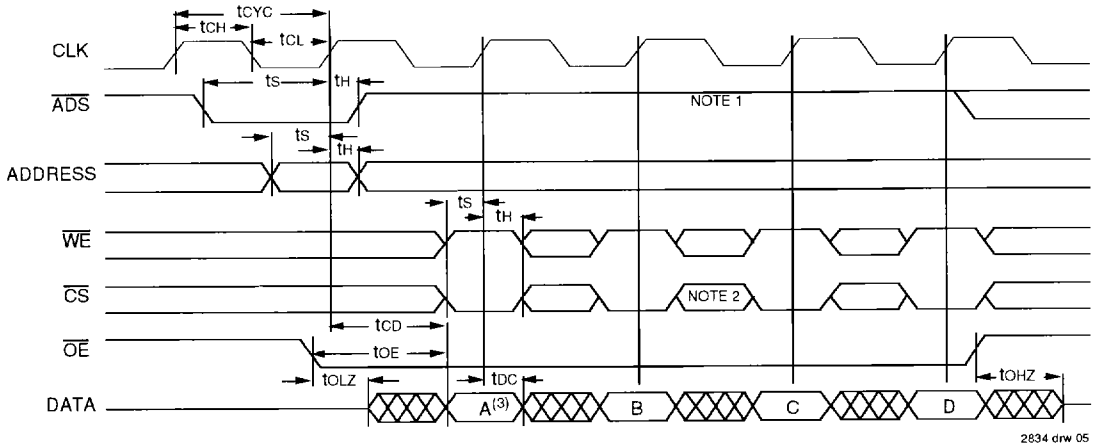
AC ELECTRICAL CHARACTERISTICS (VCC = 5.0V ± 5%, TA = 0° to +70°C)

Symbol	Parameter	7MP6085/6087SxxM 40 MHz Min.	40 MHz Max.	33 MHz Min.	33 MHz Max.	Unit
tCYC	Clock Cycle Time	25	—	30	—	ns
tCH	Clock Pulse HIGH	10	—	11	—	ns
tCL	Clock Pulse LOW	10	—	11	—	ns
tS1	Set-up Time ($\overline{ADS}$, $\overline{WE}$, $\overline{CS}$)	4	—	4	—	ns
tS2	Set-up Time (Address, Input Data)	5	—	5	—	ns
tH1	Hold Time ($\overline{CS}\downarrow$ Input Data)	1	—	1	—	ns
tH2	Hold Time ($\overline{CS}\uparrow$, $\overline{WE}$, Address)	2	—	2	—	ns
tADSH	Hold Time ($\overline{ADS}$)	3	—	3	—	ns
tCD	Clock to Data Valid	—	19	—	24	ns
tDC	Data Valid After Clock	4	—	4	—	ns
tOE	Output Enable to Output Valid	—	8	—	9	ns
tOLZ	Output Enable to Output in Low-Z[1,2]	2	—	2	—	ns
tOHZ	Output Disable to Output in High-Z[1,2]	—	8	—	9	ns

NOTES:
1. Transition is measured ±200mV from low or high-impedance voltage with load (Figure 2).
2. This parameter is guaranteed, but not tested.

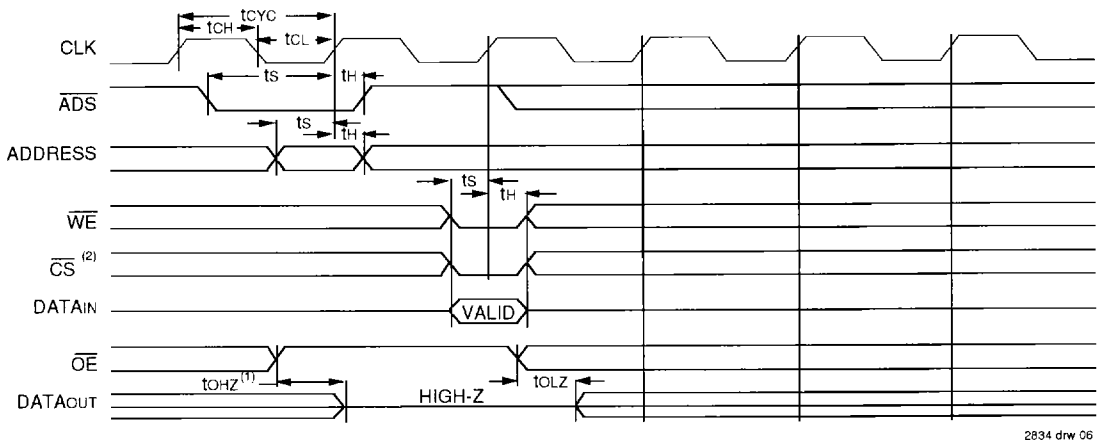
2834 tbl 10

TIMING WAVEFORM OF BURST READ CYCLE



NOTES:
1. If $\overline{ADS}$ goes LOW during a burst cycle, a new address will be loaded and another burst cycle will be started.
2. If $\overline{CS}$ is taken inactive during a burst read cycle, the burst counter will discontinue counting until $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters ts and tH.
3. A-Data from input address. B-Data from input address except A_0 is now $\overline{A}_0$. C-Data from input address except A_1 is now $\overline{A}_1$. D-Data from input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.

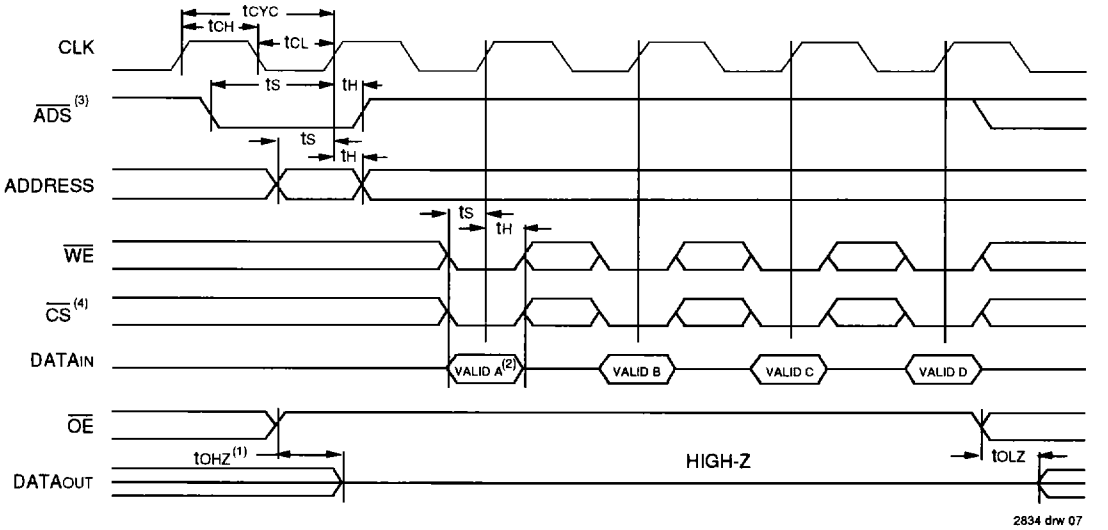
TIMING WAVEFORM OF WRITE CYCLE



NOTES:
1. $\overline{OE}$ Must be taken inactive at least as long as t_{OHZ} + ts before the second rising clock edge of write cycle.
2. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

7

TIMING WAVEFORM OF BURST WRITE CYCLE

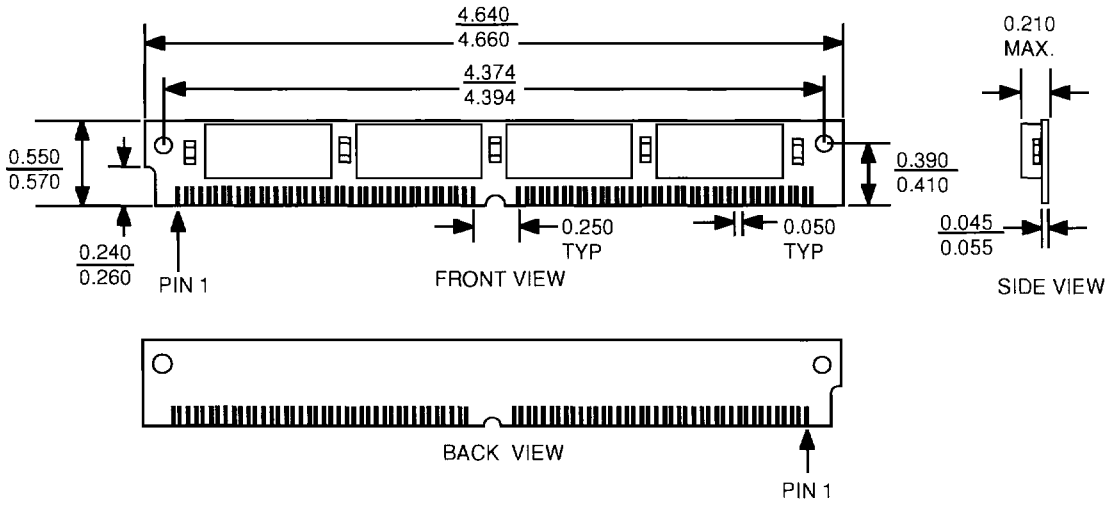


NOTES:

1. $\overline{OE}$ Must be taken inactive at least as long as $t_{OHZ} + t_S$ before the second rising clock edge of write cycle.
2. A-Data to be written to original input address.
   B-Data to be written to original input address except A_0 is now $\overline{A}_0$.
   C-Data to be written to original input address except A_1 is now $\overline{A}_1$.
   D-Data to be written to original input address except A_0 and A_1 are now $\overline{A}_0$ and $\overline{A}_1$.
3. If $\overline{ADS}$ goes low during a burst cycle, a new address will be loaded, and another burst cycle will be started.
4. If $\overline{CS}$ is taken inactive during a burst write cycle the burst counter will discontinue counting until the $\overline{CS}$ input again goes active. The timing of the $\overline{CS}$ input for this control of the burst counter must satisfy setup and hold parameters t_S and t_H. $\overline{CS}$ timing is the same as any synchronous signal when used to block writes or to stop the burst count sequence.

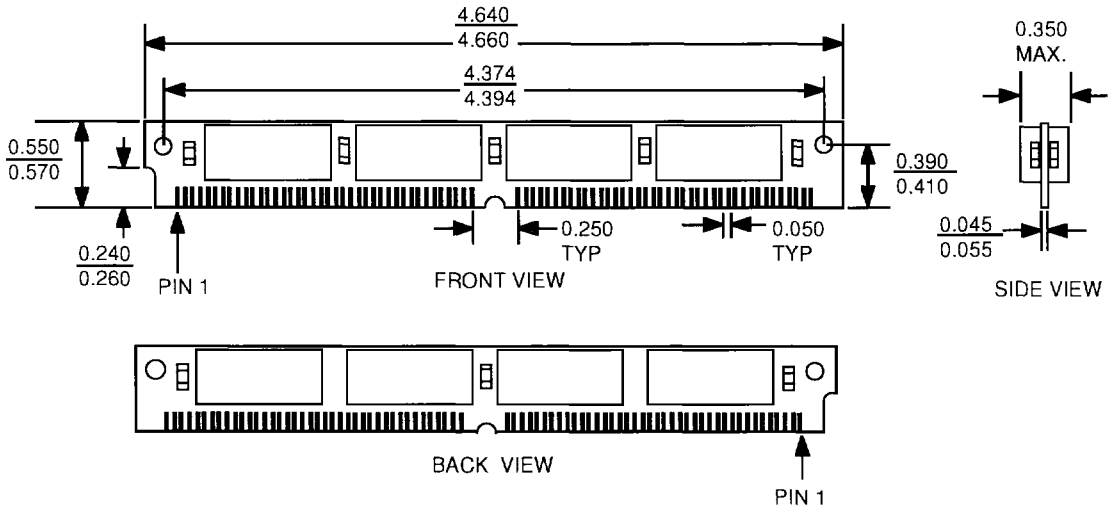
PACKAGE DIMENSIONS

IDT7MP6085



2834 drw 08

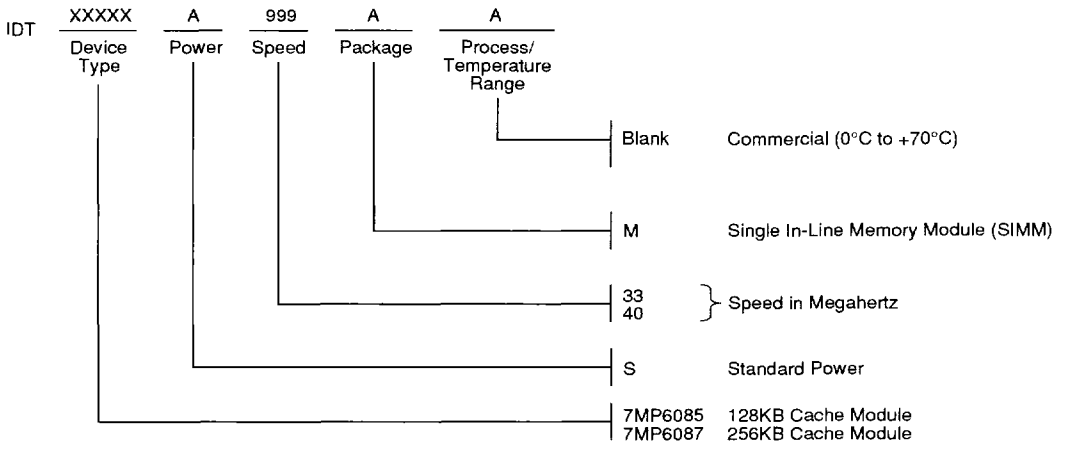
IDT7MP6087



2834 drw 09

7

ORDERING INFORMATION



2834 drw 10