■ FLASH MEMORIES (Continued)

☆ New product
★ Under development

<Boot Block*4 Smart Voltage Flash Memory>

Capacity	Bit configuration	Block configuration		Model No.	Access time (ns) MAX. (Vcc = 5 V)	Supply voltage	Read current (mA) MAX. (f = 8 MHz, Vcc = 5 V)	Standby current (μA) MAX.	Operating temperature (°C)	Package
4M	× 16	4k x 2 (boot), 4k × 6 (parameter), 32k × 7 (main)	Top boot	★ LH28F400BGE/N/B-TL85/TL12	85/120	Smart voltage*3 (2.7 V read, write, erase available)	50	100	0 to 70	48TSOP(I)*1/44SOP/48FBGA(CSP)*9
				★ LH28F400BGHE/B-TL85/TL12	85/120		50	100	–40 to 85	48TSOP(I)*1/48FBGA(CSP)*9
			Bottom boot	★ LH28F400BGE/N/B-BL85/BL12	85/120		50	100	0 to 70	48TSOP(I)*1/44SOP/48FBGA(CSP)*9
				★ LH28F400BGHE/B-BL85/BL12	85/120		50	100	–40 to 85	48TSOP(I)*1/48FBGA(CSP)*9
8M	× 16	4k x 2 (boot), 4k × 6 (parameter), 32k × 15 (main)	Top boot	☆ LH28F800BGE/R/N/B-TL85/TL12	85/120	Smart voltage*3 (2.7 V read, write, erase available)	50	100	0 to 70	48TSOP(I)*1/48TSOP(I)*2/44SOP*/48FBGA(CSP)*10
				☆ LH28F800BGHE/R/B-TL85/TL12	85/120		50	100	–40 to 85	48TSOP(I)*1/48TSOP(I)*2/48FBGA(CSP)*10
			Bottom boot	☆ LH28F800BGE/R/N/B-BL85/BL12	85/120		50	100	0 to 70	48TSOP(I)*1/48TSOP(I)*2/44SOP*/48FBGA(CSP)*10
				☆ LH28F800BGHE/R/B-BL85/BL12	85/120		50	100	–40 to 85	48TSOP(I)*1/48TSOP(I)*2/48FBGA(CSP)*10
16M	× 16	4k x 2 (boot), 4k × 6 (parameter), 32k × 31 (main)	Top boot	★ LH28F160BGE/R/B-TTL10/TTL12	100*7/120*7	Smart 3*5 (2.7 V read, write, erase available)	25*7	50	0 to 70	48TSOP(I)*1/48TSOP(I)*2/60FBGA(CSP)
				★ LH28F160BGHE/R/B-TTL10/TTL12	100*7/120*7		25*7	50	–40 to 85	48TSOP(I)*1/48TSOP(I)*2/60FBGA(CSP)
			Bottom boot	★ LH28F160BGE/R/B-BTL10/BTL12	100*7/120*7		25*7	50	0 to 70	48TSOP(I)*1/48TSOP(I)*2/60FBGA(CSP)
				★ LH28F160BGHE/R/B-BTL10/BTL12	100*7/120*7		25*7	50	–40 to 85	48TSOP(I)*1/48TSOP(I)*2/60FBGA(CSP)
			Top boot	★ LH28F160BGE/R/B-TTLL12/TTLL15	120*8/150*8	Smart 3L*6 (2.4 V read, write, erase available)	20*8	20	0 to 70	48TSOP(I)*1/48TSOP(I)*2/60FBGA(CSP)
				★ LH28F160BGHE/R/B-TTLL12/TTLL15	120*8/150*8		20*8	20	–40 to 85	48TSOP(I)*1/48TSOP(I)*2/60FBGA(CSP)
			Bottom boot	★ LH28F160BGE/R/B-BTLL12/BTLL15	120*8/150*8		20*8	20	0 to 70	48TSOP(I)*1/48TSOP(I)*2/60FBGA(CSP)
				★ LH28F160BGHE/R/B-BTLL12/BTLL15	120*8/150*8		20*8	20	–40 to 85	48TSOP(I)*1/48TSOP(I)*2/60FBGA(CSP)

*1 Normal bend *2 Reverse bend
*3 Smart voltage: Power supply is made an arbitrary selection among Vcc = 3.3 V, Vpp = 3.3 V/Vcc = 3.3 V, Vpp = 5 V/Vcc = 3.3 V, Vpp = 12 V/ Vcc = 5 V, Vpp = 5 V/Vcc = 5 V, Vpp = 12 V without using control signals.
*4 Boot block architecture: Well-balanced block architecture to store system program. This architecture consists of small size blocks (4k-word) for boot code storage and parameter storage and target size symmetric blocks (32k-word) for main code storage.
*5 Smart 3: Power supply is made an arbitrary selection between Vcc = 2.7 to 3.6 V, Vpp = 2.7 to 3.6 V/Vcc = 2.7 to 3.6 V, Vpp = 12 V without using control signals.
*6 Smart 3L: Power supply is made an arbitrary selection between Vcc = 2.4 to 3.0 V, Vpp = 2.4 to 3.0 V/Vcc = 2.4 to 3.0 V, Vpp = 12 V without using control signals.
*7 Vcc = 3.3 V *8 Vcc = 2.7 V *9 Nominal dimensions: 6 x 8 mm *10 Nominal dimensions: 8 x 8 mm

<Fast Programming Flash Memory (with Fast Write Function*3)>

Capacity	Bit configuration	Block configuration	Model No.	Access time (ns) MAX. (Vcc = 3.3 V)	Supply voltage (V)	Read current (mA) MAX. (f = 8 MHz)	Standby current (μA) MAX.	Operating temperature (°C)	Package
16M	×8/×16	64kB	☆ LH28F160S3D/T/R/NS/B-L10/L13	100/130	Smart voltage 3*4 (2.7 V read, write, erase available)	25	100	0 to 70	64SDIP/56TSOP(I)*1/56TSOP(I)*2/56SSOP/64FBGA(CSP)
			☆ LH28F160S3HD/T/R/NS/B-L10/L13	100/130				–40 to 85	64SDIP/56TSOP(I)*1/56TSOP(I)*2/56SSOP/64FBGA(CSP)
			★ LH28F160S5D/T/R/NS/B-L70/L10	70/100	Smart 5*5	50	100	0 to 70	64SDIP/56TSOP(I)*1/56TSOP(I)*2/56SSOP/64FBGA(CSP)
			★ LH28F160S5HD/T/R/NS/B-L70/L10	70/100				–40 to 85	64SDIP/56TSOP(I)*1/56TSOP(I)*2/56SSOP/64FBGA(CSP)
32M	×8/×16	64kB	★ LH28F320S3NS/B-L11/L14	110/140	Smart 3*4 (2.7 V read, write, erase available)	25	100	0 to 70	56SSOP/80FBGA(CSP)
			★ LH28F320S3HNS/B-L11/L14	110/140				–40 to 85	56SSOP/80FBGA(CSP)
			★ LH28F320S5NS/B-L90/L12	90*6/120*6	Smart 5*5	50	100	0 to 70	56SSOP/80FBGA(CSP)
			★ LH28F320S5HNS/B-L90/L12	90*6/120*6				–40 to 85	56SSOP/80FBGA(CSP)

*1 Normal bend
*2 Reverse bend
*3 Fast write function: Available with built-in two pages of 32-byte page buffer
*4 Smart 3: Power supply is made an arbitrary selection between Vcc = 3 V, Vpp = 3 V/Vcc = 3 V, Vpp = 5 V without using control signals.
*5 Smart 5: Vcc = 5 V, Vpp = 5V
*6 Vcc = 5 V

<Dual Work*2 Flash Memory>

Capacity	Bit configuration	Block configuration	Model No.	Access time (ns) MAX. (Vcc = 5 V)	Supply voltage (V)	Read current (mA) MAX. (f = 8 MHz)	Standby current (μA) MAX.	Operating temperature (°C)	Package
8M	×8	64kB	☆ LH28F008SCHSD-ZL	150	Vcc = 2.9 to 3.3V, Vpp = 2.9 to 3.3V (2.7 V read available)	12	100	–40 to 85	48TSOP(I)*1*3
16M	×16	32k words	☆ LH28F160SGED-L10	100	Smart voltage*4 (2.7 V read available)	50	100	–40 to 85	48TSOP(I)*1
32M	×8/×16	64kB	☆ LH28F320S3TD-L10	100	Smart 3*5	30	100	0 to 70	56TSOP(I)*1

*1 Normal bend
*2 Dual work: Write/erase and read can be operated simultaneously. Impossible to perform read from both banks at a time.
*3 Nominal dimensions:10 × 14 mm, pin pitch: 0.4 mm
*4 Smart voltage: Power supply is made an arbitrary selection among Vcc = 3.3 V, Vpp = 3.3 V / Vcc = 3.3V, Vpp = 5 V / Vcc = 3.3 V, Vpp =12 V / Vcc = 5V, Vpp = 5 V / Vcc = 5V, Vpp = 12 V without using control signals.
*5 Smart 3: Power supply is made an arbitrary selection between Vcc = 3.3 V (2.7 V MIN.), Vpp = 3.3 V (2.7 V MIN.)/Vcc = 3.3 V (2.7 V MIN.), Vpp = 5 V without using control signals.