Quad 8-Bit Nonvolatile DACPOT™ Electronic Potentiometer With a Mute Control Input

FEATURES

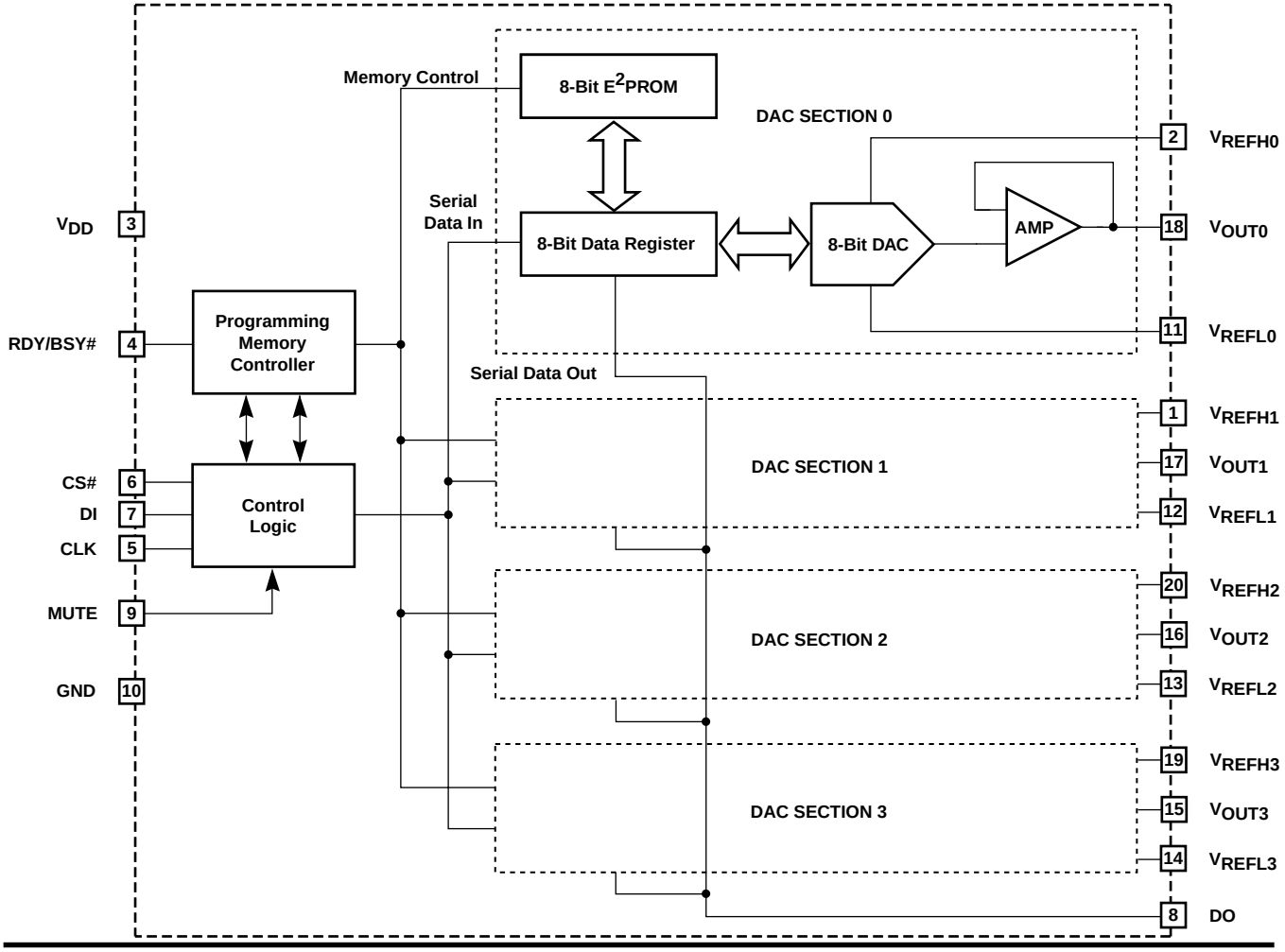
- **Four 8-Bit DACs**
  - **— Differential Non-linearity: ±0.5LSB max**
  - **— Integral Non-Linearity Error: ±1LSB max**
- **Each DAC has Independent Reference Inputs**
  - **— Output Buffer Amplifiers Swing Rail-to-Rail**
  - **— Ground to V_{DD} Reference Input Range**
- **Each DAC's Digital Inputs Maintained in EEPROM**
- **Power-On Reset Reloads Registers with Non-volatile Data**
- **Simple Serial Interface for Reading and Writing DAC values, SPI™ and QSPI™ compatible.**
- **Fully operational from 2.7V to 5.5V**
- **Low Power, 4mW max at +5V**

OVERVIEW

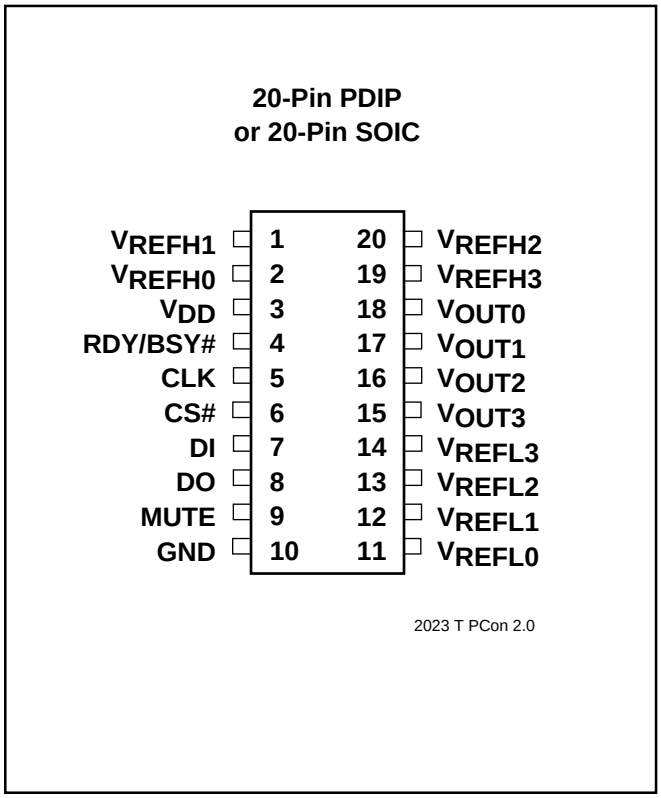
The S9418 DACPOT™ is a serial input, voltage output, quad 8-bit digital to analog converter (DAC). The S9418 operates from a single 2.7V to 5.5V supply. Internal precision buffers swing rail-to-rail and the reference input range includes both ground and the positive supply.

The S9418 integrates four 8-bit DACs and their associated circuits which include; an enhanced unity gain operational amplifier output, an 8-bit data latch, an 8-bit non-volatile register and an industry standard serial interface for reading and writing data to the DACs' data latches and registers. The DACs are independently programmable and each has its own electrically isolated Vreference inputs.

BLOCK DIAGRAM



PINOUT and SIGNAL DEFINITION



Pin	Name	Function
1, 2 19, 20	V_{REFH}	Vreference High: V_{REFH} - V_{DD} > V_{REFL}
3	V_{DD}	Power Supply Voltage
4	RDY/ BSY#	Ready/Busy#: open drain output indicating status of nonvolatile write operations
5	CLK	Clock Input Pin: used for serial data communication
6	CS#	Chip Select: When high deselects the device and places it in a low power mode
7	DI	Data Input: serial data input pin
8	DO	Data Output: serial data output pin
9	MUTE	When active forces V_{OUT} to V_{REFL}
10	GND	Power Supply Ground
11, 12 13, 14	V_{REFL}	Vreference Low
15, 16 17, 18	V_{OUT}	DAC Output: buffered D to A converter output

The analog outputs of the S9418 can be programmed to any one of 256 individual voltage steps. Each step value is 1/256th of the voltage differential between V_{REFH} and V_{REFL} of the respective DAC. Once programmed these settings can be retained in nonvolatile memory during all power conditions and will be automatically recalled upon a power-up sequence. Each DAC can be independently read without affecting the output voltage during the read cycle. In addition each output can be adjusted an unlimited number of times without altering the value stored in the nonvolatile memory.

DEVICE OPERATION

Analog Section

The S9418 is an 8-bit, voltage output digital-to-analog converter (DAC). The DAC consists of a resistor network that converts 8-bit digital inputs into equivalent analog output voltages in proportion to the applied reference voltage.

Reference inputs

The voltage differential between the V_{REFL} and V_{REFH} inputs sets the full-scale output voltage for its respective DAC. V_{REFL} must be equal to or greater than ground (positive voltage). V_{REFH} must be greater (more positive) than V_{REFL} or equal to V_{DD}.

Output Buffer Amplifiers

The voltage outputs are from precision unity-gain followers that can slew up to 1V/µs. The outputs can swing from V_{REFL} to V_{REFH}. With a 0V to 5V output transition the amplifier outputs typically settle to 1LSB in 40µs.

DIGITAL INTERFACE

The S9418 employs a common 4-wire serial interface. It is comprised of a Clock (CLK), Chip Select (CS#), Data input (DI) and Data output (DO). Data is clocked into the device on the clock's rising edge and out of the device on the clock's falling edge. Data is shifted in and out MSB first. DO only becomes active after the device has been selected and after a valid read command and address has been received.

All data transfers are initiated after CS# goes low and a logic '1' is clocked into the device. This first data transfer is the start bit and must precede all operations. Following the start bit are two command bits used to specify which of four commands to execute. The next two bits are the address bits used to select one of the four DACs. The action of the next eight clock cycles will be dependent upon the command issued.

Start	C_1	C_0	A_1	A_0	Command
1	0	0	A	A	NV Write Enable
1	0	1	A	A	Write — Data In
1	1	0	A	A	Read — Data Out
1	1	1	A	A	Recall

TABLE 1.

Internally there are four DACs and associated with each are two registers. There is one data register that is used by the DAC to hold the digital value it converts. There is also one nonvolatile register that holds the default value that can be recalled into the data register during power-up or by executing the Recall command.

READ

Read operations are initiated by taking CS# low and clocking in a start bit followed by the read command and the address of the data register to be read. The next eight clocks will output on the DO pin the contents of the selected data register. This read will not affect the contents of the register or the output of the DAC. Refer to Figure 1 for an illustration of the sequence of bus conditions for a read operation.

WRITE

Write operations are initiated by taking CS# low and clocking in a start bit followed by the write command and the address of the data register to be written. This action is followed by the host clocking eight bits of data into the register, MSB first. The output of the selected DAC will change as the last bit is clocked into the device. At this point the clock counter will reset the command register, requiring a full sequence to be initiated in order to write to the DAC again. Refer to Figure 2 for an illustration of the sequence of bus conditions for a write operation.

NOTE: *This write operation does not affect the contents of the nonvolatile register. Therefore, the nonvolatile register can contain the power-on default settings (e.g. volume), and the write DAC command can be used to make situational adjustments.*

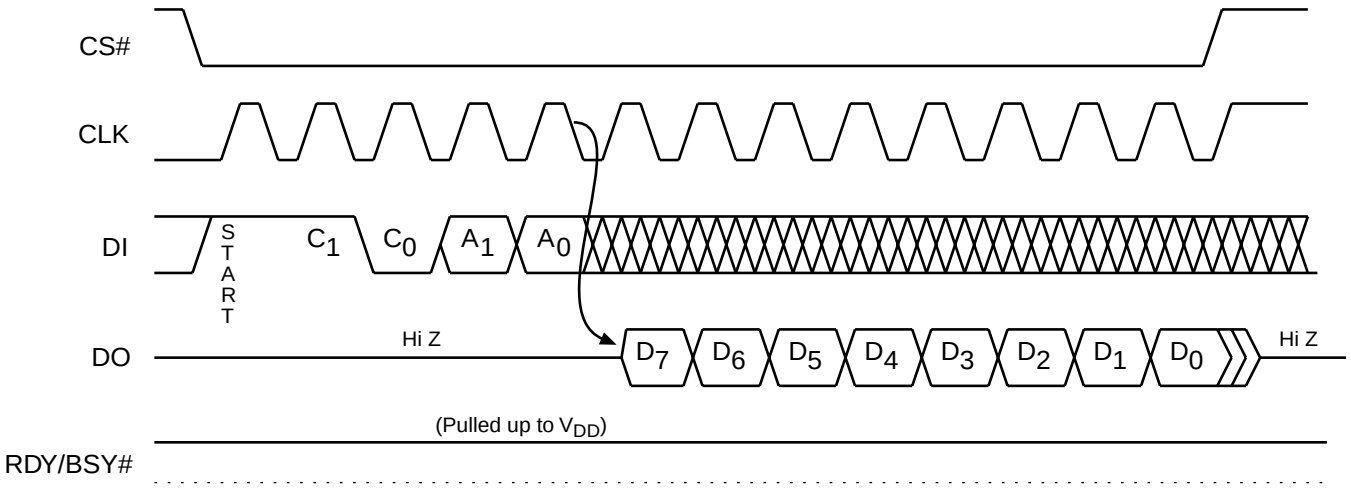


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FIGURE 1. READ SEQUENCE

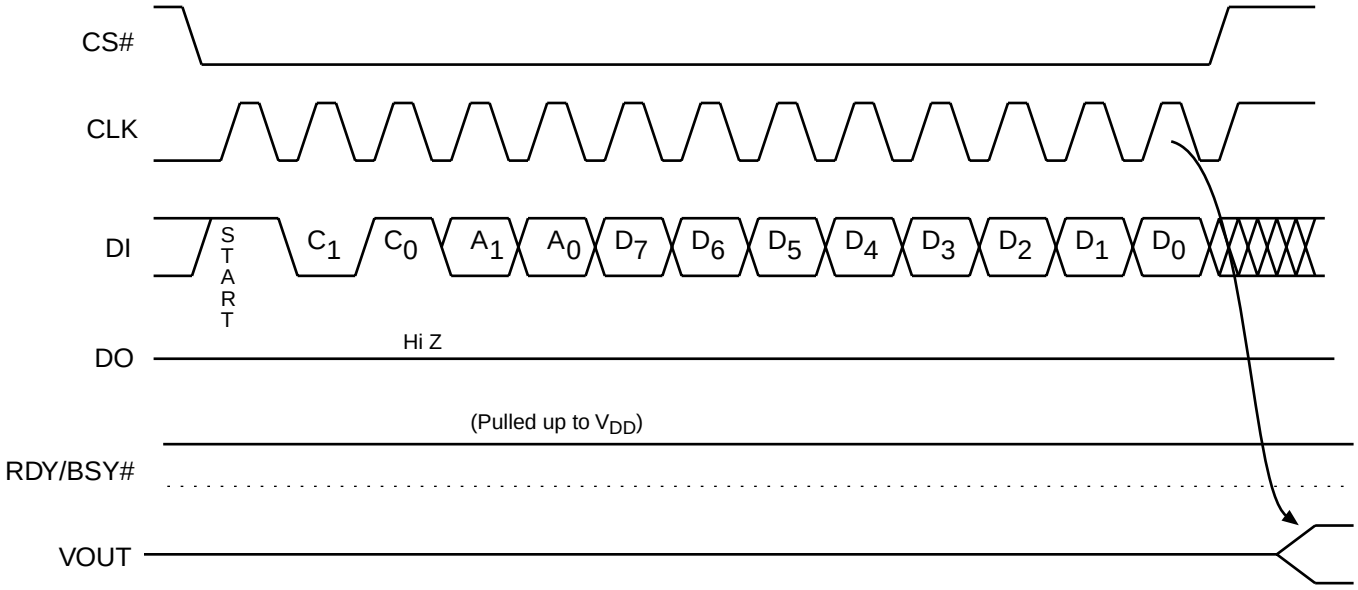

FIGURE 2. WRITE SEQUENCE

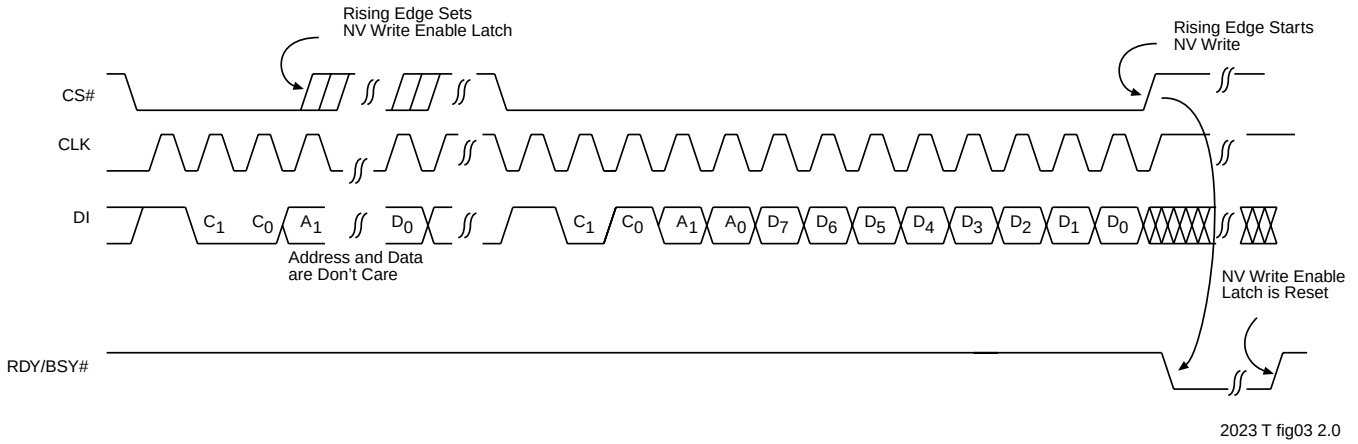

FIGURE 3. NONVOLATILE WRITE SEQUENCE

NONVOLATILE WRITE

A nonvolatile write is a two step operation: it is initiated by taking CS# low and clocking in a start bit followed by the NV Write Enable command. At this point the host can take CS# back high or continue clocking in data. This data is don't care and will be ignored by the S9418.

Next, the host takes CS# low again and issues a write command and address and then clocks in the eight data bits to be programmed. The host will then bring CS# high and the data will be latched into the data register and a nonvolatile write operation will commence.

The status of the nonvolatile write can be monitored on the RDY/BSY# pin. A logic low indicates the write is still in progress and the S9418 will not be accessible to the host; a logic high indicates the write has completed and the S9418 is ready for the next command. Refer to Figure 3 for an illustration of the sequence of bus conditions for a nonvolatile write operation.

RECALL COMMAND

The recall command will retrieve data from the selected nonvolatile register and write it into the data register of the associated DAC. This operation is initiated by taking CS# low and clocking in a start bit followed by the recall command and the address of the nonvolatile register to be recalled. The eight bits of data are don't care, so CS# can be taken high any time after the address bits are clocked in. Refer to Figure 4 for an illustration of the sequence of bus conditions for a Recall operation.

Power-On Recall

Whenever the S9418 is powered on, the V_{OUT} values will be returned to the analog equivalent of the data byte stored in the nonvolatile register.

MUTE Operation

The MUTE input is active high. Whenever the input is low the V_{OUT} will reflect the value in the data register. If MUTE is driven high the V_{OUT} outputs will be switched to V_{REFL}. Releasing the MUTE input returns the V_{OUT} outputs to the analog equivalent of the data register contents.

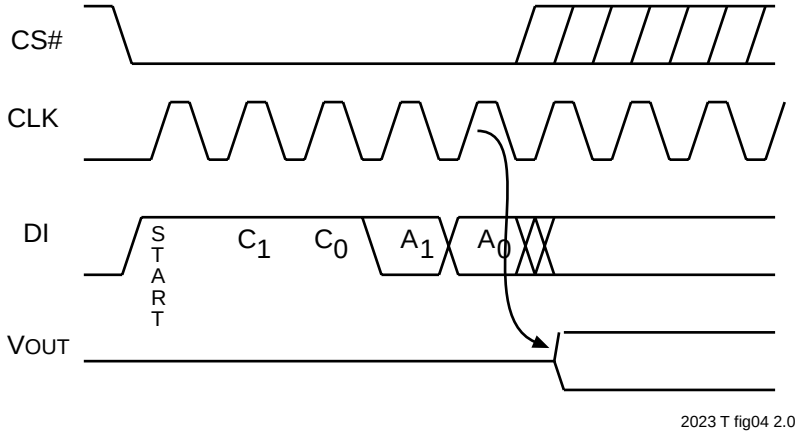

FIGURE 4. RECALL COMMAND SEQUENCE

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND ..... -0.5V to +7V
Digital Inputs to Gnd ..... -0.5V to V_{DD}+0.5V
Analog Inputs to ground ..... -0.5V to V_{DD}+0.5V
Digital Outputs to Gnd ..... -0.5V to V_{DD}+0.5V
Analog Outputs to Gnd ..... -0.5V to V_{DD}+0.5V
Temperature Under Bias ..... -55°C to +125°C
Storage Temperature ..... -65°C to +150°C
Lead Soldering (10 Sec Max) ..... 300°C

Stresses listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions outside those listed in the operational sections of this specification is not implied. Exposure to any absolute maximum rating for extended periods may affect device performance and reliability.

RECOMMENDED OPERATING CONDITIONS

Condition	Min	Max
Temperature	-40°C	+85°C
V_{DD}	+2.7V	+5.5V

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RELIABILITY CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Min	Max	Unit
V_{ZAP}	ESD Susceptibility	2000		V
I_{LTH}	Latch-up	100		mA
T_{DR}	Data Retention	100		Years
N_{END}	Endurance	1,000,000		Storage Cycles

DC ELECTRICAL CHARACTERISTICS (over recommended operating conditions unless otherwise specified)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I_{DD}	Supply current during store (note 1)	CS = V_{IL}		1.8	3.0	mA
I_{SB}	Standby supply current	CS = V_{IH}		260	500	µA
I_{IH}	Input leakage current	V_{IN} = V_{DD}		<1	10	µA
I_{IL}	Input leakage current	V_{IN} = 0V		<1	–10	µA
V_{IH}	High level input voltage	4.5V ≤ VCC ≤ 5.5V	2		V_{DD}	V
		VCC ≤ 4.5V	0.9 × V_{CC}		V_{DD}	V
V_{IL}	Low level input voltage	4.5V ≤ VCC ≤ 5.5V	0		0.8	V
		VCC ≤ 4.5V	0		0.1 × V_{CC}	V
V_{OH}	High level output voltage	IOH = –400µA	V_{DD} – 0.3			V
V_{OL}	Low level output voltage	IOL = 1mA, V_{DD} = 5V; IOL = 0.4mA, V_{DD} = 2.7V			0.4	V

Note 1: I_{DD} is the supply current drawn while the EEPROM is being updated.

Typical T_A = 25ºC and V_{CC} = 5.0V.

AC ELECTRICAL CHARACTERISTICS

V_{DD} = +4.5V to +5.5V, V_{REFH} = V_{DD}, V_{REFL} = 0V, T_A = -40°C to +85°C, unless otherwise specified

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
f_C	Clock Frequency		DC		1	MHz
t_{WH}	Minimum CLK High Time		500			ns
t_{WL}	Minimum CLK Low Time		300			ns
t_{CS}	Minimum CS High Time		150			ns
t_{CSS}	CS Setup Time		100			ns
t_{CSH}	CS Hold Time	C_L = 100pF See Note 1	0			ns
t_{SU}	Data In Setup Time		50			ns
t_H	Data In Hold Time		50			ns
t_V	Output Valid Time				150	ns
t_{HO}	Data Out Hold Time		0			ns
t_{DIS}	Output Disable Time			400		ns
t_{BUSY}	Write Cycle Time			3.3	5	ms

Notes: 1. All timing measurements are defined at the point of signal crossing V_{DD}/2.

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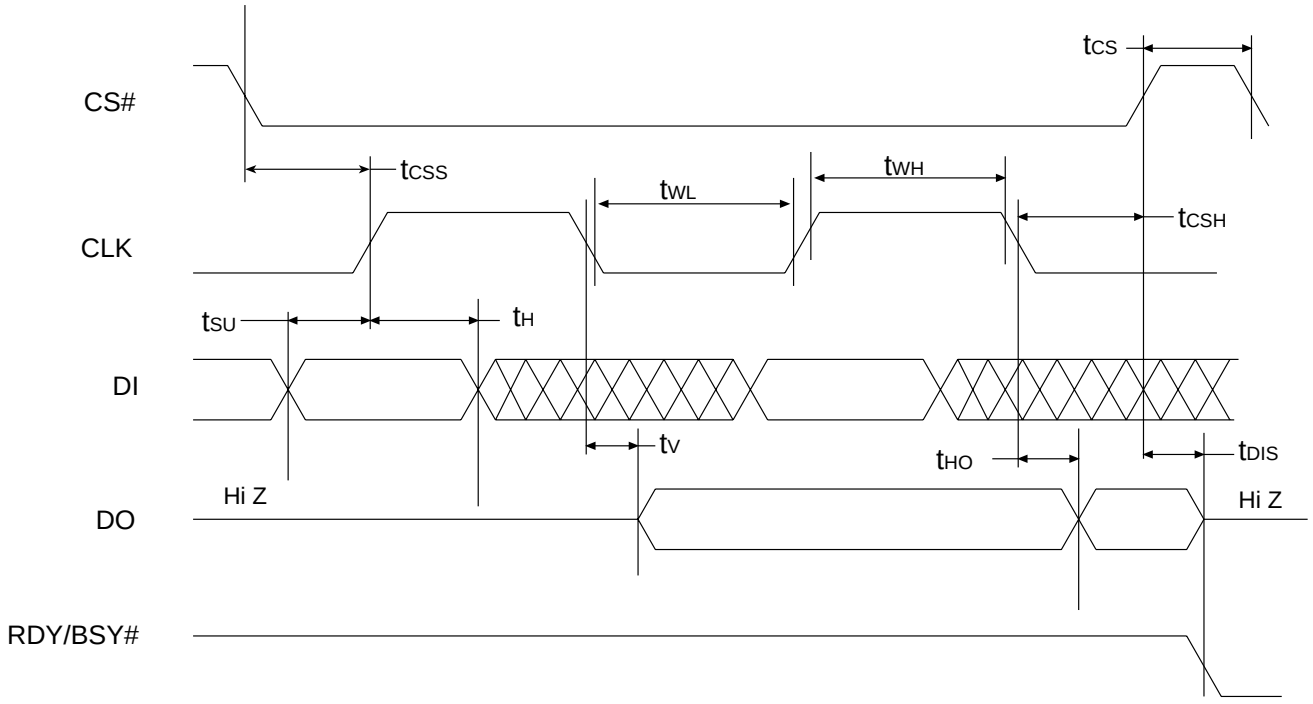

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FIGURE 5. AC TIMING DIAGRAM

DAC ELECTRICAL CHARACTERISTICS

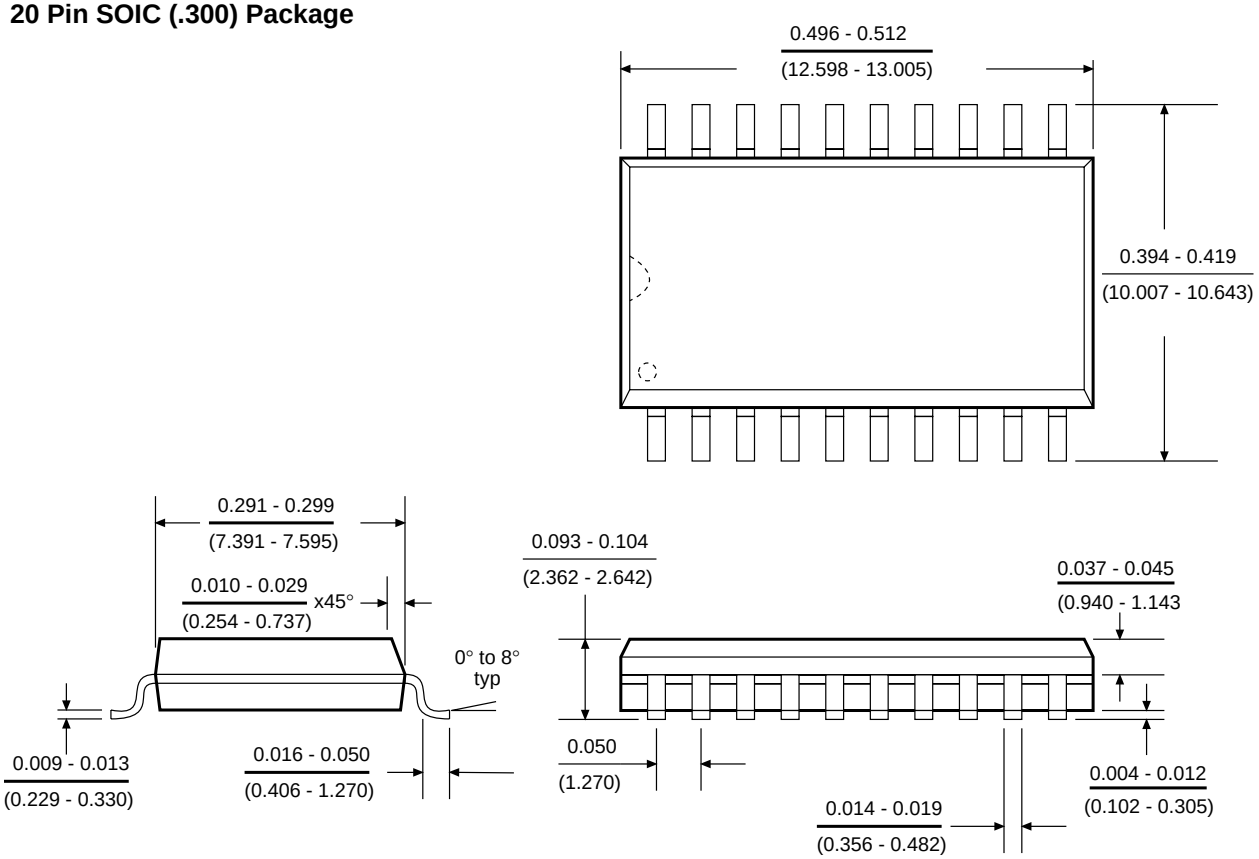
V_{DD} = 2.7V to 5.5V, V_{REFH} = VDD, V_{REFL} = 0V, T_A = –40ºC to 85ºC, unless otherwise specified

Property	Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Accuracy	INL	Integral non-linearity	I_{LOAD} = 100µA		0.5	±1	LSB
	DNL	Differential non-linearity	I_{LOAD} = 100µA (note 1)		0.1	±0.5	LSB
References	V_{REFH}	Input voltage		V_{REFL}			V
	V_{REFL}	Input voltage		GND			V
	R_{IN}	V_{REFH} to V_{REFL} resistance			40k		Ω
	TCR_{IN}	Temp. coefficient of R_{IN}			300	600	ppm/ºC
	ΔR_{IN}	Input resistance match			±0.5	±1	%
Analog Output	G_{EFS}	Full-scale gain error	D = FF_{HEX}			±1	LSB
	$V_{OUT}ZS$	Output offset voltage	D = 00_{HEX}	0	2.5	5	mV
	TCV_{OUT}	V_{OUT} temp. coeffiecient	V_{DD} = 5V, I_{LOAD} = 50µA (note 1)			50	µV/ºC
	I_L	Amp output load current		–200		1000	µA
	R_{OUT}	Amp output resistance	V_{DD} = V_{REFH} 5V 3V		10 20		Ω Ω
	PSRR	Power supply rejection	I_{LOAD} = 10µA			1	LSB/V
	t_S	DAC settling time to 1LSB	10pF 5V 10pF 3V		36 27		µs µs
	e_N	Amp output noise	f = 1kHz, V_{DD} = 5V		90		nV√Hz
	THD	Total harmonic distortion	V_{REFH} = 2.5V, V_{DD} = 5V, f = 1kHz, V_{IN} = $1V_{RMS}$		0.08		%
	BW	Bandwidth –3dB	V_{REFH} = 2.5V, V_{DD} = 5V, V_{IN} = $100mV_{RMS}$		300		kHz

Note 1: Guaranteed but not tested.

Typical T_A = 25ºC and V_{CC} = 5.0V.

20 Pin SOIC (.300) Package



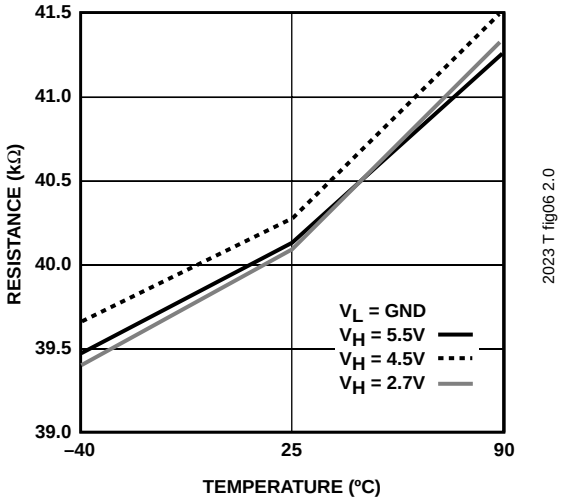
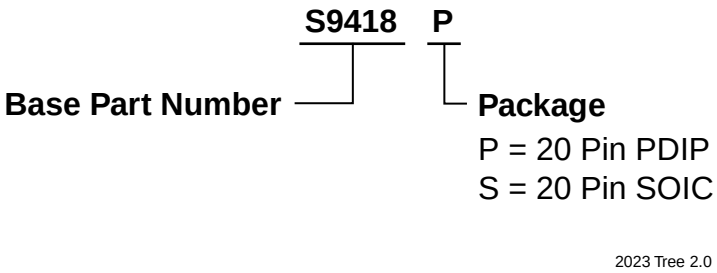


FIGURE 6. V_L TO V_H END-TO-END RESISTANCE OVER TEMPERATURE

ORDERING INFORMATION



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