NEC

MOS INTEGRATED CIRCUIT

μPD75036

4 BIT SINGLE-CHIP MICROCOMPUTER

The μPD75036 is a 75X series 4-bit single-chip microcomputer.

The μPD75036 is an expanded version of the μPD75028. It has ROM and RAM with a larger capacity.

The minimum instruction execution time of the μPD75036 is 0.95 μs. In addition to this high-speed capability, it contains an A/D converter and furnishes high-performance functions such as the serial bus interface (SBI) function that follows the NEC standard format, providing powerful features and high cost performance.

A built-in PROM product, μPD75P036, is also available. The μPD75P036 is suitable for small-scale production or experimental production in system development.

The following user's manual describes the details of functions. Be sure to read it before design.

μPD75028 User's Manual: IEU-694

FEATURES

- Variable instruction execution time advantageous to high-speed operation and power-saving:
  - 0.95 μs, 1.91 μs, or 15.3 μs (at 4.19 MHz when the main system selected)
  - 122 μs (at 32.768 kHz when the subsystem clock selected)
- Program memory (ROM) capacity: 16256 × 8 bits
- Data memory (RAM) capacity: 1024 × 4 bits
- Built-in A/D converter (8-bit resolution, successive approximation): 8 channels
- Powerful timer function: 4 channels
  - Usable for 16-bit integral A/D conversion and PWM output
- Built-in NEC standard serial bus interface (SBI)
- Very low-power clock operation allowed (5 μA TYP. at 3 V)

APPLICATIONS

Electric household appliances, air cooling/heating apparatus, cameras, and electronic measuring instruments

ORDERING INFORMATION

Part number	Package	Quality grade
μPD75036CW-×××	64-pin plastic shrink DIP (750 mil)	Standard
μPD75036GC-×××-AB8	64-pin plastic QFP (□14 mm)	Standard

Remark ××× is a mask ROM code number.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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Date Published October 1993 P
Printed in Japan

The mark ★ shows major revised points.

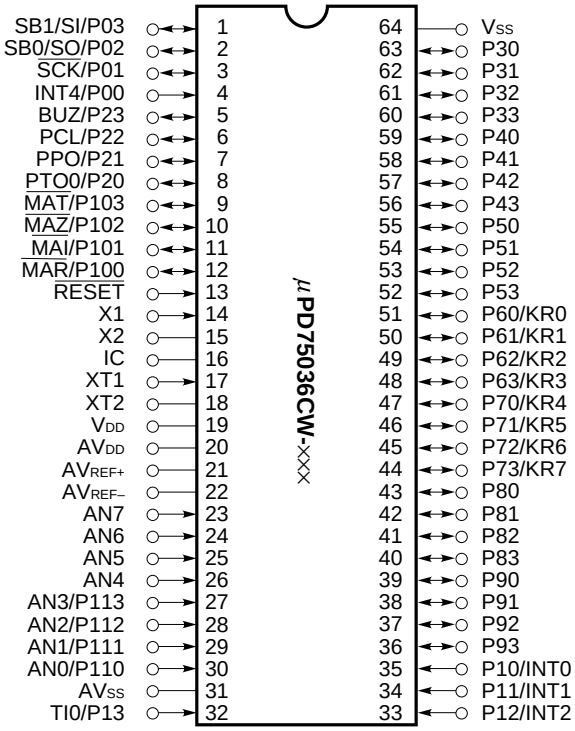
FUNCTIONS

Item		Function			
Instruction execution time		• 0.95, 1.91, 15.3 μs (Main system clock : 4.19 MHz operation) • 122 μs (Subsystem clock : 32.768 kHz operation)			
On-chip memory	ROM	16256 × 8 bits			
	RAM	1024 × 4 bits			
General register		• 4-bit manipulation : 8 • 8-bit manipulation : 4			
I/O port		48	12	CMOS input pins	• On-chip pull-up resistor by software : 27 • On-chip pull-down resistor by software: 4 • Direct LED driving: 4
			24	CMOS I/O pins	
			12	N-ch open-drain I/O pins	• Withstand voltage is 10 V • On-chip pull-up resistor by mask option • Direct LED driving: 4
Timer		4 channels	• Timer/event counter • Basic interval timer : Can be used as watchdog timer • Clock timer : Buzzer output enabled Multifunction timer : Can be used as timer, free-running timer or counter for integration A/D converter, or for PWM output		
Serial interface		• Three-wire serial I/O mode • Two-wire serial I/O mode • SBI mode			
Bit sequential buffer		16 bits			
Clock output		Φ, $f_X/2^3$, $f_X/2^4$, $f_X/2^6$ (Main system clock: 4.19 MHz operation)			
A/D converter		• 8-bit resolution × 8 channels (successive-approximation) • Capable of low-voltage operation: V_{DD} = 2.7 to 6.0 V			
Vectored interrupt		External : 3, Internal : 4			
Test input		External : 1, Internal : 1			
System clock oscillator		• Ceramic/crystal oscillator for main system clock oscillation • Crystal oscillator for subsystem clock oscillation			
Standby function		STOP/HALT mode			
★ Operating temperature range		–40 to +85 °C			
★ Operating voltage		2.7 to 6.0 V			
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (□14 mm)			

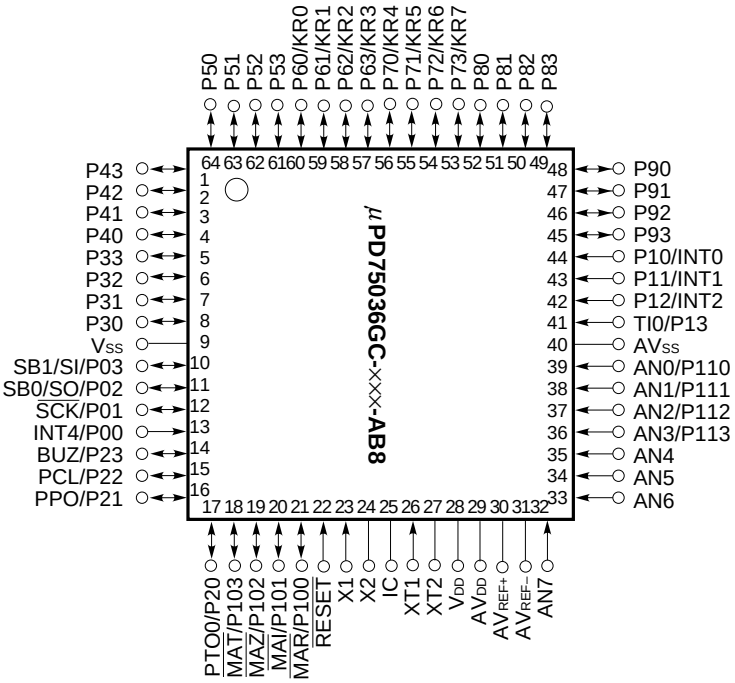
CONTENTS

1. PIN CONFIGURATIONS (TOP VIEW)

- **64-pin plastic shrink DIP**



- **64-pin plastic QFP**



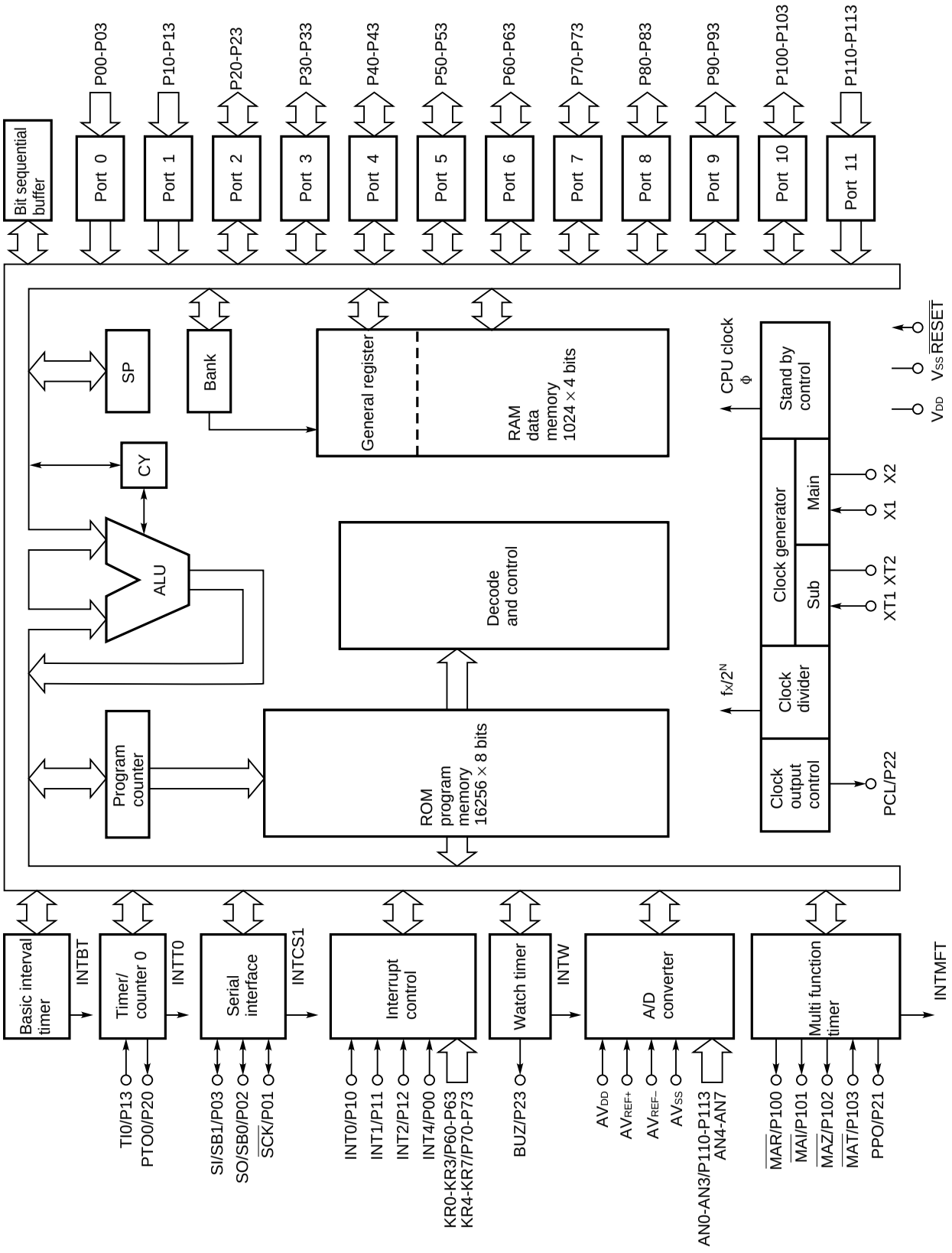
IC: Internally connected (Should be directly connected to V_{DD})

Pin names

P00-03	:	Port 0			:	Port 0
P10-13	:	Port 1			:	Port 1
P20-23	:	Port 2			:	Port 2
P30-33	:	Port 3			:	Port 3
P40-43	:	Port 4			:	Port 4
P50-53	:	Port 5			:	Port 5
P60-63	:	Port 6			:	Port 6
P70-73	:	Port 7			:	Port 7
P80-83	:	Port 8			:	Port 8
P90-93	:	Port 9			:	Port 9
P100-103	:	Port 10			:	Port 10
P110-113	:	Port 11			:	Port 11
KR0-7	:	Key Return			:	Key interrupt input
$\overline{SCK}$	:	Serial Clock			:	Serial clock I/0
SI	:	Serial Input			:	Serial data input
SO	:	Serial Output			:	Serial data output
$\overline{SB0, 1}$	:	Serial Bus 0, 1			:	Serial bus I/O
$\overline{RESET}$	:	Reset Input			:	Reset input
TI0	:	Timer Input 0			:	External event pulse input
PTO0	:	Programmable Timer Output 0			:	Timer/event counter output
BUZ	:	Buzzer Clock			:	Arbitrary frequency output
PCL	:	Programmable Clock			:	Clock output
INT0, 1, 4	:	External Vectored Interrupt 0, 1, 4			:	External vectored interrupt input
INT2	:	External Test Input 2			:	External test input
X1, 2	:	Main System Clock Oscillation 1, 2			:	Main system clock oscillation pin
XT1, 2	:	Subsystem Clock Oscillation 1, 2			:	Subsystem clock oscillation pin
$\overline{MAR}$	:	Reference Integration Control			:	Reverse integration signal output
$\overline{MAI}$	:	Integration Control	MFT A/D mode		:	Integration signal output	MFT A/D mode
$\overline{MAZ}$	:	Autozero Control			:	Autozero signal output	
$\overline{MAT}$	:	External Comparate Timing Input			:	External comparator signal input	
PPO	:	Programmable Pulse Output					
		... MFT timer mode			:	Pulse output ... MFT timer mode	
AN0-7	:	Analog Input 0-7			:	Analog input
AV_{REF+}	:	Analog Reference (+)			:	Analog reference voltage (+) input
AV_{REF-}	:	Analog Reference (-)			:	Analog reference voltage (-) input
AV_{DD}	:	Analog V_{DD}			:	A/D converter power supply input
AV_{SS}	:	Analog V_{SS}			:	A/D converter GND input
V_{DD}	:	Positive Power Supply			:	Main power supply pin
V_{SS}	:	Ground			:	GND potential pin

Remark MFT: Multifunction timer

2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 PORT PINS (1/2)

Pin	Input/ output	Shared pin	Function	8-bit I/O	When reset	I/O circuit type[Note 1]
P00	Input	INT4	4-bit input port (PORT0). For P01 - P03, pull-up resistors can be provided by software in units of 3 bits.	×	Input	Ⓑ
P01	I/O	$\overline{SCK}$				Ⓕ-A
P02	I/O	SO/SB0				Ⓕ-B
P03	I/O	SI/SB1				Ⓜ-C
P10	Input	INT0	With noise elimination function	×	Input	Ⓑ-C
P11		INT1	4-bit input port (PORT1). Pull-up resistors can be provided by software in units of 4 bits.			
P12		INT2				
P13		TI0				
P20	I/O	PTO0	4-bit I/O port (PORT2). Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P21		PPO				
P22		PCL				
P23		BUZ				
P30[Note 2]	I/O	–	Programmable 4-bit I/O port (PORT3). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P31[Note 2]		–				
P32[Note 2]		–				
P33[Note 2]		–				
P40 - P43[Note 2]	I/O	–	N-ch open-drain 4-bit I/O port (PORT4). A pull-up resistor can be provided for each bit (mask option). This open-drain port has a withstand voltage of 10 V.	○	High level (when pull-up resistors are provided) or high impedance	M
P50 - P53[Note 2]	I/O	–	N-ch open-drain 4-bit I/O port (PORT5). A pull-up resistor can be provided for each bit (mask option). This open-drain port has a withstand voltage of 10 V.		High level (when pull-up resistors are provided) or high impedance	M

Notes 1. The circle (◯) indicates the Schmitt trigger input.

2. Can directly drive the LED.

3.1 PORT PINS (2/2)

Pin	Input/ output	Shared pin	Function	8-bit I/O	When reset	I/O circuit type[Note 1]
P60	I/O	KR0	Programmable 4-bit I/O port (PORT6). I/O can be specified bit by bit. Pull-up resistors can be provided by software in units of 4 bits.	○	Input	Ⓕ-A
P61		KR1				
P62		KR2				
P63		KR3				
P70	I/O	KR4	4-bit I/O port (PORT7). Pull-up resistors can be provided by software in units of 4 bits.		Input	Ⓕ-A
P71		KR5				
P72		KR6				
P73		KR7				
P80-P83	I/O	–	4-bit I/O port (PORT8). Pull-up resistors can be provided by software in units of 4 bits.	×	Input	E-B
P90-P93	I/O	–	4-bit I/O port (PORT9). Pull-down resistors can be provided by software in units of 4 bits.		Input	E-D
P100[Note 2]	I/O	$\overline{\text{MAR}}$	N-ch open-drain 4-bit I/O port (PORT10). A pull-up resistor can be provided bit by bit (mask option). This open-drain port has a withstand voltage of 10 V.	×	High level (when pull-up resistors are provided) or high impedance	M
P101[Note 2]		$\overline{\text{MAI}}$				
P102[Note 2]		$\overline{\text{MAZ}}$				
P103[Note 2]		$\overline{\text{MAT}}$				
P110	Input	AN0	4-bit input port (PORT11)		Input	Y-A
P111		AN1				
P112		AN2				
P113		AN3				

Notes 1. The circle (◯) indicates the Schmitt trigger input.

2. Can directly drive the LED.

3.2 NON-PORT PINS (1/2)

Pin	Input/ output	Shared pin	Function		When reset	I/O circuit type[Note 1]
TI0	Input	P13	Input for receiving external event pulse signal for timer/event counter		–	Ⓑ-C
PTO0	I/O	P20	Timer/event counter output		Input	E-B
PCL	I/O	P22	Clock output		Input	E-B
BUZ	I/O	P23	Output for arbitrary frequency output (for buzzer output or system clock trimming)		Input	E-B
$\overline{SCK}$	I/O	P01	Serial clock I/O		Input	Ⓕ-A
SO/SB0	I/O	P02	Serial data output Serial bus I/O		Input	Ⓕ-B
SI/SB1	I/O	P03	Serial data input Serial bus I/O		Input	Ⓜ-C
INT4	Input	P00	Edge detection vectored interrupt input (either rising edge or falling edge detection)		–	Ⓑ
INT0	Input	P10	Edge detection vectored interrupt input (detection edge selectable)	Note 2	–	Ⓑ-C
INT1		P11		Note 3		
INT2	Input	P12	Edge detection testable input (rising edge detection)	Note 3	–	Ⓑ-C
KR0 - KR3	I/O	P60 - P63	Parallel falling edge detection testable input		Input	Ⓕ-A
KR4-KR7	I/O	P70 - P73	Parallel falling edge detection testable input		Input	Ⓕ-A
$\overline{MAR}$	I/O	P100	In MFT integral A/D converter mode	Reverse integration signal output	Note 4	M
$\overline{MAI}$	I/O	P101		Integration signal output	Note 4	M
$\overline{MAZ}$	I/O	P102		Autozero signal output	Note 4	M
$\overline{MAT}$	I/O	P103		Comparator input	Note 4	M
PPO	I/O	P21	In MFT timer mode	Timer pulse output	Input	E-B
AN0 - AN3	Input	P110 - P113	For A/D converter only	8-bit analog input	Input	Y-A
AN4 - AN7		–				Y
AV_{REF+}	Input	–		Reference voltage input (on AV_{DD} side)	–	Z-A
AV_{REF-}	Input	–		Reference voltage input (on AV_{SS} side)	–	Z-A
AV_{DD}	–	–		Operating power supply	–	–
AV_{SS}	–	–		Reference GND potential	–	–

Notes 1. The circle (◯) indicates the Schmitt trigger input.

2. Clock synchronous

3. Asynchronous

4. High level (when pull-up resistors are provided) or high impedance

Remark MFT: Multifunction Timer

3.2 NON-PORT PINS (2/2)

Pin	Input/ output	Shared pin	Function	When reset	I/O circuit type[Note]
X1, X2	Input	–	Crystal/ceramic connection for main system clock generation. When external clock signal is used, it is applied to X1, and its reverse phase signal is applied to X2.	–	–
XT1, XT2	Input	–	Crystal connection for subsystem clock generation. When external clock signal is used, it is applied to XT1, and its reverse phase signal is applied to XT2, XT1 can be used as a 1-bit input (test).	–	–
$\overline{\text{RESET}}$	Input	–	System reset input	–	Ⓑ
IC	–	–	Internally connected. (To be directly connected to V_{DD})	–	–
V_{DD}	–	–	Positive power supply	–	–
V_{SS}	–	–	GND potential	–	–

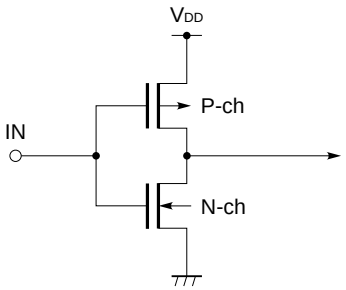
Note The circle (◯) indicates the Schmitt trigger input.

3.3 PIN INPUT/OUTPUT CIRCUITS

The input/output circuit of each μPD75036 pin is shown below in a simplified manner.

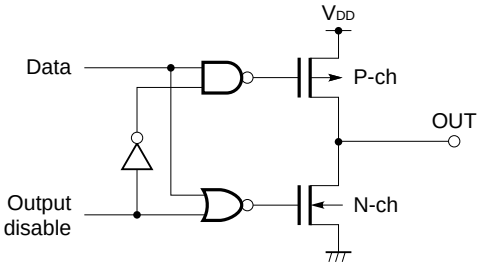
(1/3)

Type A (For type E-B)



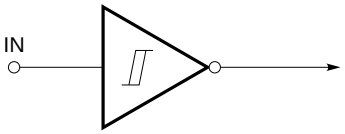
CMOS input buffer

Type D (For type E-B, F-A)



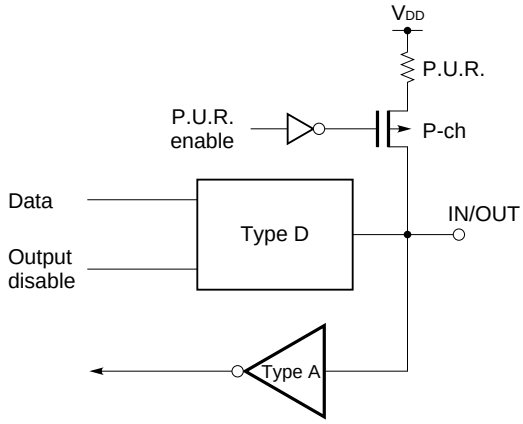
Push-pull output which can be set to high-impedance output (off for both P-ch and N-ch)

Type B



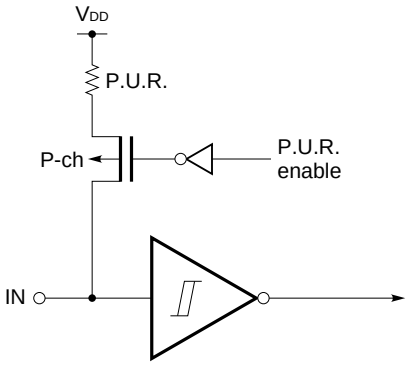
Schmitt trigger input with hysteresis

Type E-B



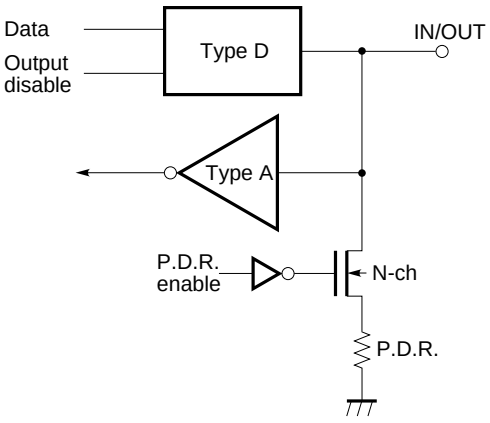
P.U.R.: Pull-Up Resistor

Type B-C



P.U.R.: Pull-Up Resistor

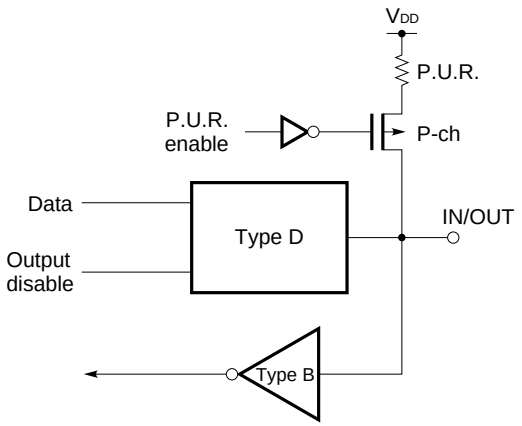
Type E-D



P.D.R.: Pull-Down Resistor

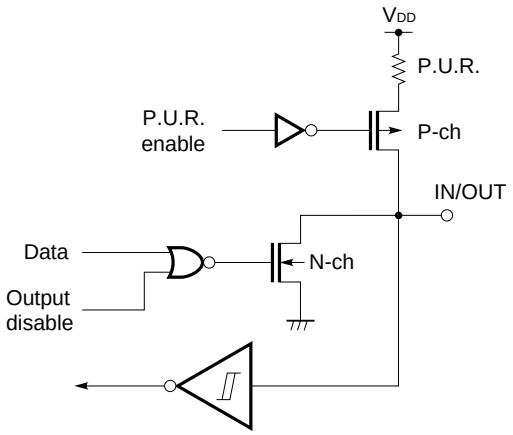
(2/3)

Type F-A



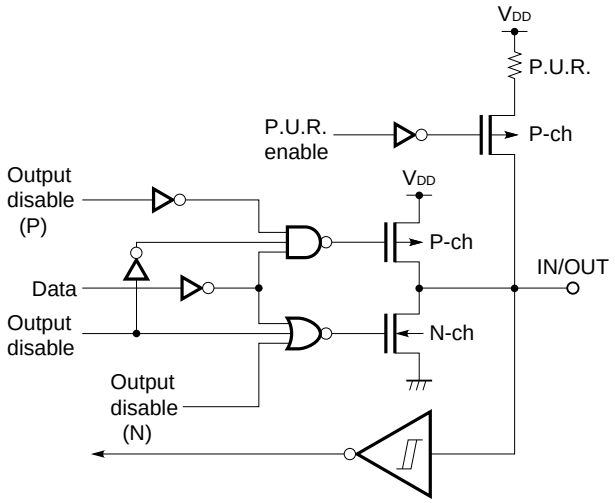
P.U.R.: Pull-Up Resistor

Type M-C



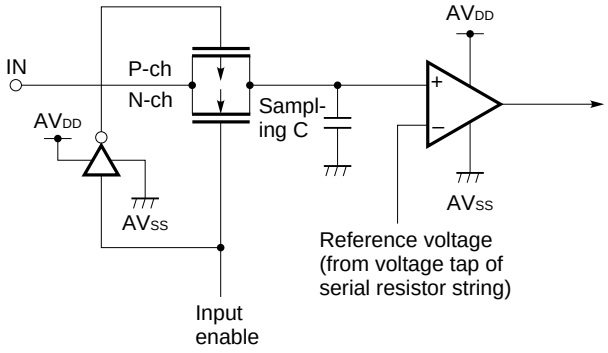
P.U.R.: Pull-Up Resistor

Type F-B

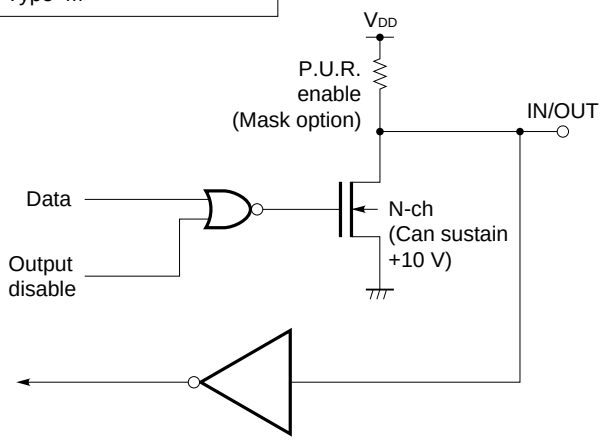


P.U.R.: Pull-Up Resistor

Type Y



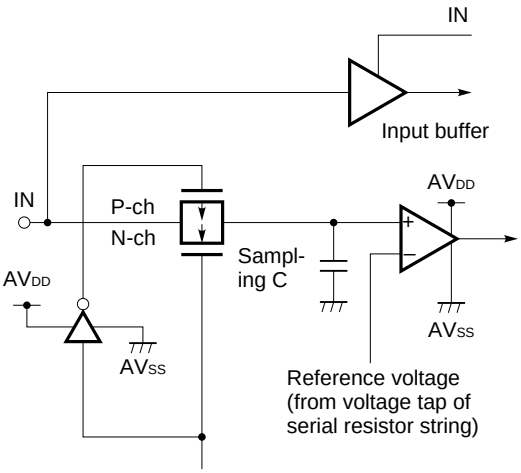
Type M



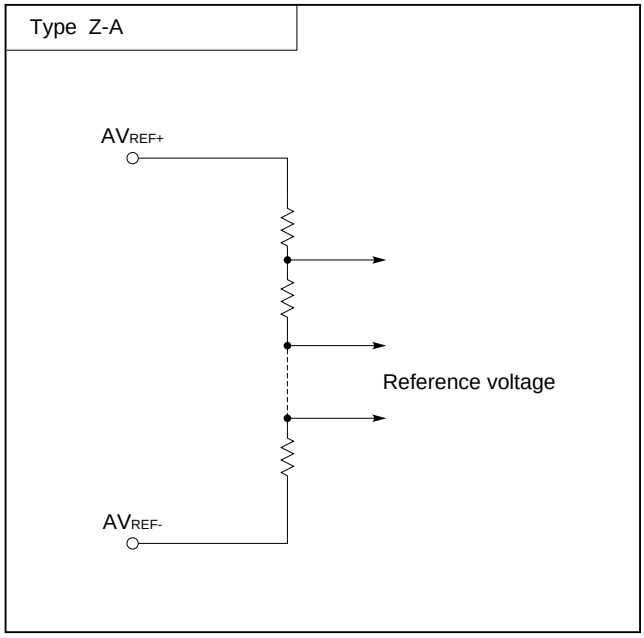
Middle-voltage input buffer
(Can sustain +10 V)

P.U.R.: Pull-Up Resistor

Type Y-A



(3/3)



3.4 MASK OPTION SELECTION

The following mask options are available for selection for each pin.

Pin name	Mask option	
P40 - P43, P50 - P53, P100-P103	① Pull-up resistor provided (specifiable bit by bit)	② Pull-up resistor not provided (specifiable bit by bit)
XT1, XT2	① Feedback resistor provided (if a subsystem clock is used)	② Feedback resistor not provided (if a subsystem clock is not used)

★ 3.5 CONNECTION OF UNUSED PINS

Pin	Recommended connection
P00/INT4	To be connected to V_{SS}
P01/$\overline{SCK}$	To be connected to V_{SS} or V_{DD}
P02/SO/SB0	
P03/SI/SB1	
P10/INT0-P12/INT2	To be connected to V_{SS}
P13/TI0	
P20/PTO0	Input state : To be connected to V_{SS} or V_{DD} Output state:To be open
P21/PPO	
P22/PCL	
P23/BUZ	
P30-P33	
P40-P43	
P50-P53	
P60/KR0-P63/KR3	
P70/KR4-P73/KR7	
P80-P83	
P90-P93	
P100/$\overline{MAR}$	
P101/$\overline{MAI}$	
P102/$\overline{MAZ}$	
P103/$\overline{MAT}$	
P110/AN0-P113/AN3	To be connected to V_{SS} or V_{DD}
AN4-AN7	
AV_{REF+}	To be connected to V_{SS}
AV_{REF-}	
AV_{SS}	
AV_{DD}	To be connected to V_{DD}
XT1	To be connected to V_{SS} or V_{DD}
XT2	To be open
IC	To be directly connected to V_{DD}

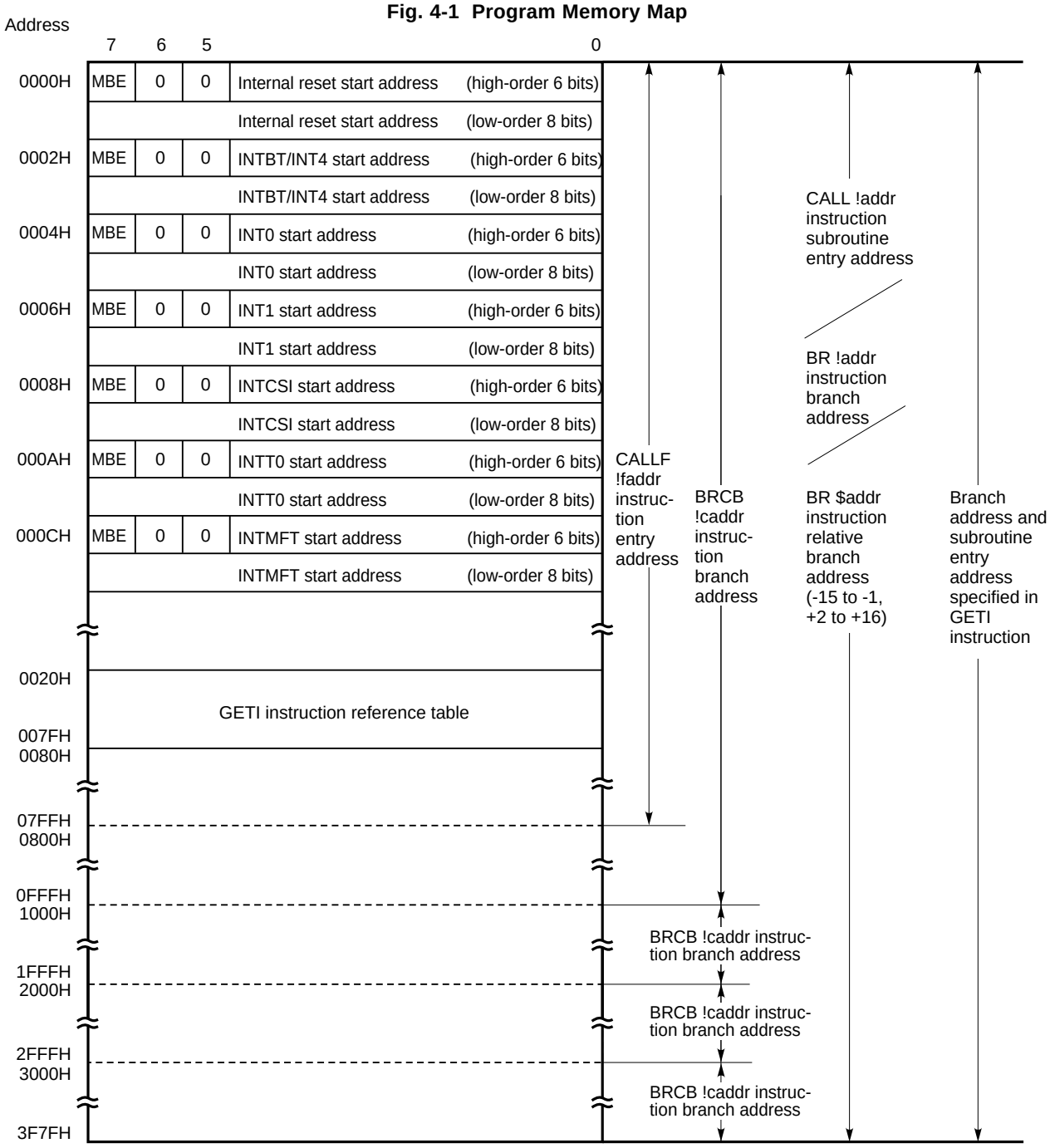
4. ARCHITECTURE AND MEMORY MAP OF THE μPD75036

The μPD75036 has two architectural features:

- Bank configuration of data memory: Static RAM (1024 words × 4 bits)
  Peripheral hardware (128 × 4 bits)
- Memory mapped I/O

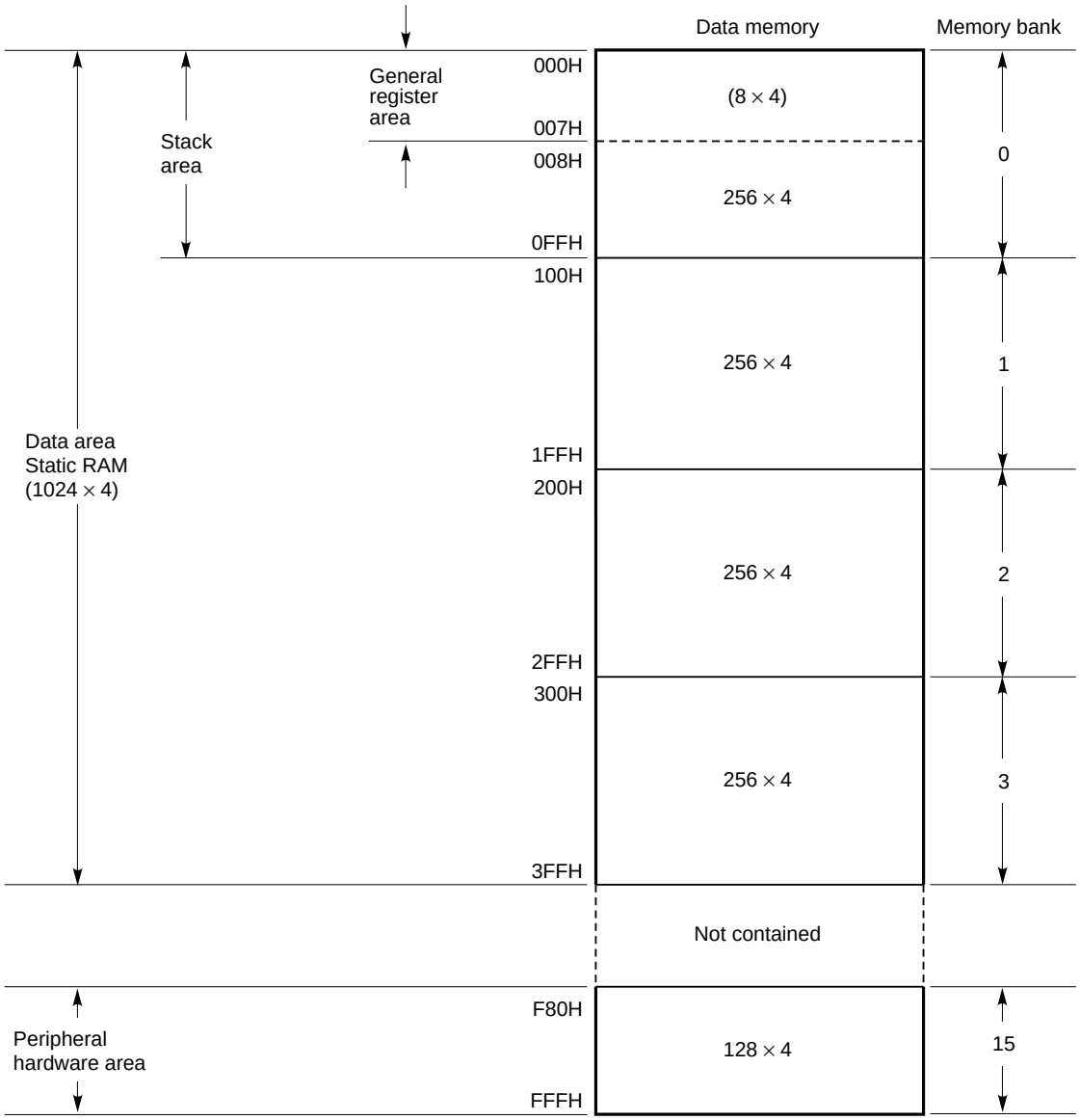
Fig. 4-1 and 4-2 show the memory maps for the μPD75036.

Fig. 4-1 Program Memory Map



Remark In addition to the above, the BR PCDE and BR PCXA instructions can cause a branch to an address with only the low-order 8 bits of the PC changed.

Fig. 4-2 Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

The μPD75036 has the following three types of I/O port:

- 12 CMOS input ports (Ports 0, 1, and 11)
- 24 CMOS I/O ports (Ports 2, 3, 6, 7, 8, and 9)
- 12 N-ch open-drain I/O ports (Ports 4, 5, and 10)

Total: 48 ports

Table 5-1 Functions of Ports

Port (symbol)	Function	Operation and feature	Remarks
PORT0 PORT1	4-bit input	Allows input and test at any time regardless of the operation modes of dual function pins.	Also used as SO/SB0, SI/SB1, $\overline{SCK}$, INT0-INT2, INT4, and TI0 pins.
PORT3[Note] PORT6	4-bit I/O	Allows input or output mode setting in units of one bit.	Port 6 is also used as KR0-KR3 pins.
PORT2 PORT7		Allows input or output mode setting in units of four bits. Ports 6 and 7 make a pair, allowing data I/O in units of eight bits.	Port 2 is also used as PTO0, PPO, PCL, and BUZ pins.
			Also used as KR4-KR7 pins.
PORT4[Note] PORT5[Note] PORT10[Note]	4-bit I/O (N-ch open-drain, withstand voltage: 10 V)	Allows input or output mode setting in units of four bits. Ports 4 and 5 make a pair, allowing data I/O in units of eight bits.	Use of an internal pull-up registor can be mask-programmed in units of one bit.
			Port 10 is also used as $\overline{MAR}$, $\overline{MAI}$, $\overline{MAZ}$, and $\overline{MAT}$ pins.
PORT8 PORT9	4-bit I/O	Allows input or output mode setting in units of four bits.	
PORT11	4-bit input	Port for 4-bit input	Port 11 is also used as AN0-AN3 pins.

Note Ports 3, 4, 5 and 10 can directly drive an LED.

5.2 CLOCK GENERATOR

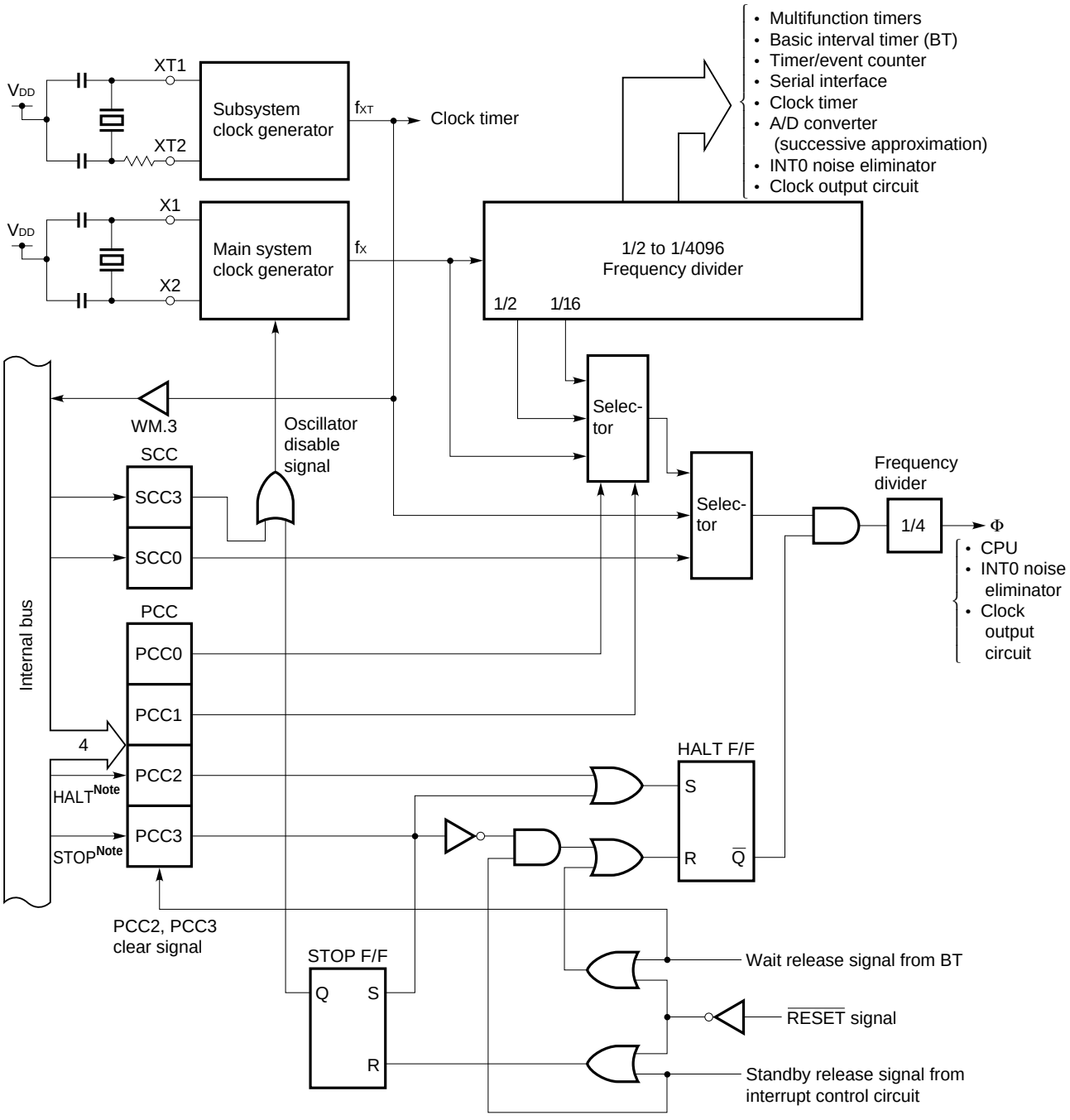
Operation of the clock generator is specified by the processor clock control register (PCC) and system clock control register (SCC).

The main system clock or subsystem clock can be selected.

The instruction execution time is variable.

- 0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz)
- 122 μs (subsystem clock: 32.768 kHz)

★ **Fig. 5-1 Block Diagram of the Clock Generator**



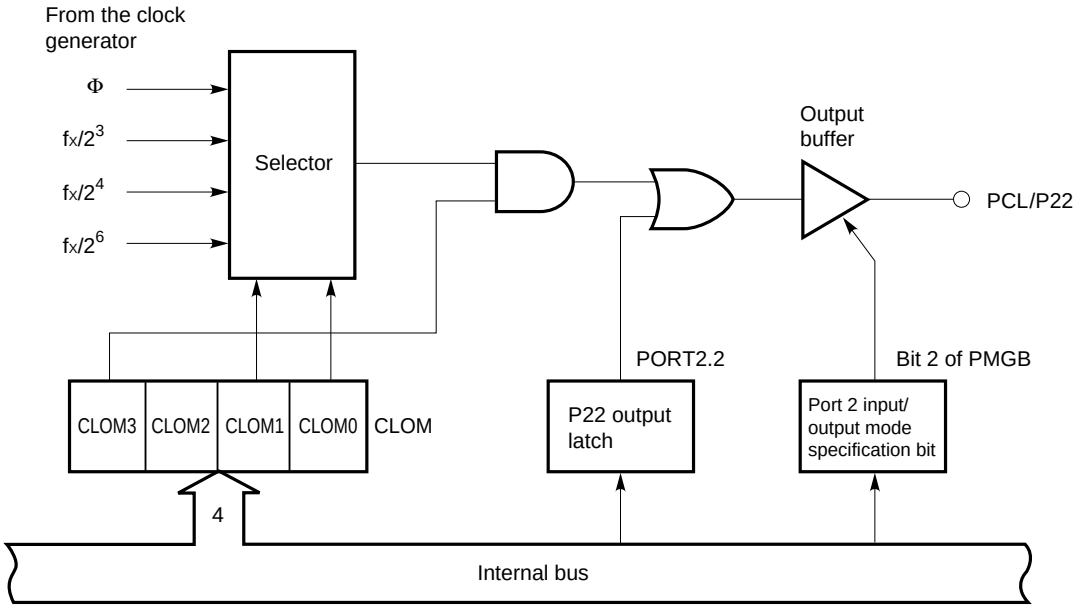
Note Instruction execution

Remarks 1. f_X : Main system clock frequency
2. f_{XT} : Subsystem clock frequency
3. Φ = CPU clock
4. PCC: Processor clock control register
5. SCC: System clock control register
6. One clock cycle (t_{CY}) of the CPU clock (Φ) is equal to one machine cycle of an instruction. See **Chapter 10** for details of t_{CY}.

5.3 CLOCK OUTPUT CIRCUIT

The clock output circuit outputs a clock pulse signal on the P22/PCL pin for remote control or for supplying clock pulses to a peripheral LSI device.

Fig. 5-2 Configuration of the Clock Output Circuit



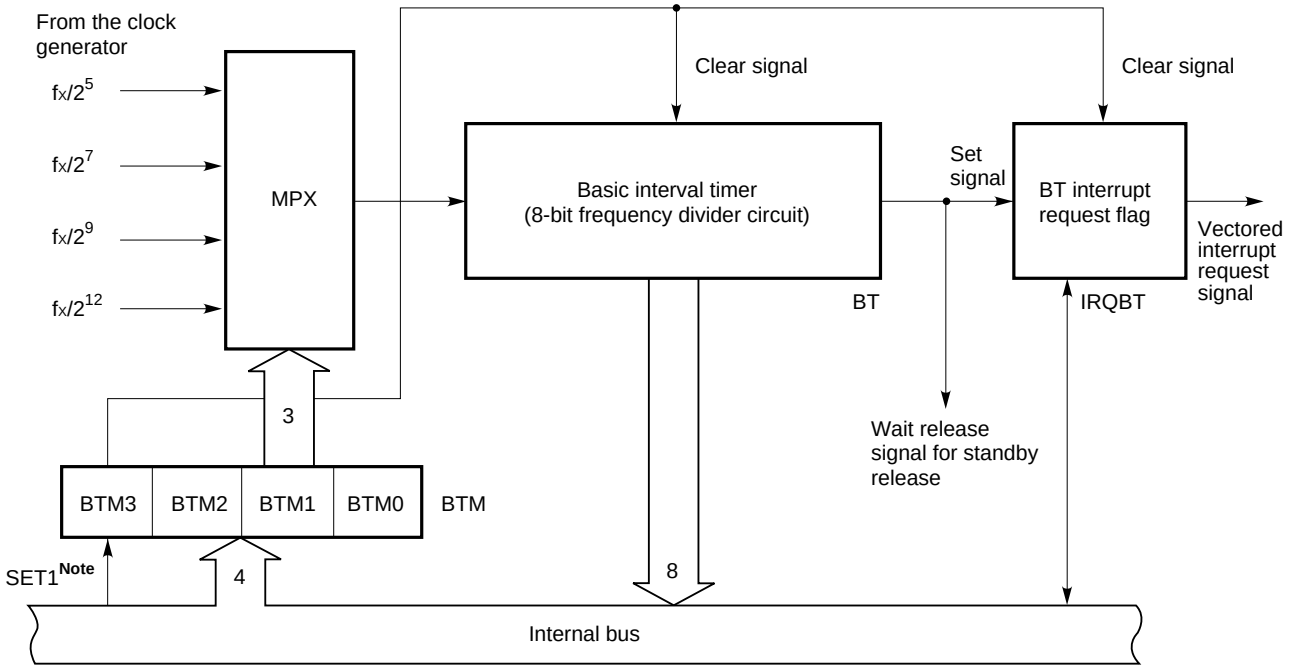
Remark The clock output circuit is designed so that pulses with short widths do not appear in enabling or disabling clock output.

5.4 BASIC INTERVAL TIMER

The basic interval timer provides the following functions:

- Interval timer operation that generates a reference time interrupt
- Application of watchdog timer for detecting program crashes
- Selection of a wait time for releasing the standby mode, and counting
- Reading the count value

Fig. 5-3 Configuration of the Basic Interval Timer



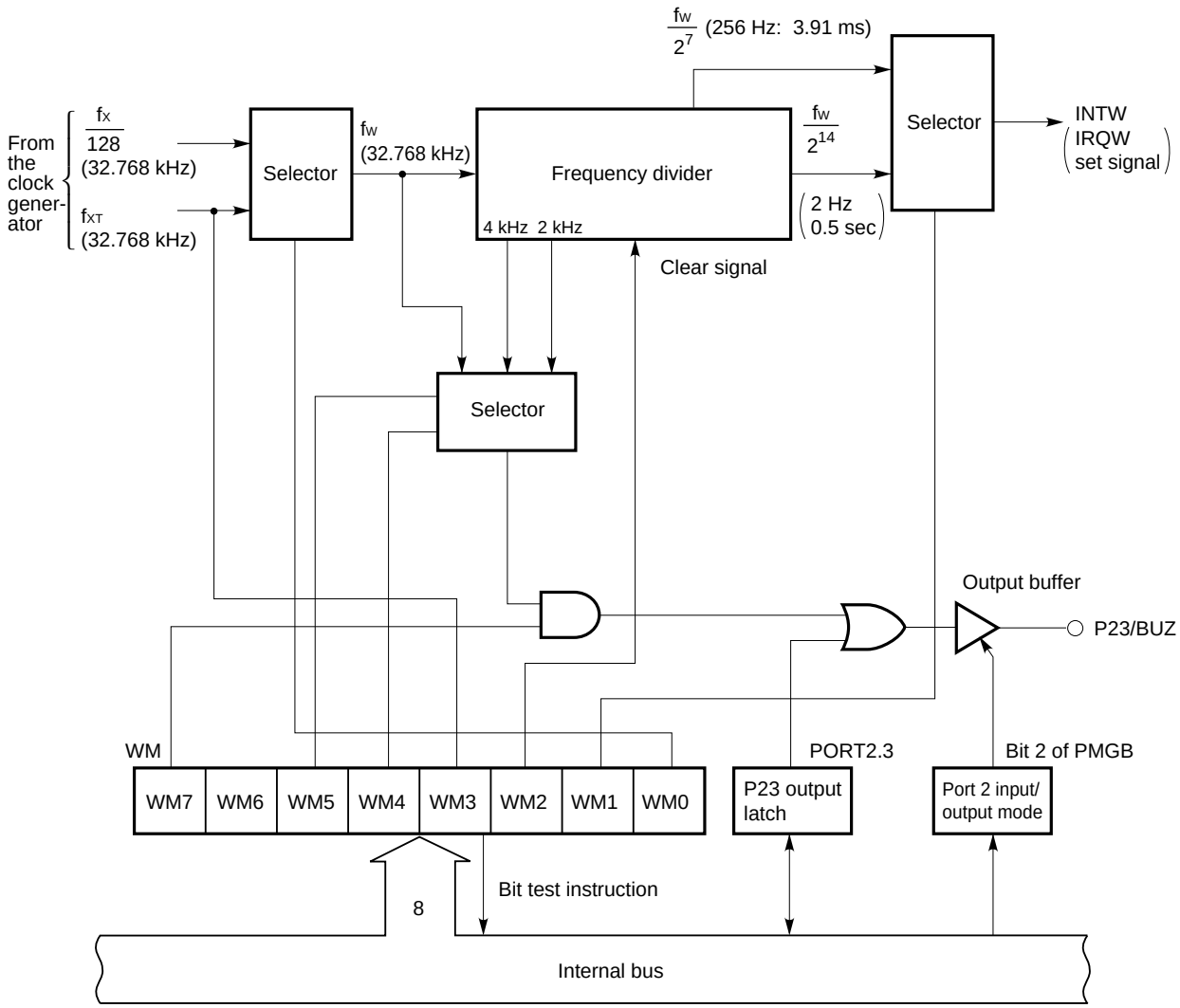
Note Instruction execution

5.5 CLOCK TIMER

The μPD75036 contains one channel for a clock timer. The clock timer provides the following functions:

- The clock timer sets the test flag (IRQW) every 0.5 seconds.
  The standby mode can be released with IRQW.
- Either the main system clock or subsystem clock can produce 0.5-second intervals.
- The fast-forward mode produces an interval 128 times faster (3.91 ms), which is useful for program debugging and testing.
- An arbitrary frequency (2.048, 4.096, or 32.768 kHz) can be output to the P23/BUZ pin, so that it can be used for sounding the buzzer and system clock frequency trimming.
- The frequency divider can be cleared, so the clock can start from zero seconds.

Fig. 5-4 Block Diagram of the Clock Timer



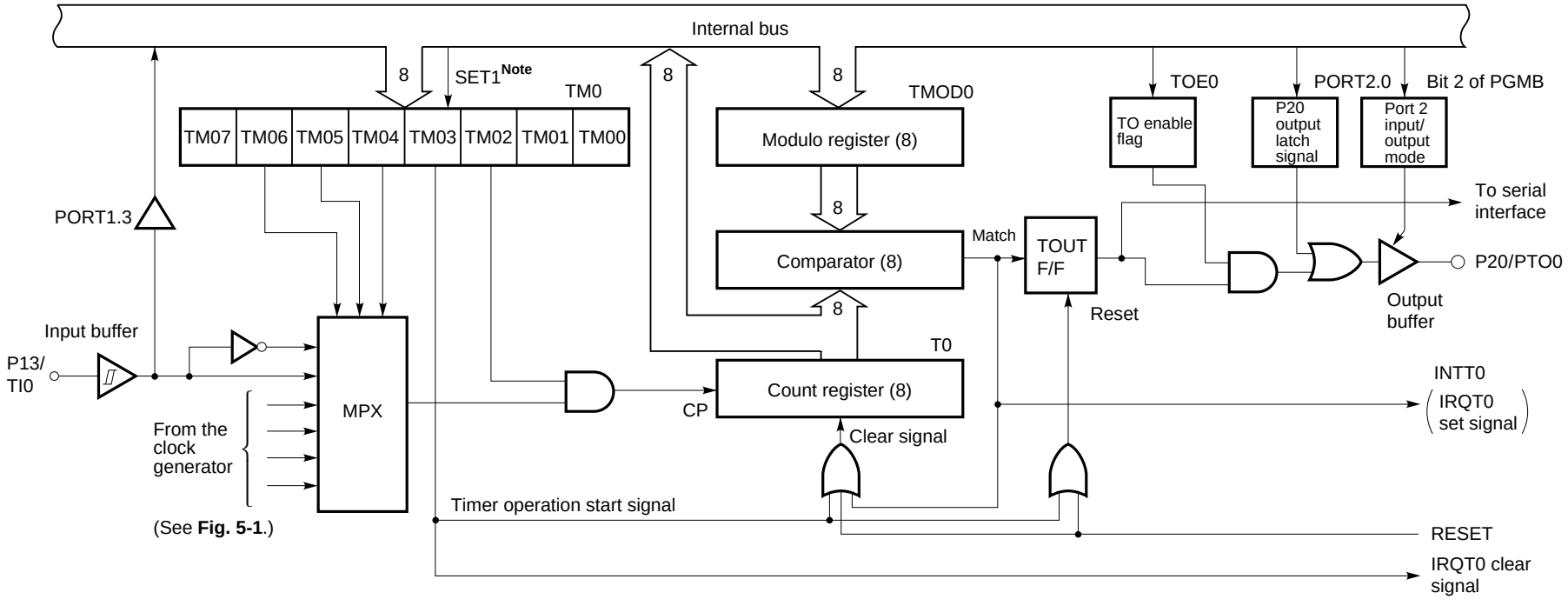
The values in parentheses indicates are for f_X = 4.194304 MHz and f_{XT} = 32.768 kHz

5.6 TIMER/EVENT COUNTER

The μPD75036 contains one channel of timer/event counter. The timer/event counter provides the following functions:

- Programmable interval timer operation
- Output of a square wave at a given frequency to the PTO0 pin
- Event counter operation
- Frequency divider operation that divides TI0 pin input by N and outputs the result to the PTO0 pin
- Supply of serial shift clock signal to a serial interface circuit
- Function of reading the state of counting

Fig. 5-5 Block Diagram of the Timer/Event Counter



Note Instruction execution

5.7 SERIAL INTERFACE

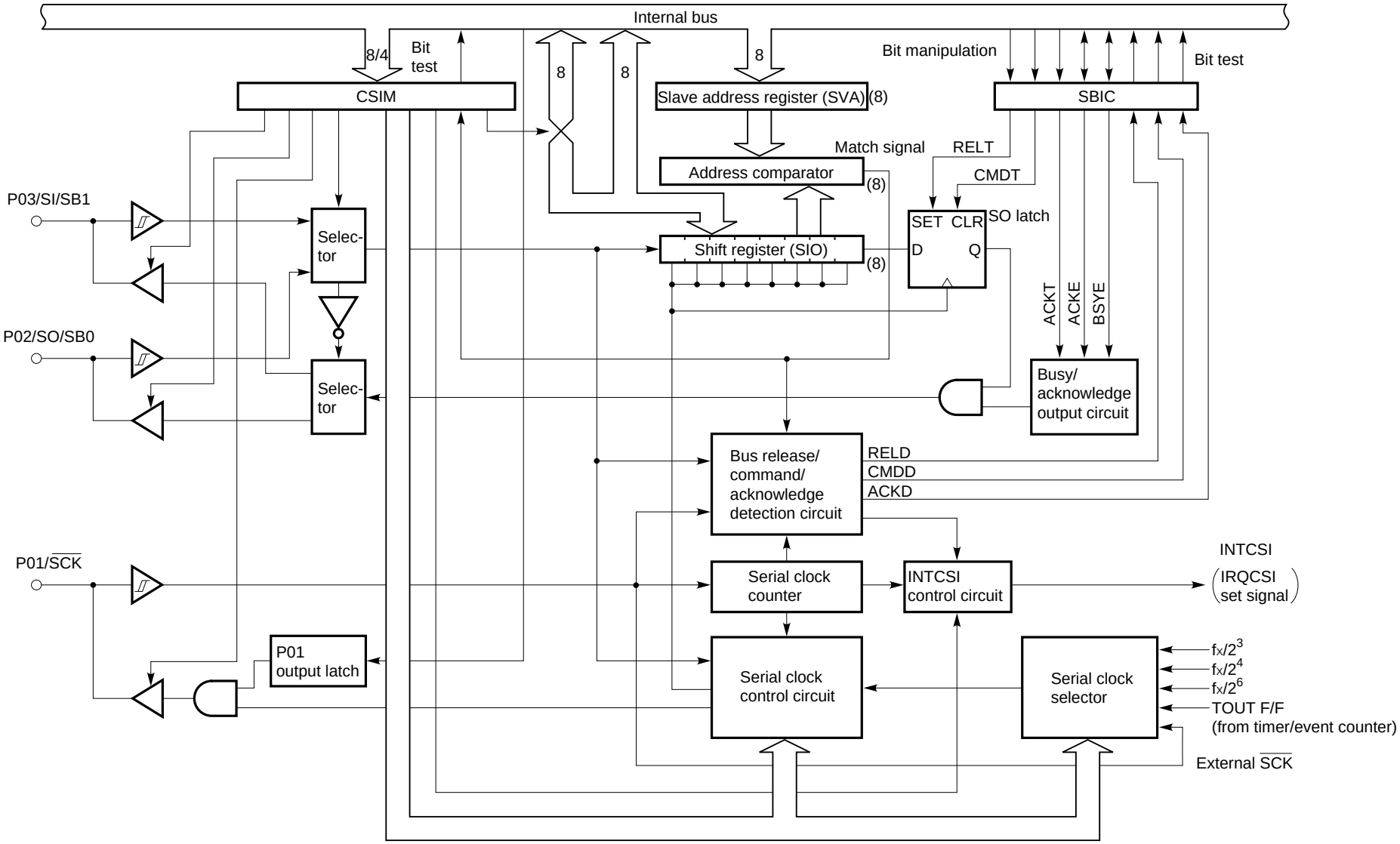
The μPD75036 has three modes.

- Three-wire serial I/O mode (The first bit is switchable between MSB and LSB.)
- Two-wire serial I/O mode (The first bit is MSB.)
- SBI mode (The first bit is MSB.)

The three-wire serial I/O mode enables connections to be made with the 75X series, 78K series, and many other types of I/O devices.

The two-wire serial I/O mode and SBI mode enable communication with two or more devices.

Fig. 5-6 Block Diagram of the Serial Interface

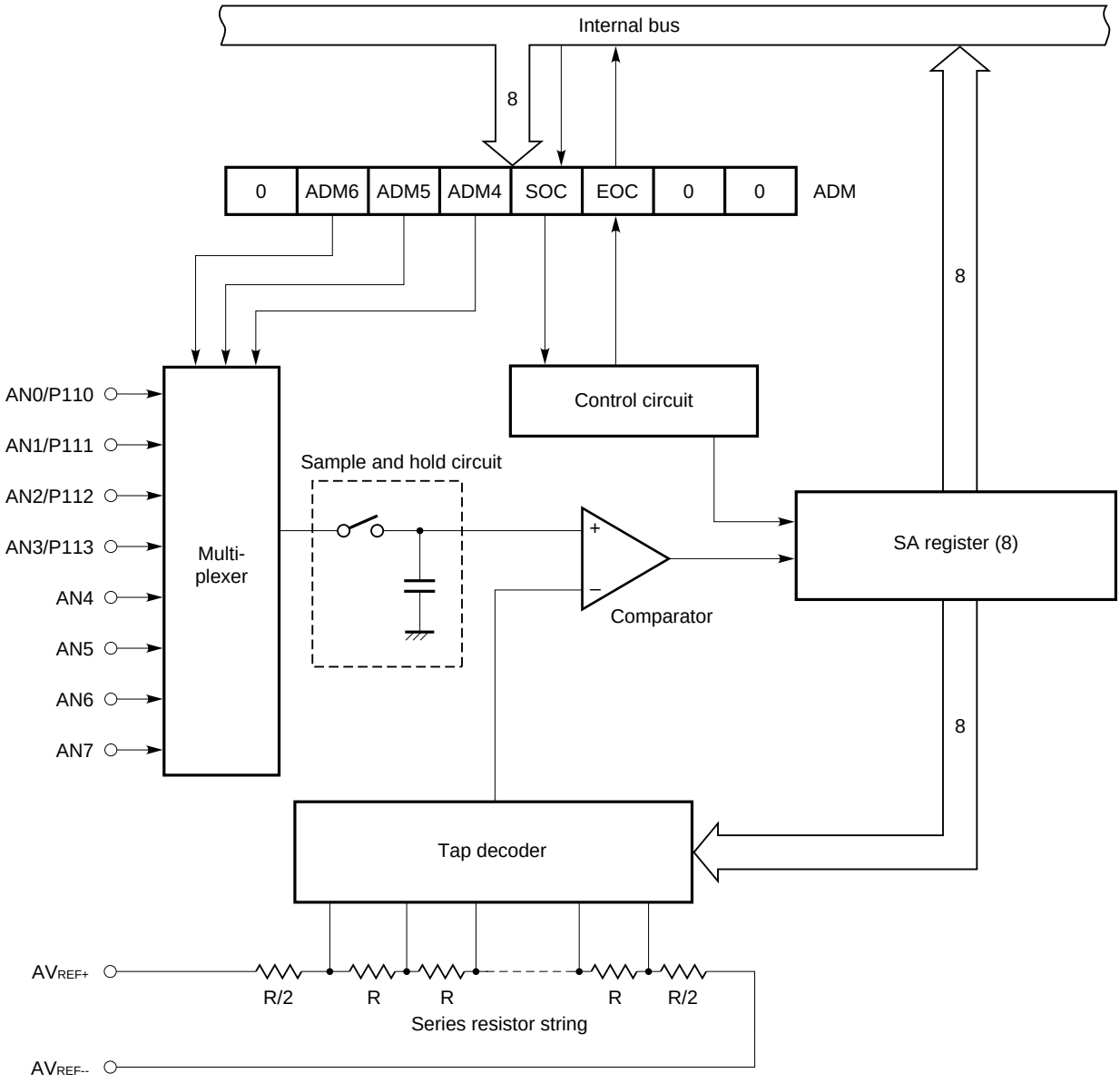


5.8 A/D CONVERTER

The μPD75036 contains an 8-bit resolution analog/digital (A/D) converter that has eight analog input channels (AN0 - AN7).

The A/D converter employs the successive-approximation method.

Fig. 5-7 Configuration of the A/D Converter

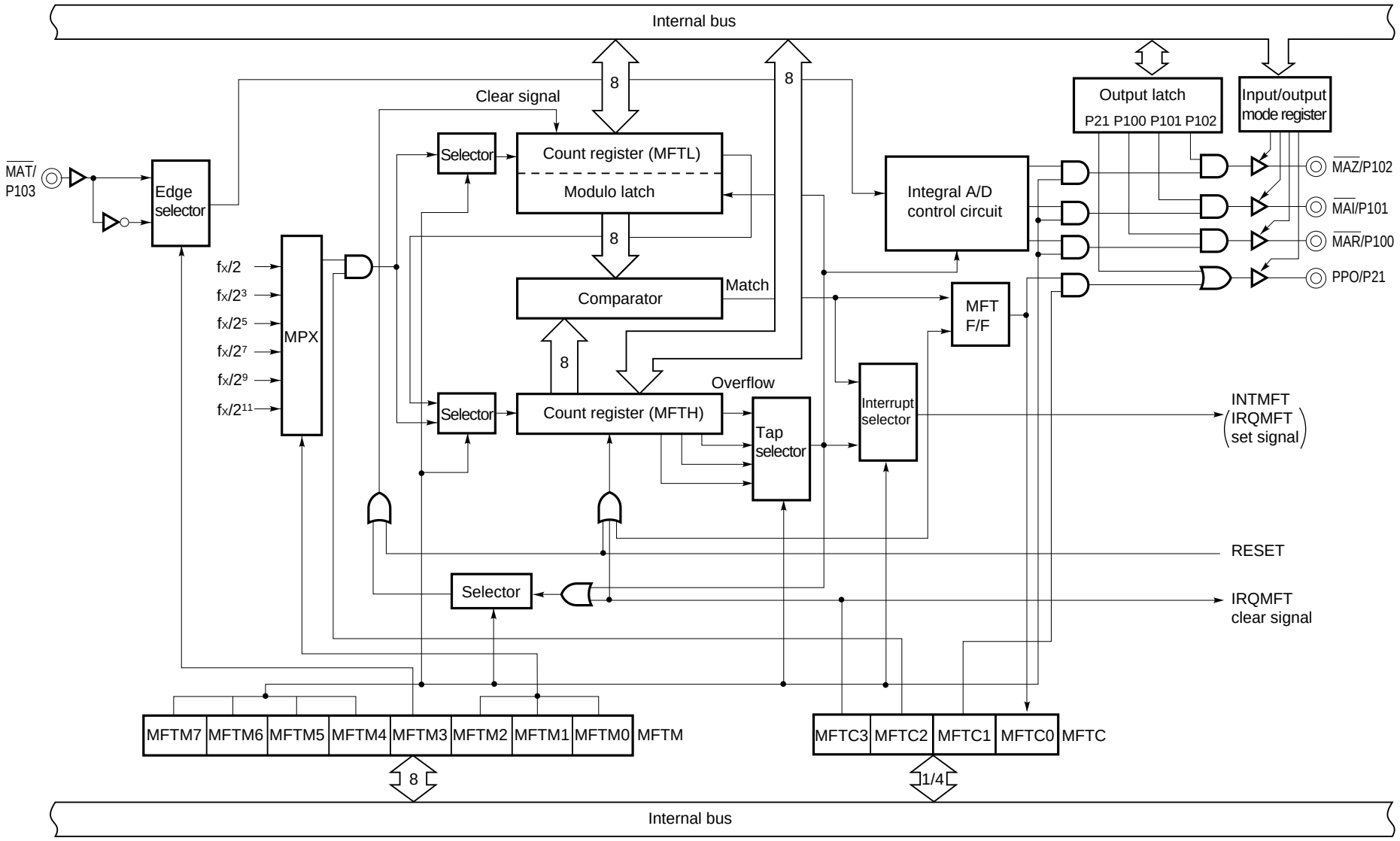


5.9 MULTIFUNCTION TIMER (MFT)

The μPD75036 contains one multifunction timer (MFT). The MFT has four operation modes. Each mode provides the following functions:

- 8-bit timer mode
  - Operates as a programmable interval timer.
  - Outputs a square wave of an arbitrary frequency on the PPO pin.
- PWM output mode
  - Outputs a 6-bit, 7-bit, or 8-bit precision PWM signal on the PPO pin.
- 16-bit free-running timer mode
  - Operates as an interval timer that generates an interrupt at specified time intervals.
  - Usable as a one-shot timer.
- Integral A/D converter modes
  - Outputs a control signal for a 16-bit integral A/D converter.
  - Allows a resolution to be selected from 13 bits, 14 bits, 15 bits, and 16 bits.

Fig. 5-8 Block Diagram of the Multifunction Timer



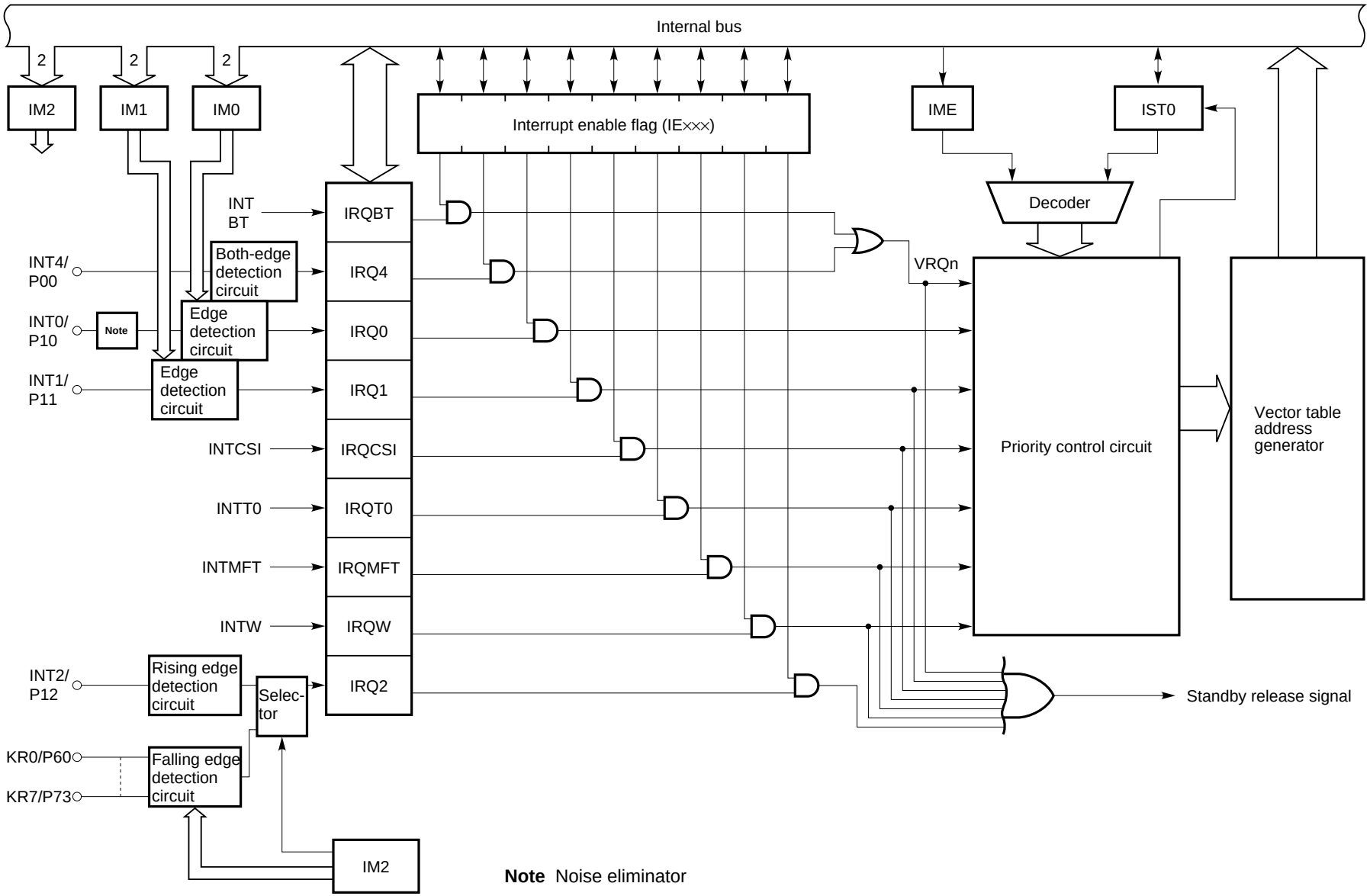
6. INTERRUPT FUNCTION

The μPD75036 has nine vectored interrupt sources and provides multiple interrupts by software control. It also has two types of edge detected testable input pins.

The interrupt control circuitry of the μPD75036 has the following features:

- Vectored interrupts are controlled by the hardware. Whether to accept an interrupt is controlled by an interrupt flag (IE×××) and interrupt master enable flag (IME).
- An interrupt start address can be freely set.
- An interrupt request flag (IRQ×××) can be tested. (Whether an interrupt has occurred can be checked by software.)
- A standby mode can be released. (What interrupt source to release can be selected using an interrupt enable flag.)

Fig. 6-1 Block Diagram of Interrupt Control Circuit



Note Noise eliminator

7. STANDBY FUNCTION

To reduce the power consumption of the system waiting for a program input, the μPD75036 has two standby modes STOP and HALT modes.

Table 7-1 Standby Modes and Operation Status

		STOP mode	HALT mode
Instruction for setting		STOP instruction	HALT instruction
System clock at setting		This mode can be set only when the main system clock is used.	This mode can be set when either the main system clock or subsystem clock is used.
Operation status	Clock generator	Only the main system clock is stopped.	Only CPU clock Φ is stopped (with oscillation continued).
	Basic interval timer	Operation is stopped.	Operation is possible only when the main system clock is oscillated. (Sets IRQBT at reference time intervals)
	Serial interface	Operation is possible only when external $\overline{SCK}$ input is selected for the serial clock.	Operation is possible only when external $\overline{SCK}$ input is selected for the serial clock or the main system clock is oscillated.
	Timer/event counter	Operation is possible only when TI0 pin input is selected for the count clock.	Operation is possible only when TI0 pin input is selected for the count count clock or the main system clock is oscillated.
	Clock timer	Operation is possible when f_{XT} is selected for the count clock.	Operation is possible.
	A/D converter	Operation is stopped.	Operation is possible.[Note]
	Multifunction timer	Operation is stopped.	Operation is possible.[Note]
	External interrupt	INT1, INT2, and INT4 are enabled. INT0 is disabled.	
	CPU	Operation is stopped.	
Release signal		Interrupt request signals sent out from hardware, which are enabled by interrupt enable flags, or $\overline{RESET}$ input	Interrupt request signals sent out from hardware, which are enabled by interrupt enable flags, or $\overline{RESET}$ input

Note Operation is possible only when the main system clock operates.

8. RESET FUNCTION

The μPD75036 is reset by $\overline{RESET}$ signal input.

9. INSTRUCTION SET

(1) Operand identifier and its descriptive method

The operands are described in the operand column of each instruction according to the descriptive method for the operand format of the appropriate instructions (refer to *RA75X Assembler Package User's Manual, Language* (EEU-1363) for details). For descriptions in which alternatives exist, one element should be selected. Capital letters and plus and minus signs are keywords; therefore, they should be described as they are.

For immediate data, the appropriate numerical values or labels should be described.

Identifier	Description
reg reg1	X, A, B, C, D, E, H, L X, B, C, D, E, H, L
rp rp1 rp2	XA, BC, DE, HL BC, DE, HL BC, DE
rpa rpa1	HL, DE, DL DE, DL
n4 n8	4-bit immediate data or label 8-bit immediate data or label
mem[Note] bit	8-bit immediate data or label 2-bit immediate data or label
fmem pmem	FB0H - FBFH, FF0H - FFFH immediate data or label FC0H - FFFH immediate data or label
addr caddr faddr	0000H - 3F7FH immediate data or label 12-bit immediate data or label 11-bit immediate data or label
taddr	20H - 7FH immediate data (however, bit 0 = 0) or label
PORTn IE××× MBn	PORT0 - PORT11 IEBT, IECSI, IET0, IE0, IE1, IE2, IE4, IEW, IEMFT MB0, MB1, MB2, MB3, MB15

Note Only even address can be specified for mem when processing 8-bit data.

(2) Symbol definitions in operation description

A : A register; 4-bit accumulator
B : B register
C : C register
D : D register
E : E register
H : H register
L : L register

X : X register
XA : Pair register (XA); 8-bit accumulator
BC : Pair register (BC)
DE : Pair register (DE)
HL : Pair register (HL)
PC : Program counter
SP : Stack pointer
CY : Carry flag; Bit accumulator
PSW : Program status word
MBE : Memory bank enable flag
PORTn : Port n (n = 0 to 11)
IME : Interrupt master enable flag
IE××× : Interrupt enable flag
MBS : Memory bank selection register
PCC : Processor clock control register
. : Address bit delimiter
(××) : Contents addressed by ××
××H : Hexadecimal data

(3) Explanation of the symbols in the addressing area field

*1	MB = MBE•MBS (MBS = 0, 1, 2, 3, or 15)	Data memory addressing
*2	MB = 0	
*3	MBE = 0: MB = 0 (00H-7FH) MB = 15 (80H-FFH) MBE = 1: MB = MBS (MBS = 0, 1, 2, 3, or 15)	
*4	MB = 15, fmem = FB0H-FBFH or FF0H-FFFH	
*5	MB = 15, pmem = FC0H-FFFH	
*6	addr = 0000H-3F7FH	Program memory addressing
*7	addr = (Current PC) - 15 to (Current PC) - 1 or (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H-0FFFH ($PC_{13,12}$ = 00B) or 1000H-1FFFH ($PC_{13,12}$ = 01B) or 2000H-2FFFH ($PC_{13,12}$ = 10B) or 3000H-3F7FH ($PC_{13,12}$ = 11B)	
*9	faddr = 0000H-07FFH	
*10	taddr = 0020H-007FH	

Remarks 1. MB indicates an accessible memory bank.
2. For *2, MB is always 0 irrespective of MBE and MBS.
3. For *4 and *5, MB is always 15 irrespective of MBE and MBS.
4. *6 to *10 indicate each addressable area.

(4) Description of machine cycle column

S indicates the number of machine cycles necessary for skipping any skip instruction. The value of S changes as follows:

- When no skip is performed ····· S = 0
- When a 1-byte or 2-byte instruction is skipped ····· S = 1
- When a 3-byte instruction (BR !addr, CALL !addr instruction) is skipped ····· S = 2

Caution The GETI instruction is skipped in one machine cycle.

One machine cycle is equivalent to one CPU clock Φ cycle (t_{CY}). Therefore, the length of the machine cycle can be selected from three different lengths by the PCC setting.

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Transfer	MOV	A, #n4	1	1	A ← n4		String A
		reg1, #n4	2	2	reg1 ← n4		
		XA, #n8	2	2	XA ← n8		String A
		HL, #n8	2	2	HL ← n8		String B
		rp2, #n8	2	2	rp2 ← n8		
		A, @HL	1	1	A ← (HL)	*1	
		A, @rpa1	1	1	A ← (rpa1)	*2	
		XA, @HL	2	2	XA ← (HL)	*1	
		@HL, A	1	1	(HL) ← A	*1	
		@HL, XA	2	2	(HL) ← XA	*1	
		A, mem	2	2	A ← (mem)	*3	
		XA, mem	2	2	XA ← (mem)	*3	
		mem, A	2	2	(mem) ← A	*3	
		mem, XA	2	2	(mem) ← XA	*3	
		A, reg1	2	2	A ← reg1		
		XA, rp	2	2	XA ← rp		
		reg1, A	2	2	reg1 ← A		
		rp1, XA	2	2	rp1 ← XA		
	XCH	A, @HL	1	1	A ↔ (HL)	*1	
		A, @rpa1	1	1	A ↔ (rpa1)	*2	
		XA, @HL	2	2	XA ↔ (HL)	*1	
		A, mem	2	2	A ↔ (mem)	*3	
		XA, mem	2	2	XA ↔ (mem)	*3	
		A, reg1	1	1	A ↔ reg1		
		XA, rp	2	2	XA ↔ rp		
Table reference	MOVT	XA, @PCDE	1	3	XA ← $(PC_{13-8} + DE)_{ROM}$		
		XA, @PCXA	1	3	XA ← $(PC_{13-8} + XA)_{ROM}$		
Arithmetic	ADDS	A, #n4	1	1 + S	A ← A + n4		carry
		A, @HL	1	1 + S	A ← A + (HL)	*1	carry
	ADDC	A, @HL	1	1	A, CY ← A + (HL) + CY	*1	
	SUBS	A, @HL	1	1 + S	A ← A – (HL)	*1	borrow
	SUBC	A, @HL	1	1	A, CY ← A – (HL) – CY	*1	
	AND	A, #n4	2	2	A ← A ∧ n4		
		A, @HL	1	1	A ← A ∧ (HL)	*1	
	OR	A, #n4	2	2	A ← A ∨ n4		
		A, @HL	1	1	A ← A ∨ (HL)	*1	
	XOR	A, #n4	2	2	A ← A ∀ n4		
		A, @HL	1	1	A ← A ∀ (HL)	*1	

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Accumulator manipulation	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/ decrement	INCS	reg	1	1 + S	reg ← reg + 1		reg = 0
		@HL	2	2 + S	(HL) ← (HL) + 1	*1	(HL) = 0
		mem	2	2 + S	(mem) ← (mem) + 1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg ← reg – 1		reg = FH
Comparison	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
Carry flag manipulation	SET1	CY	1	1	CY ← 1		
	CLR1	CY	1	1	CY ← 0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit) ← 1	*3	
		fmem.bit	2	2	(fmem.bit) ← 1	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) \leftarrow 1$	*5	
		@H+mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 1$	*1	
	CLR1	mem.bit	2	2	(mem.bit) ← 0	*3	
		fmem.bit	2	2	(fmem.bit) ← 0	*4	
		pmem.@L	2	2	$(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) \leftarrow 0$	*5	
		@H+mem.bit	2	2	$(H + mem_{3-0}.bit) \leftarrow 0$	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 1$	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$	*1	(@H + mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 0$	*5	(pmem.@L) = 0
		@H+mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 0$	*1	(@H + mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if $(pmem_{7-2} + L_{3-2}.bit(L_{1-0})) = 1$ and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if $(H + mem_{3-0}.bit) = 1$ and clear	*1	(@H + mem.bit) = 1
	AND1	CY, fmem.bit	2	2	$CY \leftarrow CY \wedge (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \wedge (pmem_{7-2} + L_{3-2}.bit(L_{1-0}))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow CY \wedge (H + mem_{3-0}.bit)$	*1	
	OR1	CY, fmem.bit	2	2	$CY \leftarrow CY \vee (fmem.bit)$	*4	
		CY, pmem.@L	2	2	$CY \leftarrow CY \vee (pmem_{7-2} + L_{3-2}.bit(L_{1-0}))$	*5	
		CY, @H+mem.bit	2	2	$CY \leftarrow CY \vee (H + mem_{3-0}.bit)$	*1	

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Memory bit manipulation	XOR1	CY, fmem.bit	2	2	CY ← CY ∀ (fmem.bit)	*4	
		CY, pmem.@L	2	2	CY ← CY ∀ ($pmem_{7-2}$ + L_{3-2}.bit(L_{1-0}))	*5	
		CY, @H+mem.bit	2	2	CY ← CY ∀ (H + mem_{3-0}.bit)	*1	
Branch	BR	addr	–	–	PC_{13-0} ← addr (Appropriate instructions are selected from BR !addr, BRCB !caddr, and BR $addr by the assembler.)	*6	
		!addr	3	3	PC_{13-0} ← addr	*6	
		$addr	1	2	PC_{13-0} ← addr	*7	
	BRCB	!caddr	2	2	PC_{13-0} ← $PC_{13, 12}$ + $caddr_{11-0}$	*8	
Subroutine stack control	CALL	!addr	3	3	(SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, PC_{13}, PC_{12} PC_{13-0} ← addr, SP ← SP – 4	*6	
	CALLF	!faddr	2	2	(SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP–3) ← MBE, 0, PC_{13}, PC_{12} PC_{13-0} ← 000, faddr, SP ← SP – 4	*9	
	RET		1	3	MBE, 0, PC_{13}, PC_{12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4		
	RETS		1	3 + S	MBE, 0, PC_{13}, PC_{12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) SP ← SP + 4, then skip unconditionally		Unconditional
	RETI		1	3	MBE, 0, PC_{13}, PC_{12} ← (SP + 1) PC_{11-0} ← (SP)(SP + 3)(SP + 2) PSW ← (SP + 4)(SP + 5), SP ← SP + 6		
	PUSH	rp	1	1	(SP – 1)(SP – 2) ← rp, SP ← SP – 2		
		BS	2	2	(SP – 1) ← MBS, (SP – 2) ← 0, SP ← SP – 2		
	POP	rp	1	1	rp ← (SP + 1)(SP), SP ← SP + 2		
		BS	2	2	MBS ← (SP + 1), SP ← SP + 2		
Interrupt control	EI		2	2	IME ← 1		
		IE×××	2	2	IE××× ← 1		
	DI		2	2	IME ← 0		
		IE×××	2	2	IExxx ← 0		
Input/ output	IN[Note]	A, PORTn	2	2	A ← PORTn (n = 0 - 11)		
		XA, PORTn	2	2	XA ← PORTn+1,PORTn (n = 4, 6)		
	OUT[Note]	PORTn, A	2	2	PORTn ← A (n = 2 - 10)		
		PORTn, XA	2	2	PORTn+1,PORTn ← XA (n = 4, 6)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2 ← 1)		
	STOP		2	2	Set STOP Mode (PCC.3 ← 1)		
	NOP		1	1	No Operation		

Group	Mnemonic	Operand	Bytes	Machining cycle	Operation	Addressing area	Skip condition
Special	SEL	MBn	2	2	MBS ← n (n = 0, 1, 2, 3, or 15)		
	GETI	taddr	1	3	• For the TBR instruction $PC_{13-0} \leftarrow (taddr)_{5-0} + (taddr + 1)$	*10	
					• For the TCALL instruction (SP – 4)(SP – 1)(SP – 2) ← PC_{11-0} (SP – 3) ← MBE, 0, PC_{13}, PC_{12} $PC_{13-0} \leftarrow (taddr)_{5-0} + (taddr + 1)$ SP ← SP – 4		
					• For other than the TBR and TCALL instruction (taddr) (taddr + 1) is executed.		Depends on the reference instruction

Caution When executing the IN/OUT instruction, MBE must be set to 0 or MBE and MBS must be set to 1 and 15, respectively.

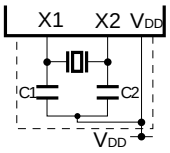
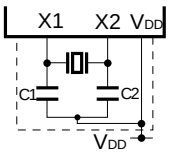
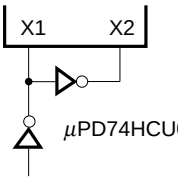
10. ELECTRICAL CHARACTERISTICS ★

ABSOLUTE MAXIMUM RATINGS (T_a = 25 °C)

Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V_{DD}			–0.3 to +7.0	V
Input voltage	V_{I1}	Ports other than ports 4, 5, and 10		–0.3 to V_{DD} + 0.3	V
	V_{I2}	Ports 4, 5, and 10	Built-in pull-up resistor	–0.3 to V_{DD} + 0.3	V
			Open drain	–0.3 to +11	V
Output voltage	V_O			–0.3 to V_{DD} + 0.3	V
High-level output current	I_{OH}	1 pin		–10	mA
		All pins		–30	mA
Low-level output current	I_{OL}**Note**	1 pin of parts 0, 3, 4, and 5	Peak value	30	mA
			rms	15	mA
		1 pin of ports other than ports 0, 3, 4 and 5	Peak value	20	mA
			rms	5	mA
		Total of all pins of ports 3 to 9 and 11	Peak value	170	mA
			rms	120	mA
		Total of all pins of ports 0, 2, and 10	Peak value	30	mA
			rms	20	mA
Operating temperature	T_{opt}			–40 to +85	˚C
Storage temperature	T_{stg}			–65 to +150	˚C

Note Calculate rms with [rms] = [peak value] × $\sqrt{\text{duty}}$.

CHARACTERISTICS OF THE MAIN SYSTEM CLOCK OSCILLATOR (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constant	Parameter	Conditions	Min.	Typ.	Max.	Unit
Ceramic resonator		Oscillator frequency (f_X) **Note 1**		1.0		5.0	MHz
		Oscillation settling time **Note 2**				4	ms
Crystal resonator		Oscillator frequency (f_X) **Note 1**		1.0	4.19	5.0**Note 3**	MHz
		Oscillation settling time **Note 2**	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) **Note 1**		1.0		5.0	MHz
		X1 input high/low level width (t_{XH}, t_{XL})		100		500	ns

Notes 1. The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

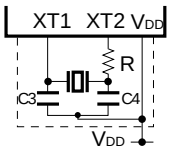
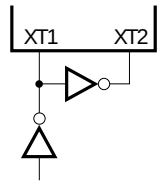
2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} is applied or after the STOP mode is released.

3. When 4.19 MHz < $f_X \leq$ 5.0 MHz, do not select PCC = 0011 as the instruction execution time. When PCC = 0011, one machine cycle falls short of 0.95 μs, the minimum value for the standard.

Caution When the main system clock oscillator is used, conform to the following guidelines when wiring at the portions of surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of V_{DD}. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

CHARACTERISTICS OF THE SUBSYSTEM CLOCK OSCILLATOR (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Resonator	Recommended constant	Parameter	Conditions	Min.	Typ.	Max.	Unit
Crystal resonator		Oscillator frequency (f_{XT}) **Note 1**		32	32.768	35	kHz
		Oscillation settling time **Note 2**	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT}) **Note 1**		32		100	kHz
		XT1 input high/low level width (t_{XTH}, t_{XTL})		5		15	μs

Notes 1. The oscillator frequency and input frequency indicate only the oscillator characteristics. See the item of AC characteristics for the instruction execution time.

2. The oscillation settling time means the time required for the oscillation to settle after V_{DD} reaches Min. of the oscillation voltage range.

Caution When the subsystem clock oscillator is used, conform to the following guidelines when wiring at the portions of surrounded by dotted lines in the figures above to eliminate the influence of the wiring capacity.

- **The wiring must be as short as possible.**
- **Other signal lines must not run in these areas.**
- **Any line carrying a high fluctuating current must be kept away as far as possible.**
- **The grounding point of the capacitor of the oscillator must have the same potential as that of V_{DD}. It must not be grounded to ground patterns carrying a large current.**
- **No signal must be taken from the oscillator.**

When the subsystem clock is used, pay special attention to its wiring; the subsystem clock oscillator has low amplification to minimize current consumption and is more likely to malfunction due to noise than the main system clock oscillator.

CAPACITANCE (T_a = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input capacitance	C_I	f = 1 MHz 0 V for pins other than pins to be measured			15	pF
Output capacitance	C_O				15	pF
I/O capacitance	C_{IO}				15	pF

DC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}	Ports 2, 3, 8, 9, and 11		$0.7V_{DD}$		V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, and 7 and $\overline{\text{RESET}}$		$0.8V_{DD}$		V_{DD}	V
	V_{IH3}	Ports 4, 5, and 10	Built-in pull-up resistor	$0.7V_{DD}$		V_{DD}	V
			Open drain	$0.7V_{DD}$		10	V
	V_{IH4}	X1, X2, XT1, and XT2		V_{DD} – 0.5		V_{DD}	V
Low-level input voltage	V_{IL1}	Ports 2 to 5 and 8 to 11		0		$0.3V_{DD}$	V
	V_{IL2}	Ports 0, 1, 6, and 7 and $\overline{\text{RESET}}$		0		$0.2V_{DD}$	V
	V_{IL3}	X1, X2, XT1, and XT2		0		0.4	V
High-level output voltage	V_{OH}	V_{DD} = 4.5 to 6.0 V, I_{OH} = –1 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Low-level output voltage	V_{OL}	Ports 3, 4, and 5	V_{DD} = 4.5 to 6.0 V, I_{OL} = 15 mA		0.5	2.0	V
		V_{DD} = 4.5 to 6.0 V, I_{OL} = 1.6 mA				0.4	V
		I_{OL} = 400 μA				0.5	V
		SB0 and SB1	Open drain Pull-up resistor: 1 kΩ or more			$0.2V_{DD}$	V
High-level input leakage current	I_{LIH1}	$V_I = V_{DD}$	Other than X1, X2, XT1, and XT2			3	μA
	I_{LIH2}		X1, X2, XT1, and XT2			20	μA
	I_{LIH3}	V_I = 10 V	Ports 4, 5, and 10 (open drain)			20	μA
Low-level input leakage current	I_{LIL1}	V_I = 0 V	Other than X1, X2, XT1, and XT2			–3	μA
	I_{LIL2}		X1, X2, XT1, and XT2			–20	μA
High-level output leakage current	I_{LOH1}	$V_O = V_{DD}$	Other than ports 4, 5, and 10			3	μA
	I_{LOH2}	V_O = 10 V	Ports 4, 5, and 10 (open drain)			20	μA
Low-level output leakage current	I_{LOL}	V_O = 0 V				–3	μA
Built-in pull-up resistor	R_{U1}	Ports 0, 1, 2, 3, 6, 7, and 8 (excl. P00) V_I = 0 V	V_{DD} = 5.0 V ±10 %	15	40	80	kΩ
			V_{DD} = 3.0 V ±10 %	30		300	kΩ
	R_{U2}	Ports 4, 5, and 10 $V_O = V_{DD}$ – 2.0 V	V_{DD} = 5.0 V ±10 %	15	40	70	kΩ
			V_{DD} = 3.0 V ±10 %	10		60	kΩ
Built-in pull-down resistor	R_D	Port 9 $V_I = V_{DD}$	V_{DD} = 5.0 V ±10 %	10	40	70	kΩ
			V_{DD} = 3.0 V ±10 %	10		60	kΩ

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
Power supply current[Note 1]	I_{DD1}	4.19 MHz[Note 2] crystal resonance C1 = C2 = 22 pF	V_{DD} = 5 V ±10 %[Note 3]			3.2	10	mA
			V_{DD} = 3 V ±10 %[Note 4]			0.25	0.75	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10 %		500	1500	μA
				V_{DD} = 3 V ±10 %		150	450	μA
	I_{DD3}	32.768 kHz[Note 5] crystal resonance	V_{DD} = 3 V ±10 %			15	45	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ±10 %		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ±10 %			0.5	20	μA
			V_{DD} = 3 V ±10 %			0.1	10	μA
				T_a = 25 °C		0.1	5	μA

Notes 1. This current excludes the current which flows through the built-in pull-up resistors.

2. This value applies also when the subsystem clock oscillates.

3. Value when the processor clock control register (PCC) is set to 0011 and the μPD75036 is operated in the high-speed mode

4. Value when the PCC is set to 0000 and the μPD75036 is operated in the low-speed mode

5. This value applies when the system clock control register (SCC) is set to 1001 to stop the main system clock pulse and to start the subsystem clock pulse.

AC CHARACTERISTICS (T_a = -40 to +85 °C, V_{DD} = 2.0 to 6.0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
CPU clock cycle time (minimum instruction execution time = 1 machine cycle)**Note 1**	t_{CY}	Operated by main system clock pulse	V_{DD} = 4.5 to 6.0 V	0.95		64	μs
				3.8		64	μs
		Operated by subsystem clock pulse		114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V		0		1	MHz
				0		275	kHz
TI0 input high/low level width	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V		0.48			μs
				1.8			μs
Interrupt input high/low level width	t_{INTH}, t_{INTL}	INT0		**Note 2**			μs
		INT1, INT2, and INT4		10			μs
		KR0 to KR7		10			μs
$\overline{\text{RESET}}$ low level width	t_{RSL}			10			μs

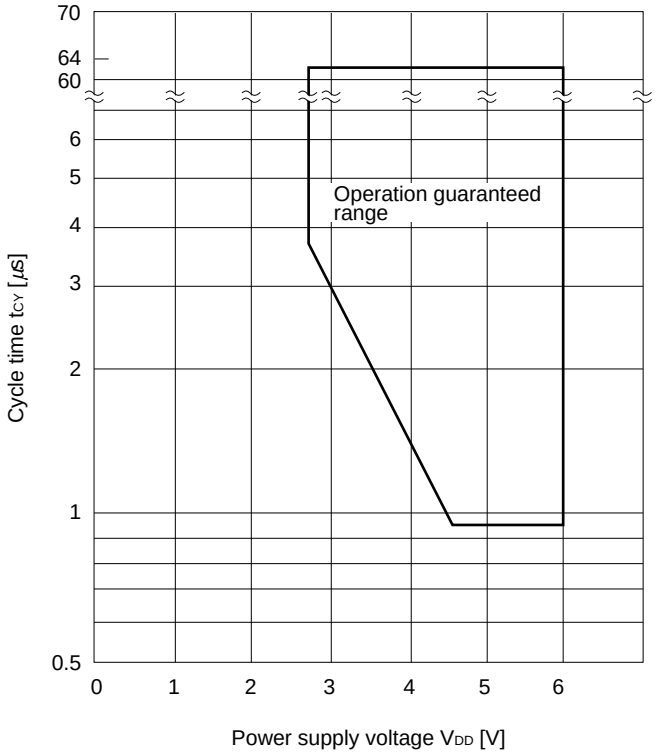
Notes 1. The cycle time of the CPU clock (Φ) depends on the connected resonator frequency, the system clock control register (SCC), and the processor clock control register (PCC).

The figure on the right side shows the cycle time t_{CY} characteristics for the supply voltage V_{DD} during main system clock operation.

2. This value becomes $2t_{CY}$ or $128/f_X$ according to the setting of the interrupt mode register (IM0).

t_{CY} vs V_{DD}

(Main system clock in operation)



Serial transfer operation

Two-wire and three-wire serial I/O modes ($\overline{SCK}$ ... Internal clock output):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY1}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL1}	V_{DD} = 4.5 to 6.0 V		$t_{KCY1}/2 - 50$			ns
	t_{KH1}			$t_{KCY1}/2 - 150$			ns
SI setup time (referred to $\overline{SCK}\uparrow$)	t_{SIK1}			150			ns
SI hold time (referred to $\overline{SCK}\uparrow$)	t_{KSI1}			400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO1}	R_L = 1 kΩ, C_L = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns

Two-wire and three-wire serial I/O modes ($\overline{SCK}$ ... External clock input):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY2}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL2}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH2}			1600			ns
SI setup time (referred to $\overline{SCK}\uparrow$)	t_{SIK2}			100			ns
SI hold time (referred to $\overline{SCK}\uparrow$)	t_{KSI2}			400			ns
Delay time from $\overline{SCK}\downarrow$ to SO output	t_{KSO2}	R_L = 1 kΩ, C_L = 100 pF[Note]	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns

Note R_L and C_L are the resistance and capacitance of the SO output line load respectively.

SBI mode ($\overline{SCK}$ ... Internal clock output (master)):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY3}	V_{DD} = 4.5 to 6.0 V		1600			ns
				3800			ns
$\overline{SCK}$ high/low level width	t_{KL3}	V_{DD} = 4.5 to 6.0 V		t_{KCY3}/2 - 50			ns
	t_{KH3}			t_{KCY3}/2 - 150			ns
SB0/SB1 setup time (referred to $\overline{SCK}$↑)	t_{SIK3}			150			ns
SB0/SB1 hold time (referred to $\overline{SCK}$↑)	t_{KSI3}			t_{KCY3}/2			ns
Delay time from $\overline{SCK}$↓ to SB0/SB1 output	t_{KSO3}	R_L = 1 kΩ, C_L = 100 pF**Note**	V_{DD} = 4.5 to 6.0 V	0		250	ns
				0		1000	ns
From $\overline{SCK}$↑ to SB0/SB1↓	t_{KSB}			t_{KCY3}			ns
From SB0/SB1↓ to $\overline{SCK}$↓	t_{SBK}			t_{KCY3}			ns
SB0/SB1 low level width	t_{SBL}			t_{KCY3}			ns
SB0/SB1 high level width	t_{SBH}			t_{KCY3}			ns

SBI mode ($\overline{SCK}$ ... External clock input (slave)):

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY4}	V_{DD} = 4.5 to 6.0 V		800			ns
				3200			ns
$\overline{SCK}$ high/low level width	t_{KL4}	V_{DD} = 4.5 to 6.0 V		400			ns
	t_{KH4}			1600			ns
SB0/SB1 setup time (referred to $\overline{SCK}$↑)	t_{SIK4}			100			ns
SB0/SB1 hold time (referred to $\overline{SCK}$↑)	t_{KSI4}			t_{KCY4}/2			ns
Delay time from $\overline{SCK}$↓ to SB0/SB1 output	t_{KSO4}	R_L = 1 kΩ, C_L = 100 pF**Note**	V_{DD} = 4.5 to 6.0 V	0		300	ns
				0		1000	ns
From $\overline{SCK}$↑ to SB0/SB1↓	t_{KSB}			t_{KCY4}			ns
From SB0/SB1↓ to $\overline{SCK}$↓	t_{SBK}			t_{KCY4}			ns
SB0/SB1 low level width	t_{SBL}			t_{KCY4}			ns
SB0/SB1 high level width	t_{SBH}			t_{KCY4}			ns

Note R_L and C_L are the resistance and capacitance of the SB0/SB1 output line load respectively.

A/D converter (T_a = -40 to +85 °C, V_{DD} = 2.7 to 6.0 V, AV_{SS} = V_{SS} = 0 V)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution				8	8	8	bit
Absolute accuracy**Note 1**		2.5 V ≤ AV_{REF} ≤ V_{DD}	-10 ≤ Ta ≤ +85°C			±1.5	LSB
			-40 ≤ Ta < -10°C			±2.0	
Conversion time**Note 2**	t_{CONV}					168/f_X	μs
Sampling time**Note 3**	t_{SAMP}					44/f_X	μs
Analog input voltage	V_{IAN}			AV_{REF-}		AV_{REF+}	V
Analog power supply voltage	AV_{DD}			2.5		V_{DD}	V
Reference input voltage**Note4**	AV_{REF+}	2.5 V ≤ (AV_{REF} +) – (AV_{REF} -)		2.5		AV_{DD}	V
Reference output voltage**Note 4**	AV_{REF-}	2.5 V ≤ (AV_{REF} +) – (AV_{REF} -)		0		1.0	V
Analog input impedance	R_{AN}				1000		MΩ
AV_{REF} current	AI_{REF}				1.0	2.0	mA

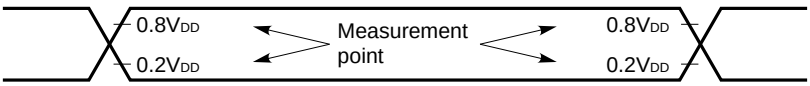
Notes 1. Absolute accuracy excluding quantization error (±1/2 LSB)

2. Time from the execution of a conversion start instruction till the end of conversion (EOC = 1) (40.1 μs: f_X = 4.19 MHz)

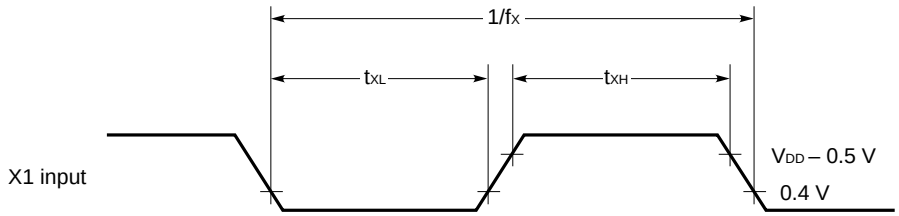
3. Time from the execution of a conversion start instruction till the end of sampling (10.5 μs: f_X = 4.19 MHz)

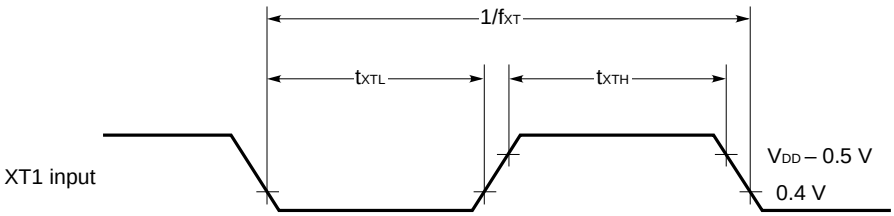
4. The value resulting from subtracting (AV_{REF-}) from (AV_{REF+}) must be greater than or equal to 2.5 V.

AC Timing Measurement Points (Excluding (X1 and XT1 Inputs)

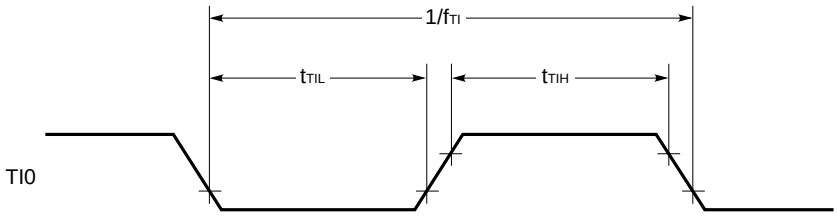


Clock Timing



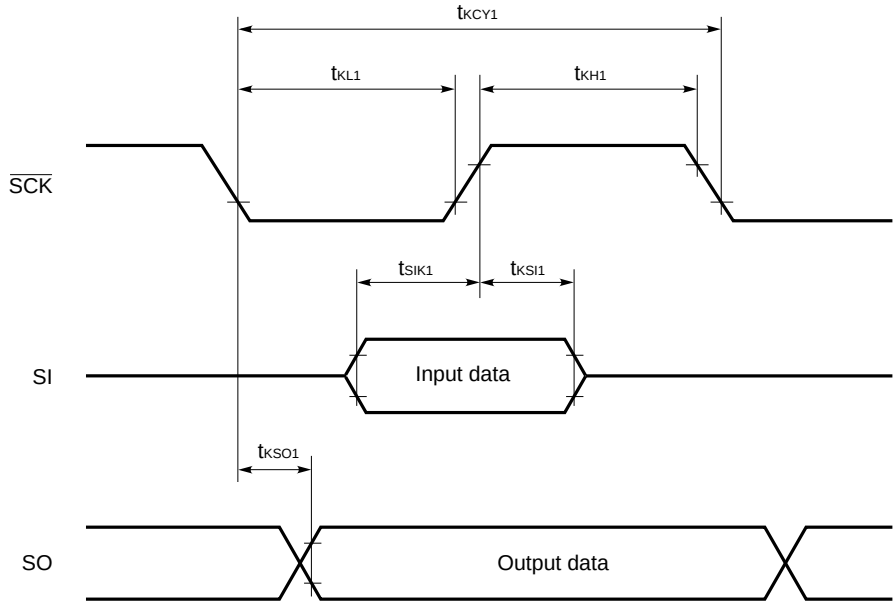


TI0 Timing

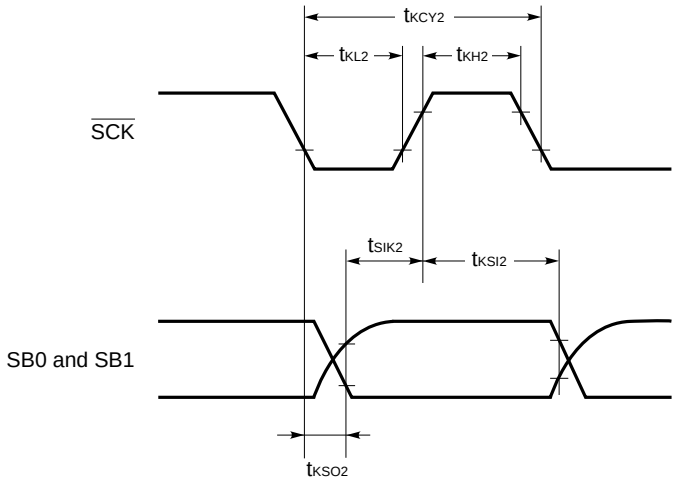


Serial Transfer Timing

Three-wire serial I/O mode:

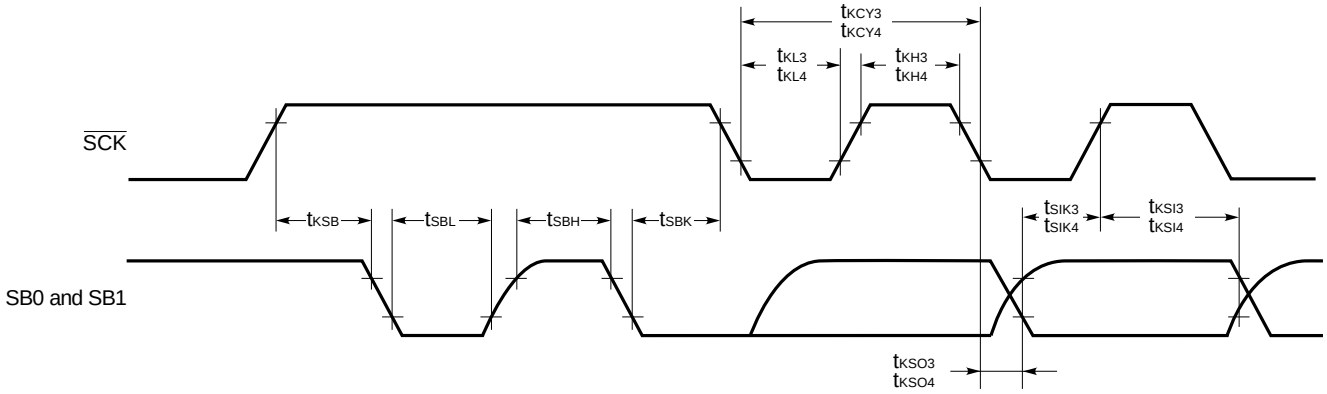


Two-wire serial I/O mode:

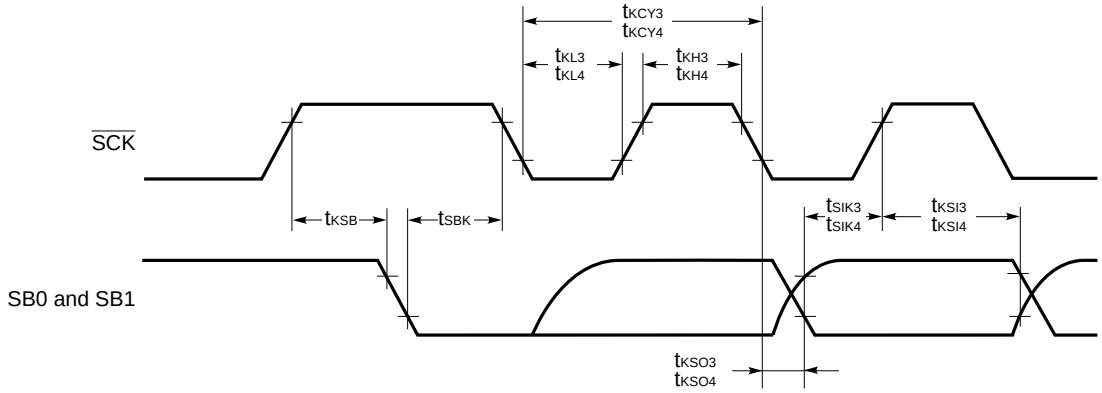


Serial Transfer Timing

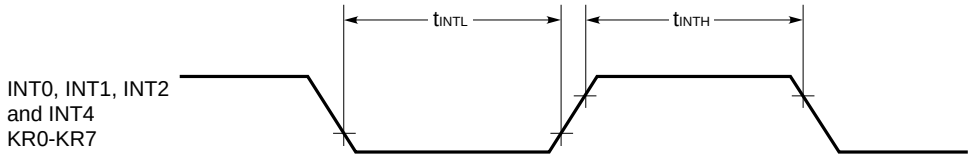
Bus release signal transfer:



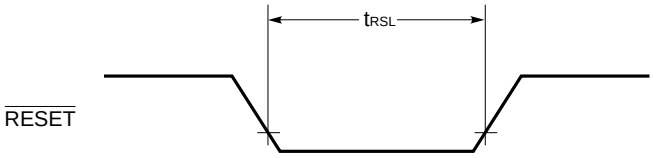
Command signal transfer:



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



DATA HOLD CHARACTERISTICS BY LOW SUPPLY VOLTAGE IN DATA MEMORY STOP MODE

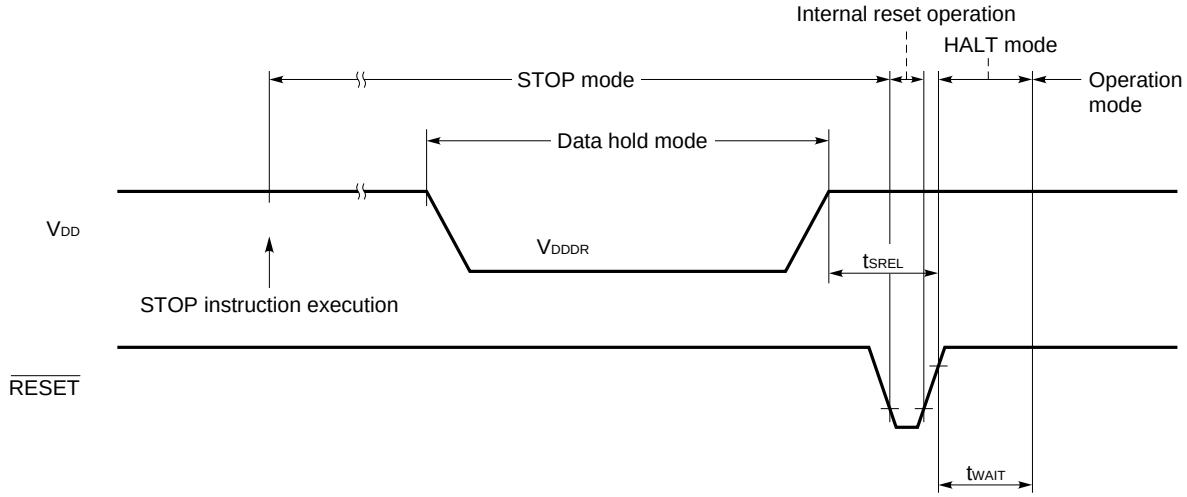
(T_a = -40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data hold supply voltage	V_{DDDR}		2.0		6.0	V
Data hold supply current **Note 1**	I_{DDDR}	V_{DDDR} = 2.0 V		0.1	10	μA
Release signal setting time	t_{SREL}		0			μs
Oscillation settling time **Note 2**	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/f_X$		ms
		Release by interrupt request		**Note 3**		ms

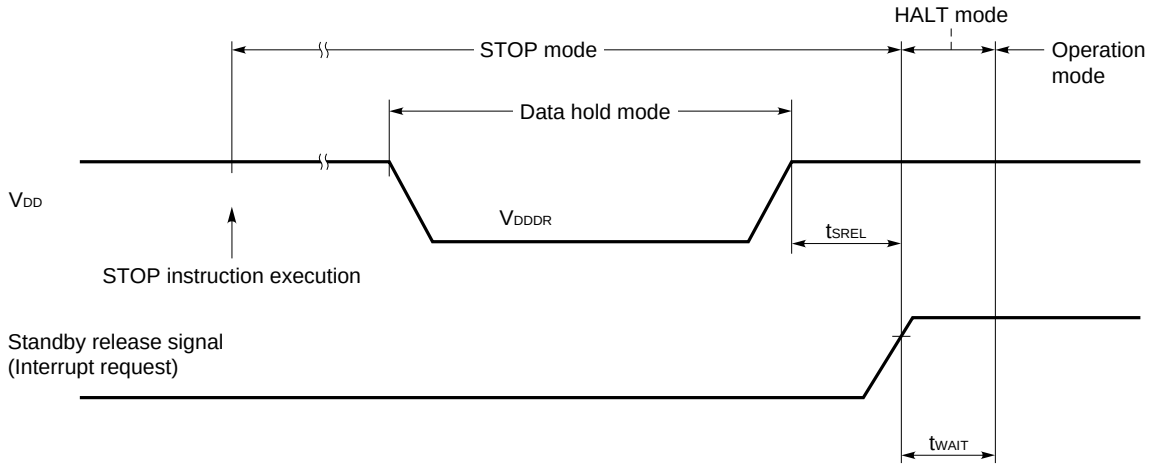
Notes 1. Excluding the current which flows through the built-in pull-up resistors
2. CPU operation stop time for preventing unstable operation at the beginning of oscillation
3. This value depends on the settings of the basic interval timer mode register (BTM) shown below.

BTM3	BTM2	BTM1	BTM0	Wait time (Values at fx = 4.19 MHz in parentheses)
—	0	0	0	$2^{20}/f_X$ (approx. 250 ms)
—	0	1	1	$2^{17}/f_X$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/f_X$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/f_X$ (approx. 1.95 ms)

Data Hold Timing (STOP Mode Release by $\overline{RESET}$)

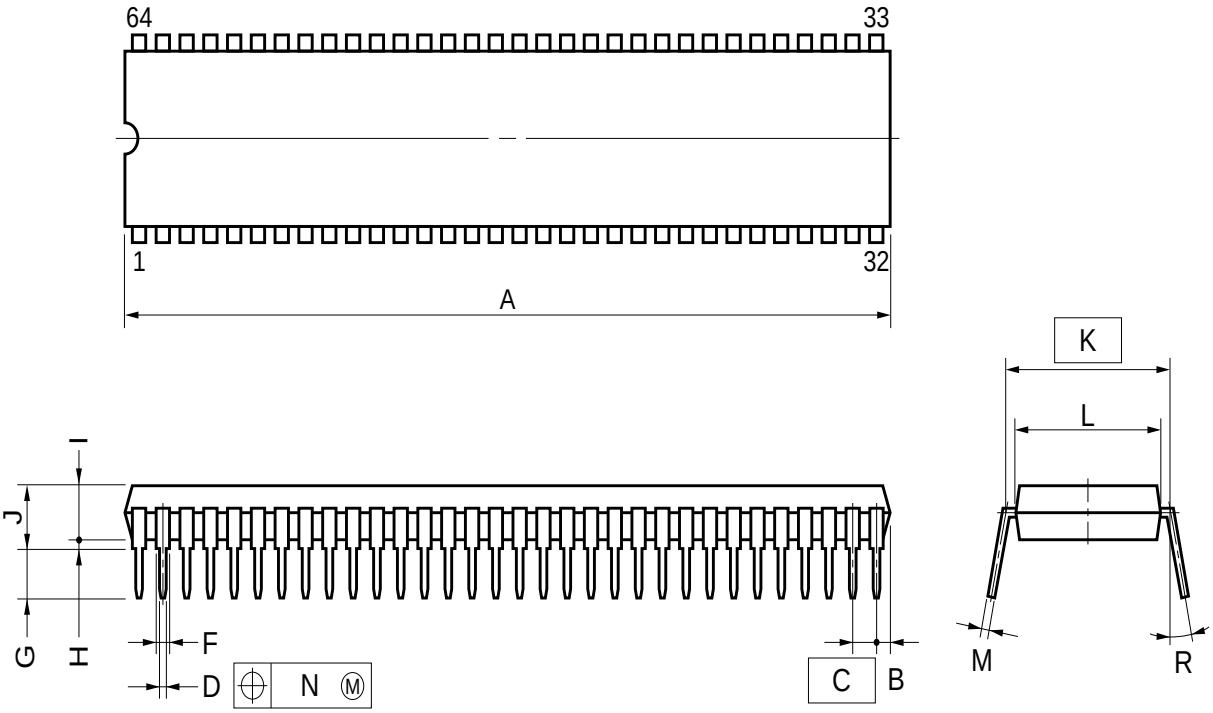


Data Hold Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



11. PACKAGE DIMENSIONS

64 PIN PLASTIC SHRINK DIP (750 mil)



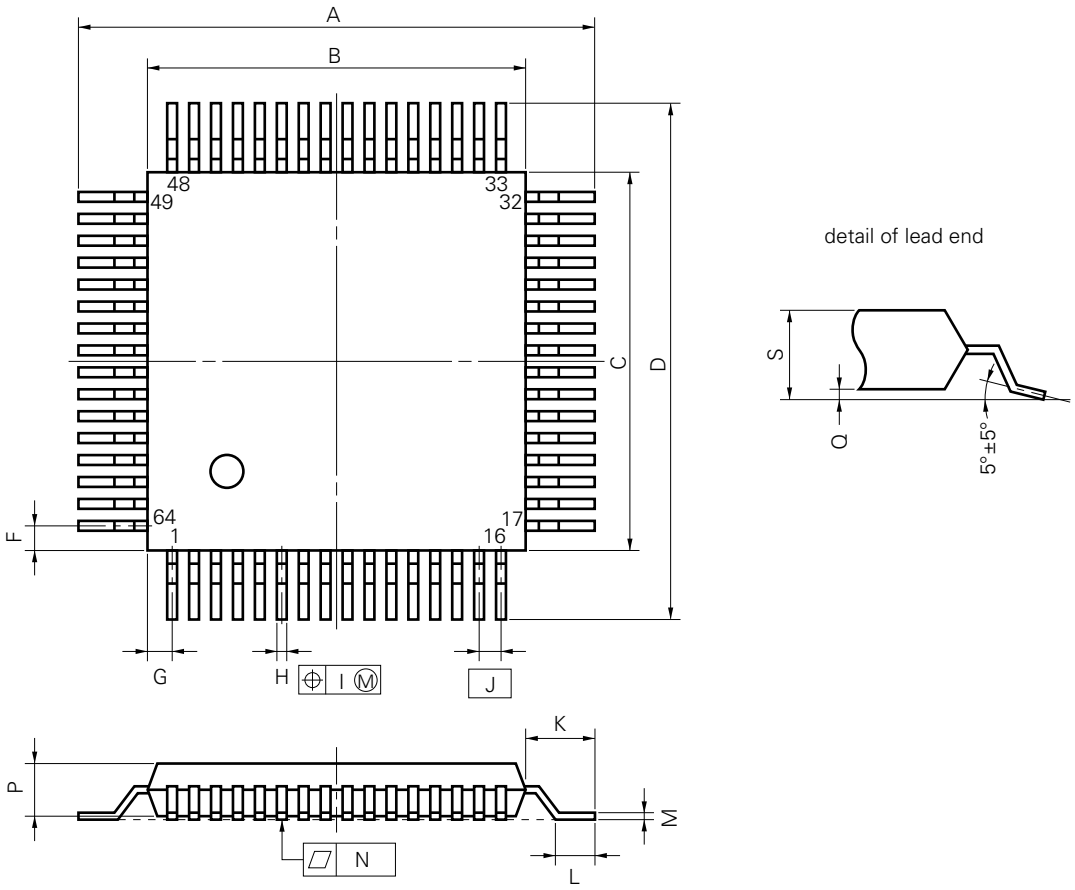
NOTE

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QFP (□14)



P64GC-80-AB8-3

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	17.6±0.4	0.693±0.016
B	14.0±0.2	$0.551^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.35±0.10	$0.014^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.8 (T.P.)	0.031 (T.P.)
K	1.8±0.2	0.071±0.008
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.55	0.100
Q	0.1±0.1	0.004±0.004
S	2.85 MAX.	0.112 MAX.

★ APPENDIX A DEVELOPMENT TOOLS

The following development tools are provided for developing systems including the μPD75036:

Hardware	IE-75000-R[Note 1] IE-75001-R	In-circuit emulator for the 75X series
	IE-75000-R-EM[Note 2]	Emulation board for the IE-75000-R and IE-75001-R
	EP-75028CW-R	Emulation probe for the μPD75036CW
	EP-75028GC-R EV-9200GC-64	Emulation probe for the μPD75036GC. A 64-pin conversion socket, the EV-9200GC-64, is attached to the probe.
	PG-1500	PROM programmer
	PA-75P036CW	PROM programmer adapter for the μPD75P036CW. Connected to the PG-1500.
	PA-75P036GC	PROM programmer adapter for the μPD75P036GC. Connected to the PG-1500.
Software	IE control program	Host machine • PC-9800 series (MS-DOS™ Ver. 3.30 to Ver. 5.00A[Note 3]) • IBM PC/AT™ series (PC DOS™ Ver. 3.10)
	PG-1500 controller	
	RA75X relocatable assembler	

Notes 1. Maintenance service only

2. Not contained in the IE-75001-R

3. These software cannot use the task swap function, which is available in MS-DOS Ver. 5.00 and Ver. 5.00A.

APPENDIX B RELATED DOCUMENTS ★

Documents related to the device

Document Name	Document No.
User's manual	IEU-1294
Application note	IEM-1294
75X series selection guide	IF-1027

Documents related to development tools

	Document Name		Document No.
Hardware	IE-75000-R User's Manual		EEU-1297
	IE-75001-R User's Manual		EEU-1416
	IE-75000-R-EM User's Manual		EEU-1294
	EP-75028CW-R User's Manual		EEU-1314
	EP-75028GC-R User's Manual		EEU-1306
	PG-1500 User's Manual		EEU-1335
Software	RA75X Assembler Package User's Manual	Operation	EEU-1346
		Language	EEU-1363
	PG-1500 Controller User's Manual		EEU-1291

Other documents

Document Name	Document No.
PACKAGE MANUAL	IEI-1213
SMD SURFACE MOUNT TECHNOLOGY MANUAL	IEI-1207
QUALITY GRADES ON NEC SEMICONDUCTOR DEVICES	IEI-1209
NEC SEMICONDUCTOR DEVICE RELIABILITY/QUALITY CONTROL SYSTEM	IEI-1203
ELECTROSTATIC DISCHARGE (ESD) TEST	IEI-1201
GUIDE TO QUALITY ASSURANCE FOR SEMICONDUCTOR DEVICES	MEI-1202

Caution The above documents may be revised without notice. Use the latest versions when you design an application system.

[MEMO]

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins.

Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

[MEMO]

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