300mA High Speed LDO Regulator, Low ESR Capacitance Compatible, with On/Off Switch

LM6219-3.3N5

General Description

The LM6219-3.3N5 is highly accurate and low noise CMOS LDO voltage regulator. It offers low output noise, high ripple rejection ratio, low dropout and very fast turn-on times.
Internally LM6219-3.3N5 includes a reference voltage source, error amplifiers, driver transistors, current limiters and phase compensators. The current limiter's foldback circuit also operates as a short protect for the output current limiter and the output pin. The output voltage is set by laser trimming. LM6219-3.3N5 is fully compatible with low ESR ceramic capacitors, reducing cost and improving output stability. This high level of stability is maintained even during frequent load fluctuations, due to the excellent transient response performance and high PSRR achieved across a broad range of frequencies.
The CE function allows the output of regulator to be turned off, resulting in greatly reduced power consumption.
The LM6219-3.3N5 is available in SOT-23-5L package.

Features

- Maximum output current : 300mA
- High accuracy : ±1%
- Standby current : less than 0.1μA typ.
- Operating temperature range : -40~+85°C
- Ultra small package
- Dropout voltage : 200mV@100mA
- Low power consumption : 25μA typ.
- High ripple rejection : 65dB@10kHz
- Low ESD capacitor : ceramic capacitor compatible
- RoHS compliant, Pb-free package

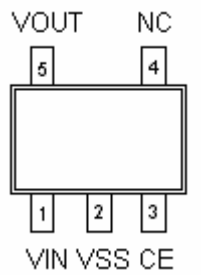
Applications

- Mobile phones
- Portable games
- Reference voltage sources
- Cordless phones, radio communication equipment
- Cameras, video cameras
- Battery powered equipments

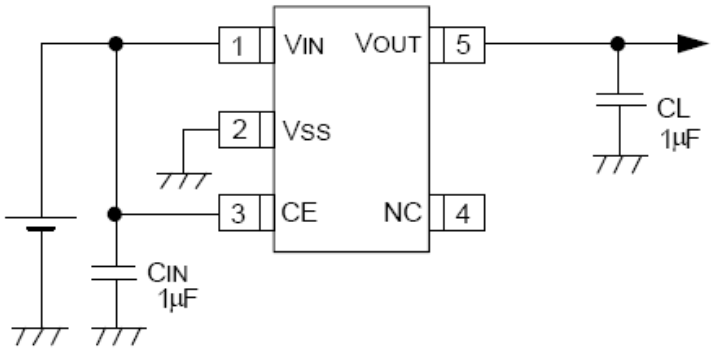
Ordering Information

Part Number	Package	Shipping
LM6219-3.3N5	SOT-23-5L (RoHS compliant package)	3000 pcs / Tape & Reel

Pin Configuration



Typical Application Circuit



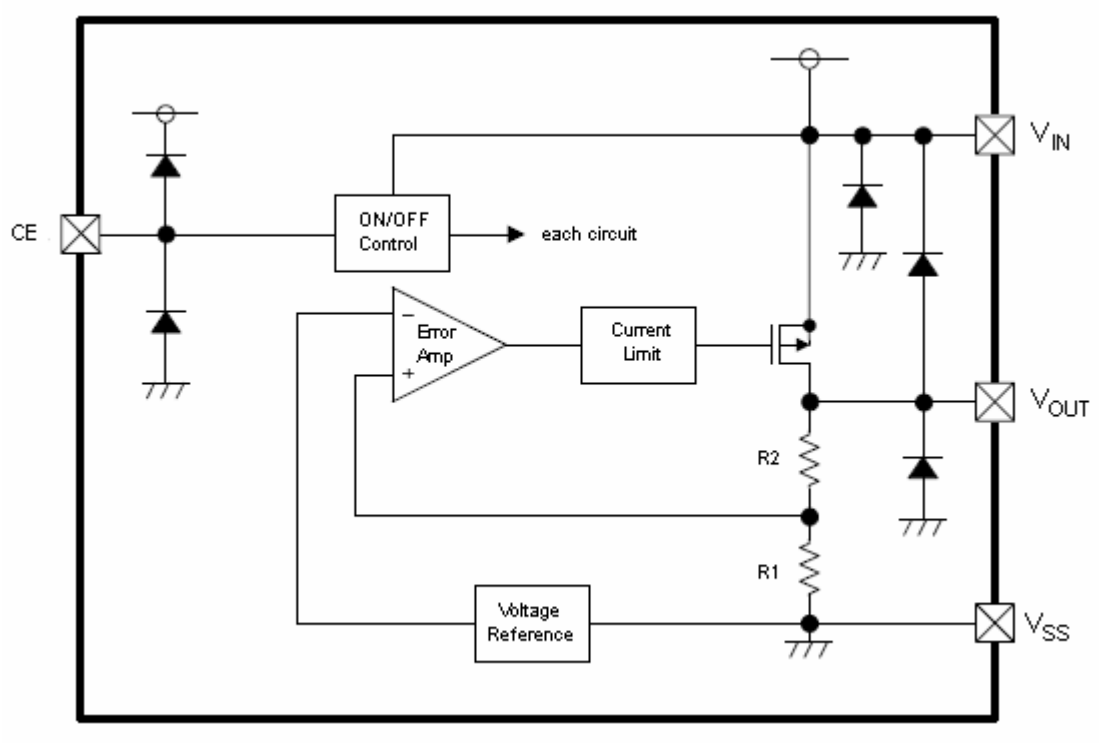
Pin Assignment

Pin Name	Pin No.	Pin Function
VIN	1	**Power Input**
VSS	2	**Ground**.
CE	3	**ON/OFF Control**
NC	4	**No Connection**
VOUT	5	**Output**

Absolute Maximum Ratings

Parameter	Symbol	Ratings	Units
Input Voltage	V_{IN}	7	V
Output Current	I_{OUT}	300	mA
Output Voltage	V_{OUT}	Vss-0.3～Vin+0.3	V
CE Pin Voltage	V_{CE}	Vss-0.3～Vin+0.3	V
Continuous Total Power Dissipation	P_D	250	mW
Operating Temperature Range	Topr	-40～+85	℃
Storage Temperature Range	Tstg	-55～+125	℃

Function Block Diagram

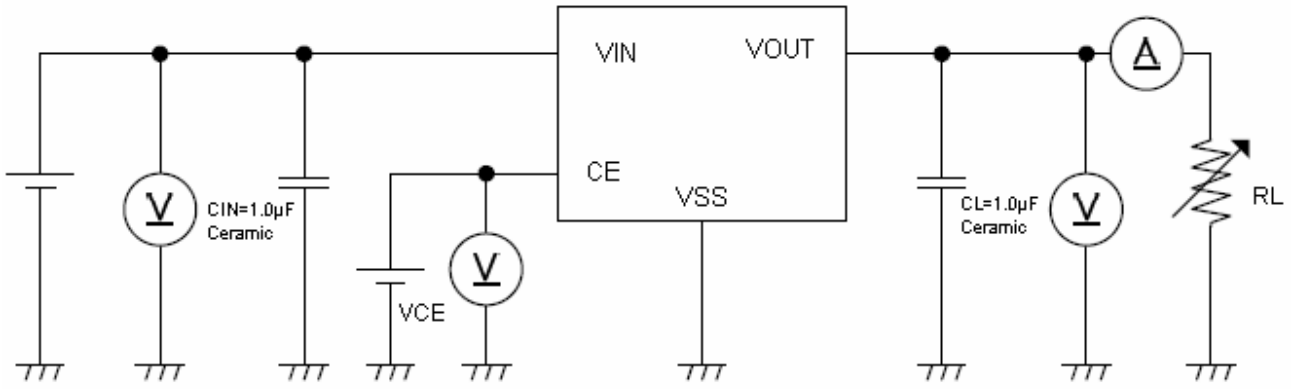


Electrical Characteristics @ T_A=25℃, V_{IN}=4.3V, unless otherwise specified

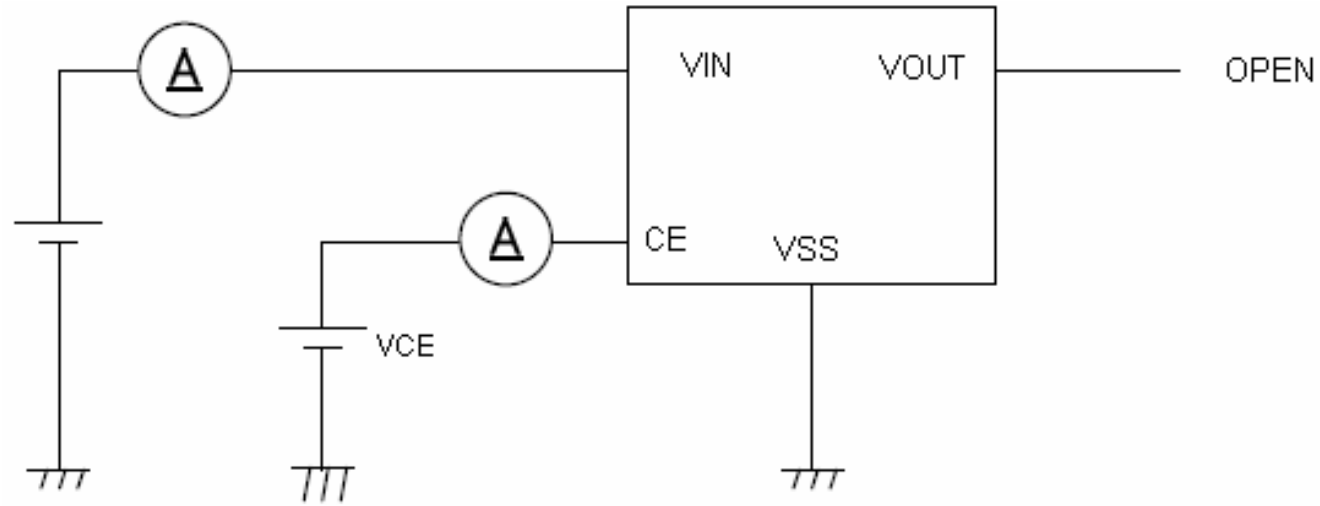
Parameter	Symbol	Test Conditions	Min	Typ	Max	Units	Circuits
Output Voltage	V_{OUT}	I_{OUT}= 30mA	3.267	3.300	3.333	V	①
Maximum Output Current	I_{OUTMAX}	V_{IN}=4.3V	300	-	-	mA	①
Load Regulation	ΔV_{OUT}	1mA≦I_{OUT}≦100mA	-	15	50	mV	①
Load Regulation 2	ΔV_{OUT2}	1mA≦I_{OUT}≦300mA	-	-	100	mV	①
Dropout Voltage	Vdif1	I_{OUT}=30mA	-	60	90	mV	①
	Vdif2	I_{OUT}=100mA	-	200	250	mV	①
Supply	I_{DD}	V_{CE}=V_{IN}=4.3V	-	25	50	μA	②
Stand-by Current	I_{STB}	V_{IN}=4.3V, V_{CE}=V_{SS}		0.01	0.1	μA	②
Line Regulation	$\Delta V_{OUT}/(\Delta V_{IN}\cdot V_{OUT})$	4.3V≦V_{IN}≦6V, I_{OUT}=30mA	-	0.01	0.2	%/V	①
Input Voltage	V_{IN}	-	2	-	6	V	-
Output Voltage Temperature Characteristics	$\Delta V_{OUT}/(\Delta Topr\cdot V_{OUT})$	I_{OUT}=30mA, -40℃≦Topr≦85℃	-	±100	-	ppm/℃	①
Power Supply Rejection Ratio	PSRR	V_{IN}=4.3V+1.0Vp-pAC I_{OUT}=50mA,f=10kHz	-	70	-	dB	③
Current Limiter	Ilim	V_{CE}=V_{IN}=4.3V	-	380	-	mA	①
Short Circuit Current	I_{SHORT}	V_{CE}=V_{IN}=4.3V	-	50	-	mA	①
CE 'High' Level	V_{CEH}	-	1.6	-	V_{IN}	V	①
CE 'Low' Level	V_{CEL}	-	-	-	0.25	V	①
CE 'High' Level Current	I_{CEH}	V_{CE}=V_{IN}=4.3V	-0.1	-	0.1	μA	②
CE 'Low' Level Current	I_{CEL}	V_{IN}=4.3V, V_{CE}=V_{SS}	-0.1	-	0.1	μA	②

Test Circuits

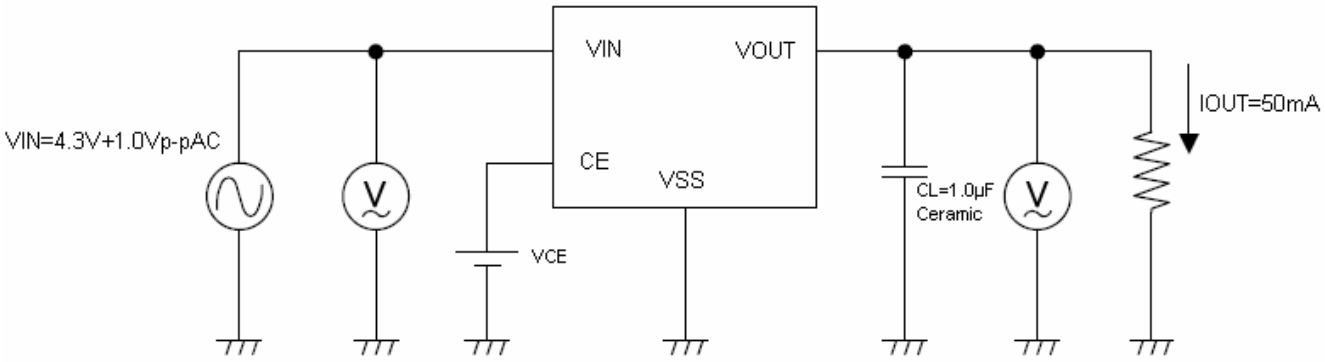
Circuit ①



Circuit ②



Circuit ③



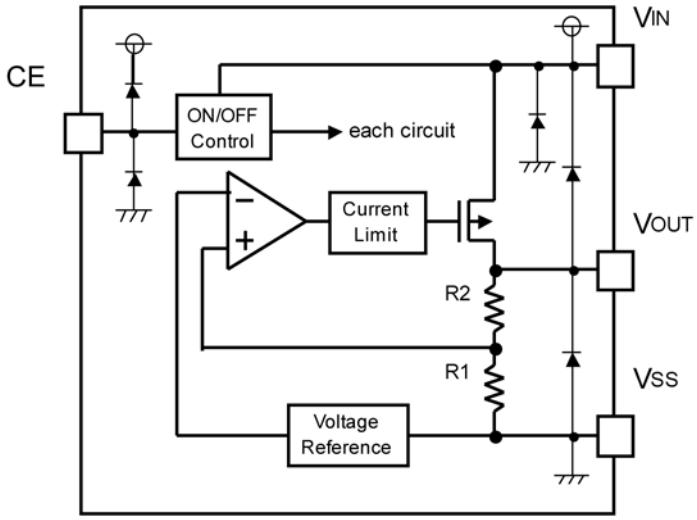
*Test Circuit VCE(CE Pin Voltage)

Active $V_{CE}=V_{IN}$; Standby $V_{CE}=V_{SS}$

Operational Explanation

•Output Voltage Control

The voltage divided by resistors R1 & R2 is compared with the internal reference voltage by the error amplifier. The P-channel MOSFET, which is connected to the V_{OUT} pin, is then driven by the subsequent output signal. The output voltage at the V_{OUT} pin is controlled and stabilized by a system of negative feedback. The current limit circuit and short protect circuit operate in relation to the level of output current. Further, the IC's internal circuitry can be shutdown via the CE pin's signal



•Low ESR Capacitors

With the LM6219-3.3N5, a stable output voltage is achievable even if used with low ESR capacitors as a phase compensation circuit is built-in. In order to ensure the effectiveness of the phase compensation, we suggest that an output capacitor (C_L) is connected as close as possible to the output pin (V_{OUT}) and the V_{SS} pin. Please use an output capacitor with a capacitance value of at least 1.0μF. Also, please connect an input capacitor (C_{IN}) of 1.0μF between the VIN pin and the VSS pin in order to ensure a stable power input.
Stable phase compensation may not be ensured if the capacitor runs out capacitance when depending on bias and temperature. In case the capacitor depends on the bias and temperature, please make sure the capacitor can ensure the actual capacitance.

•Current Limiter, Short-Circuit Protection

The LM6219-3.3N5 includes a combination of a fixed current limiter circuit & a foldback circuit, which aid the operations of the current limiter and circuit protection. When the load current reaches the current limit level, the fixed current limiter circuit operates and output voltage drops. As a result of this drop in output voltage, the foldback circuit operates, output voltage drops further and output current decreases. When the output pin is shorted, a current of about 50mA flows.

•CE Pin

The IC's internal circuitry can be shutdown via the signal from the CE pin with the LM6219-3.3N5. In shutdown mode, output at the V_{OUT} pin will be pulled down to the VSS level via R1 & R2. The operational logic of the IC's CE pin is selectable (please refer to the selection guide). Although the CE pin is equal to an inverter input with CMOS hysteresis, with either the pull-up or pull-down options, the CE pin input current will increase when the IC is in operation. We suggest that you use this IC with either a V_{IN} voltage or a V_{SS} voltage input at the CE pin. If this IC is used with the correct specifications for the CE pin, the operational logic is fixed and the IC will operate normally. However, supply current may increase as a result of through current in the IC's internal circuitry.

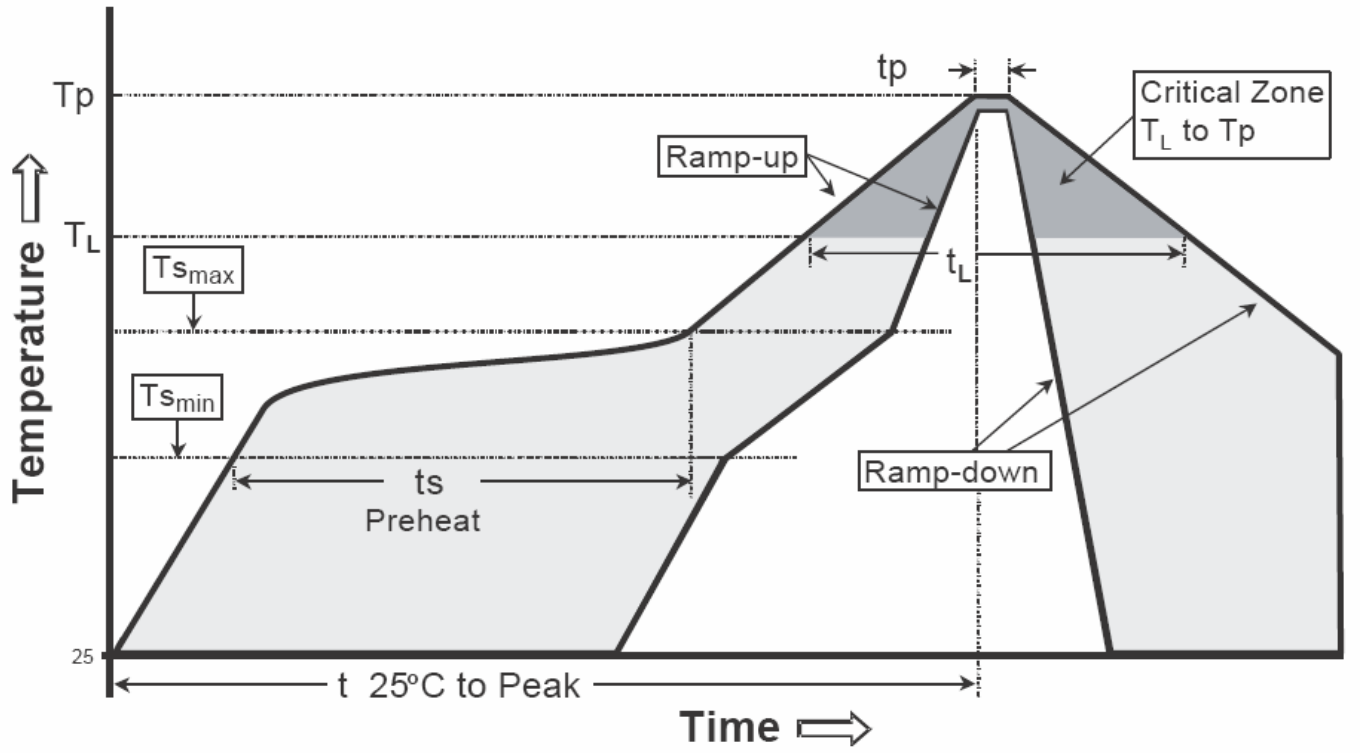
NOTES ON USE

1. For temporary, transitional voltage drop or voltage rising phenomenon, the IC is liable to malfunction should the ratings be exceeded.
2. Where wiring impedance is high, operations may become unstable due to noise and/or phase lag depending on output current. Please keep the resistance low between V_{IN} and V_{SS} wiring in particular.
3. Please wire the input capacitor (C_{IN}) and the output capacitor (C_L) as close to the IC as possible.
4. The IC is controlled with constant current start-up. Start-up sequence control is requested to draw a load current after even nominal output voltage rising up the output voltage.
5. CYS places an importance on improving our products and their reliability. We request that users incorporate fail-safe designs and post-aging protection treatment when using CYS's products in their systems.

Recommended wave soldering condition

Product	Peak Temperature	Soldering Time
Pb-free devices	260 +0/-5 °C	5 +1/-1 seconds

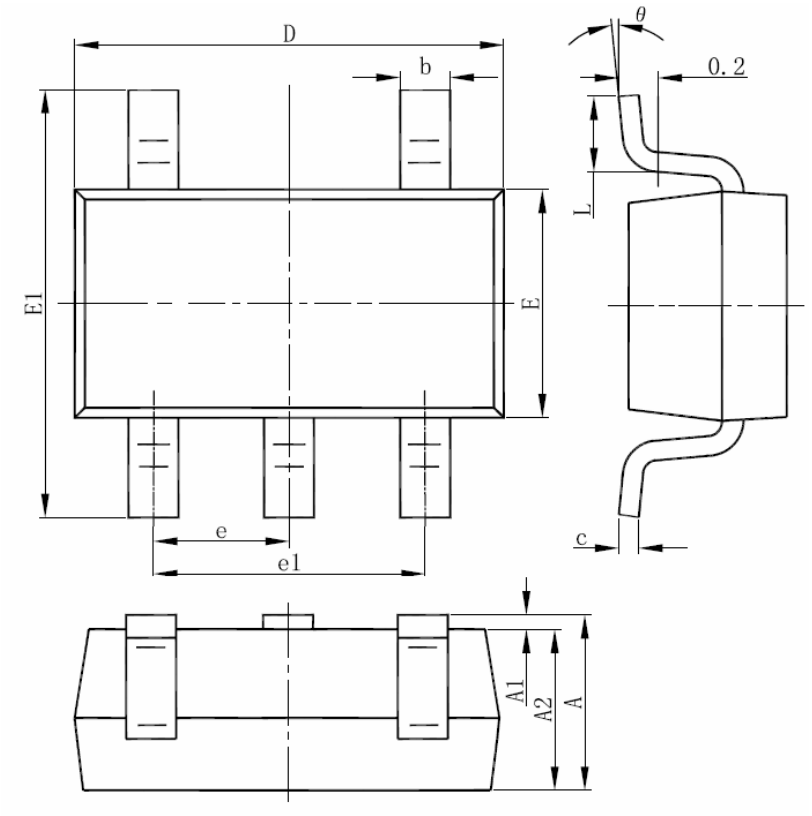
Recommended temperature profile for IR reflow

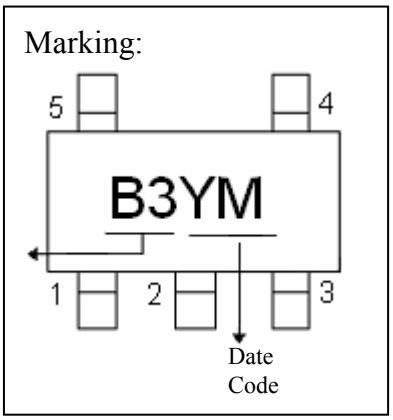


Profile feature	Sn-Pb eutectic Assembly	Pb-free Assembly
Average ramp-up rate (Tsmax to Tp)	3°C/second max.	3°C/second max.
Preheat −Temperature Min(Ts min) −Temperature Max(Ts max) −Time(ts min to ts max)	 100°C 150°C 60-120 seconds	 150°C 200°C 60-180 seconds
Time maintained above: −Temperature (TL) − Time (tL)	 183°C 60-150 seconds	 217°C 60-150 seconds
Peak Temperature(TP)	240 +0/-5 °C	260 +0/-5 °C
Time within 5°C of actual peak temperature(tp)	10-30 seconds	20-40 seconds
Ramp down rate	6°C/second max.	6°C/second max.
Time 25 °C to peak temperature	6 minutes max.	8 minutes max.

Note : All temperatures refer to topside of the package, measured on the package body surface.

SOT-25 Dimension





Device Code

Style:
Pin 1: V_{IN}
Pin 2: V_{SS}
Pin 3: V_{CE}
Pin 4: NC
Pin 5: V_{OUT}

5-Lead SOT-23-5L Plastic Surface Mounted Package
CYStek Package Code:N5

DIM	Millimeters		Inches		DIM	Millimeters		Inches	
	Min.	Max.	Min.	Max.		Min.	Max.	Min.	Max.
A	1.050	1.250	0.041	0.049	E	1.500	1.700	0.059	0.067
A1	0.000	0.100	0.000	0.004	E1	2.650	2.950	0.104	0.116
A2	1.050	1.150	0.041	0.045	e	0.950 (BSC)		0.037 (BSC)	
b	0.300	0.500	0.012	0.020	e1	1.800	2.000	0.071	0.079
c	0.100	0.200	0.004	0.008	L	0.300	0.600	0.012	0.024
D	2.820	3.020	0.111	0.119	θ	0°	8°	0°	8°

Notes : 1.Controlling dimension : millimeters.
2.Maximum lead thickness includes lead finish thickness, and minimum lead thickness is the minimum thickness of base material.
3.If there is any question with packing specification or packing method, please contact your local CYStek sales office.

Material :

- Lead :Pure tin plated.
- Mold Compound : Epoxy resin family, flammability solid burning class:UL94V-0.