

Small Signal Product

Ultra Low Capacitance ESD Protection Array

FEATURES

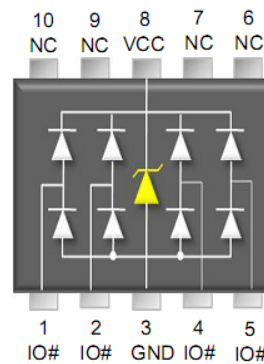
- Meet IEC61000-4-2 (ESD) ±15kV (air), ±8kV (contact)
- Meet IEC61000-4-4 (EFT) rating. 40A (5/50ns)
- Meet IEC61000-4-5 (Lightning) rating. 5A (8/20µs)
- Protects two directional I/O lines
- Working voltage: 5V
- Pb free version and RoHS compliant
- Packing code with suffix "G" means green compound (halogen-free)

MECHANICAL DATA

- Case: MSOP-10 small outline plastic package
- Terminal: Matte tin plated, lead free., solderable per MIL-STD-202, Method 208 guaranteed
- High temperature soldering guaranteed : 260°C/10s
- Weight: 12 ± 0.5 mg
- Marking code: R0544



MSOP-10



MAXIMUM RATINGS AND ELECTRICAL CHARACTERISTICS (T _A =25°C unless otherwise noted)			
PARAMETER	SYMBOL	VALUE	UNIT
Peak Pulse Power (tp=8/20µs waveform)	P _{PP}	125	W
Peak Pulse Current (tp=8/20µs)	I _{PP}	5	A
ESD per IEC 61000-4-2 (Air)	V _{ESD}	± 15	KV
ESD per IEC 61000-4-2 (Contact)		± 8	
Junction and Storage Temperature Range	T _J , T _{STG}	-55 to +150	°C

PARAMETER	SYMBOL	MIN	MAX	UNIT
Reverse Stand-Off Voltage	V _{RWM}	-	5	V
Reverse Breakdown Voltage	V _(BR)	6	-	V
Reverse Leakage Current				
Clamping Voltage	V _C	-	15	V
			20	
Junction Capacitance	C _J	1		pF

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RATINGS AND CHARACTERISTICS CURVES

($T_A=25^\circ\text{C}$ unless otherwise noted)

Fig. 1 Non-Repetitive Peak Pulse Power VS. Pulse Time

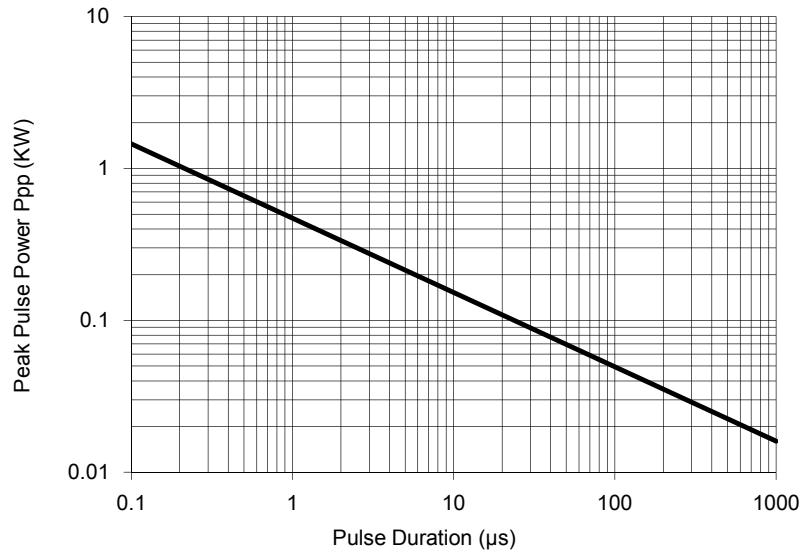


Fig. 2 Pulse Waveform

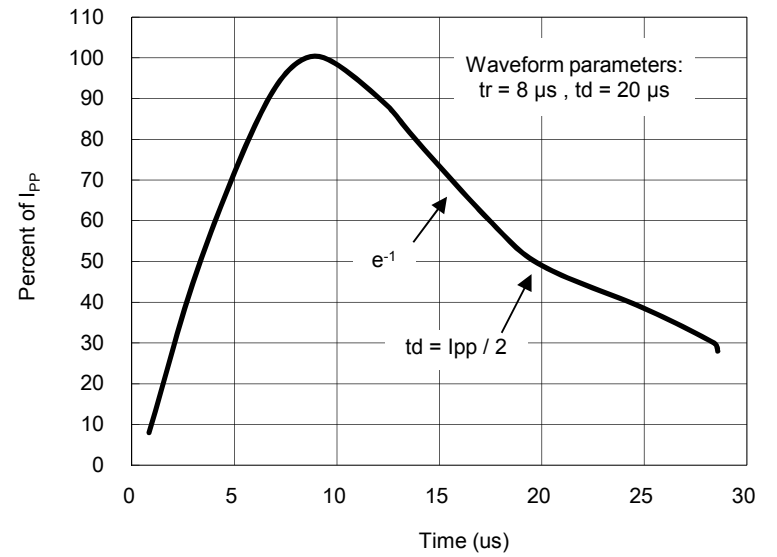


Fig. 3 Admissible Power Dissipation Curve

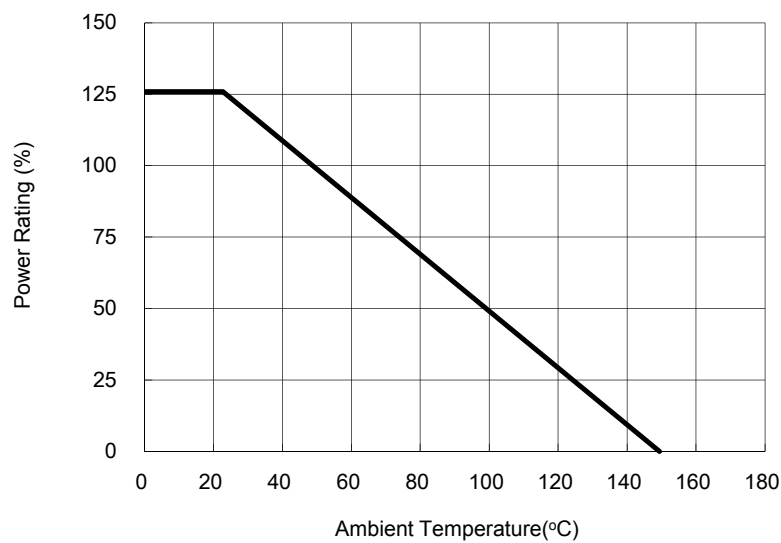


Fig. 4 Typical Junction Capacitance

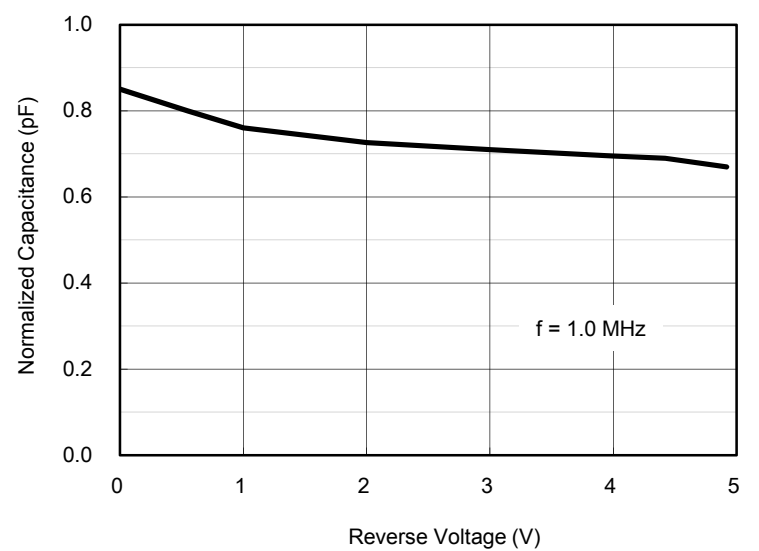
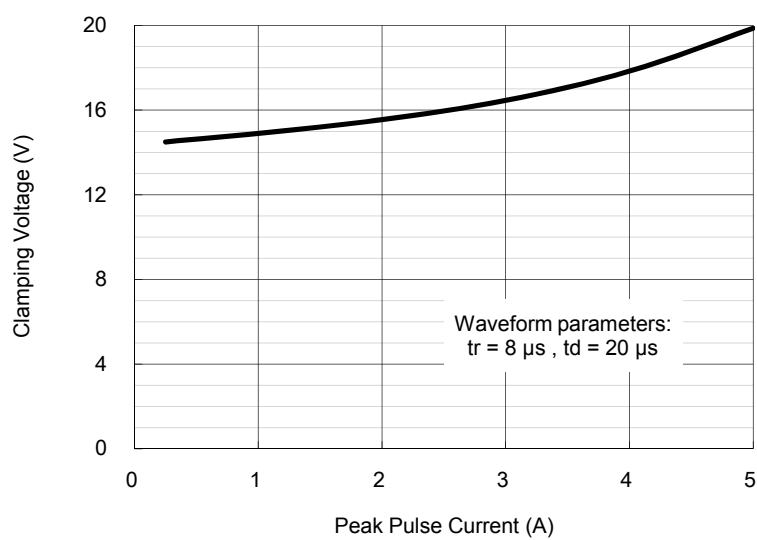
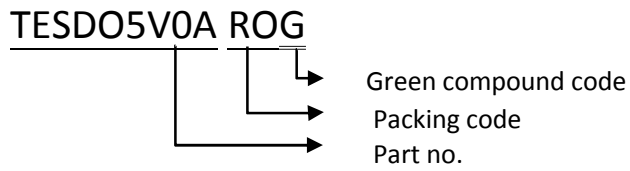


Fig. 5 Clamping Voltage VS. Peak Pulse Current



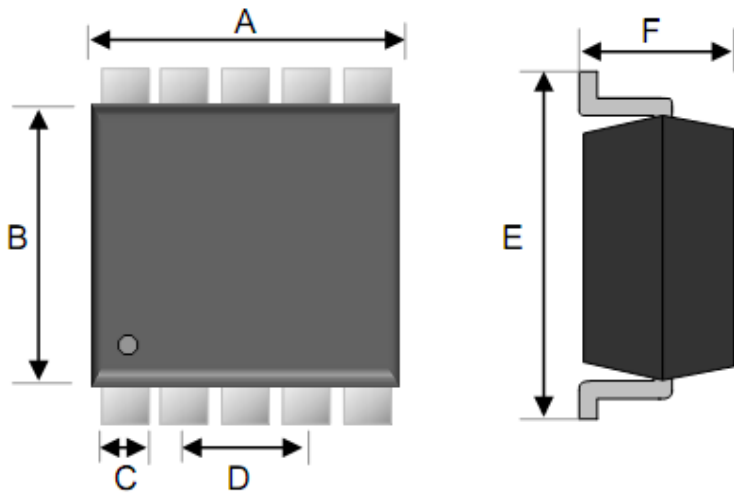
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ORDER INFORMATION (EXAMPLE)



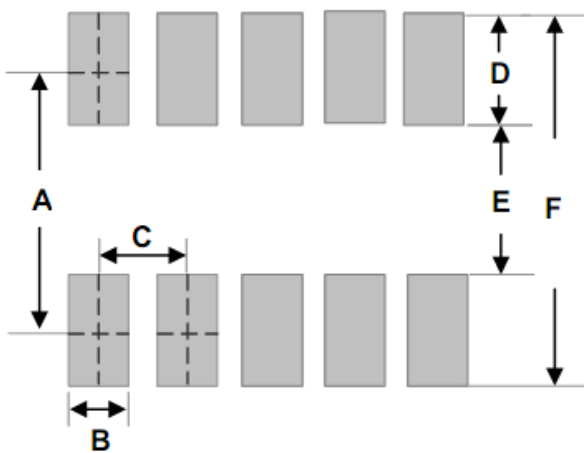
PACKAGE OUTLINE DIMENSIONS

MSOP-10



DIM.	Unit (mm)		Unit (inch)	
	Min	Max	Min	Max
A	2.90	3.10	0.114	0.122
B	2.90	3.10	0.114	0.122
C	0.17	0.27	0.007	0.011
D	0.50 REF		0.020 REF	
E	4.90 REF		0.193 REF	
F	-	1.11	-	0.044

SUGGEST PAD LAYOUT



DIM.	Unit (mm)	Unit (inch)
	Typ.	Typ.
A	4.10	0.161
B	0.30	0.012
C	0.50	0.020
D	1.60	0.063
E	2.50	0.098
F	5.70	0.224

Note: 1. The suggested land pattern dimensions have been provided for reference only, as actual pad layouts may vary depending on application.

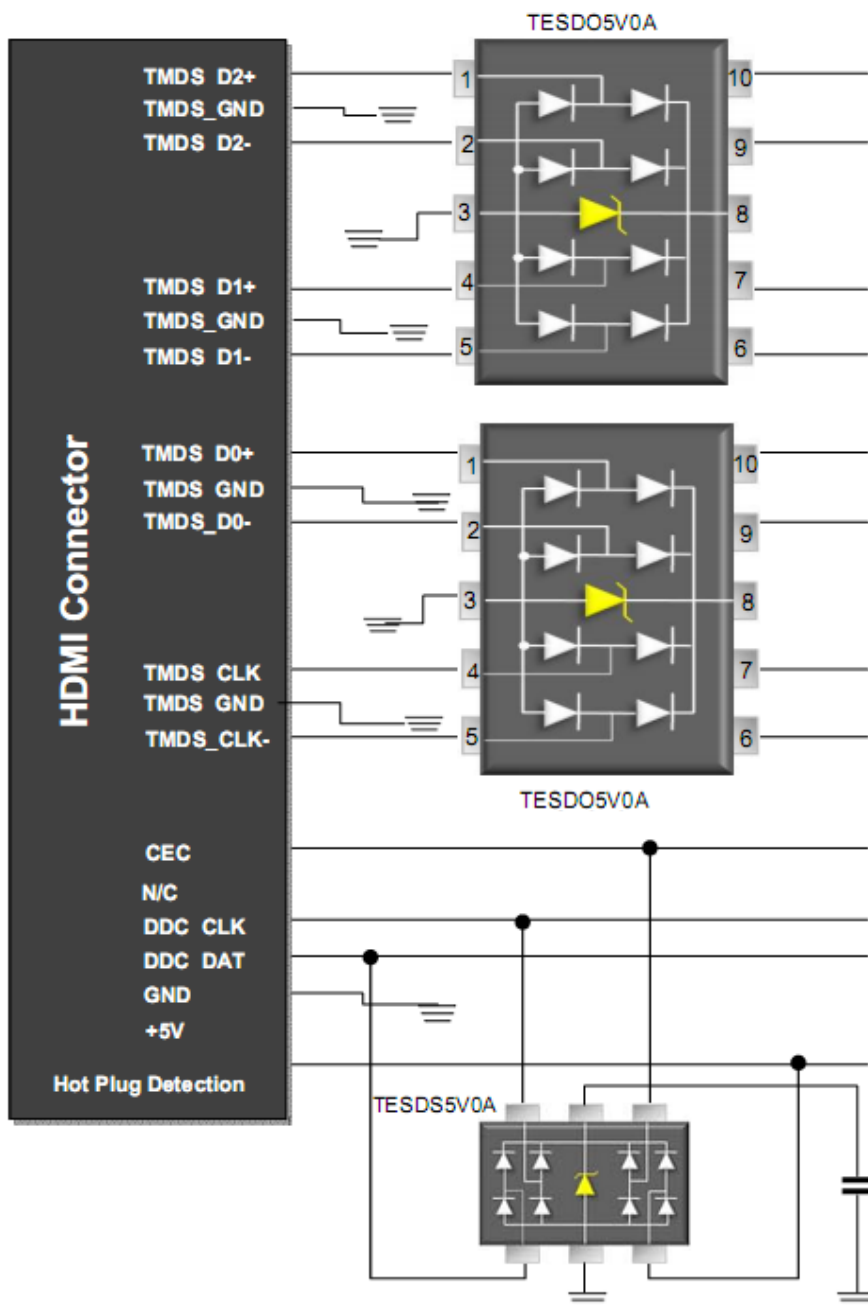
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APPLICATIONS INFORMATION

- ◇ Designed for protection of high-speed interfaces such as HDMI
- ◇ Ultra low capacitance between the pairs while being rated to handle $>\pm 8\text{kV}$, ESD contact discharges and $>\pm 15\text{kV}$ air discharge
- ◇ Each device is in a leadless package that is less than 1.1mm wide
- ◇ Designed such that the traces flow straight through the device. The narrow package and flow-through design reduces discontinuities and minimizes impact on signal integrity
- ◇ TESDO5V0A is ultra low capacitance ESD protection array designed to protect high speed data interfaces
- ◇ The combination of small size, low capacitance, and high level of ESD protection makes them a flexible solution for applications of high speed interface, ex HDMI, DisplayPort™, MDDI, and eSATA interfaces

CIRCUIT BOARD LAYOUT RECOMMENDATIONS FOR HDMI APPLICATION

- ◇ The PCB traces are used to connect the pin pairs for each line (pin 1 to pin 10, pin 2 to pin 9, pin 4 to pin 7, pin 5 to pin 6)
- ◇ Signal line enters at pin 1 and exits at pin 10 and PCB trace connects pin 1 and 10 together. Ground is connected at pins 3 and 8.
- ◇ One large ground pad should be used in lieu of two separate pads.



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