# AN4015
# Application note

## Dual-BTL class-D audio amplifier demonstration board based on the TDA7498E

## Introduction

The purpose of this application note is to describe:

- how to connect the TDA7498 demonstration board
- how to evaluate the performance of the demonstration board using the electrical curves
- how to avoid critical issues in the PCB schematic and layout of the TDA7498E

The TDA7498E represents a new generation of analog input class-D devices from STMicroelectronics and is housed in a PSSO36 package. It is able to deliver 160 W +160 W in stereo configuration with $V_{CC}$ = 36 V and a 4 Ω load[(a)].

**Figure 1. TDA7498E demonstration board**


a. All of the results and graphs included in this document are measured using Audio Precision equipment.

# Contents

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# 1 Overview

The following terms used in this application note are defined as follows:

- THD+N vs. Pout: Total Harmonic Distortion (THD) plus noise versus output power
- THD+N vs. Freq: Total Harmonic Distortion plus noise versus frequency curve
- S/N Ratio: Signal-to-noise ratio
- DNR: Dynamic range
- FFT: Fast Fourier Transform Algorithm (method)
- XTalk: Channel separation L to R, or R to L channel crosstalk

The equipment used includes the following:

- Audio Precision 2722A + AES-17 filter + DCX+ AUX-0025 filter
- DC power supply
- Digital oscilloscope (Tektronix TDS5054B)
- Differential voltage probe (LeCroy AP031)
- Current probe (Tektronix TCP300)

Reference documents include:

- TDA7498E datasheet
- Schematic diagram
- PCB layout
- Test curves

# 2 Test conditions and connections of the demonstration board

## 2.1 Power supply and interface connection

1. Connect PSU to the $V_{CC}$ terminal block
2. Connect the analog input cable to the RCA connectors on the demonstration board, the other side must be connected to a signal source such as the Audio Precision analog outputs or a DVD player

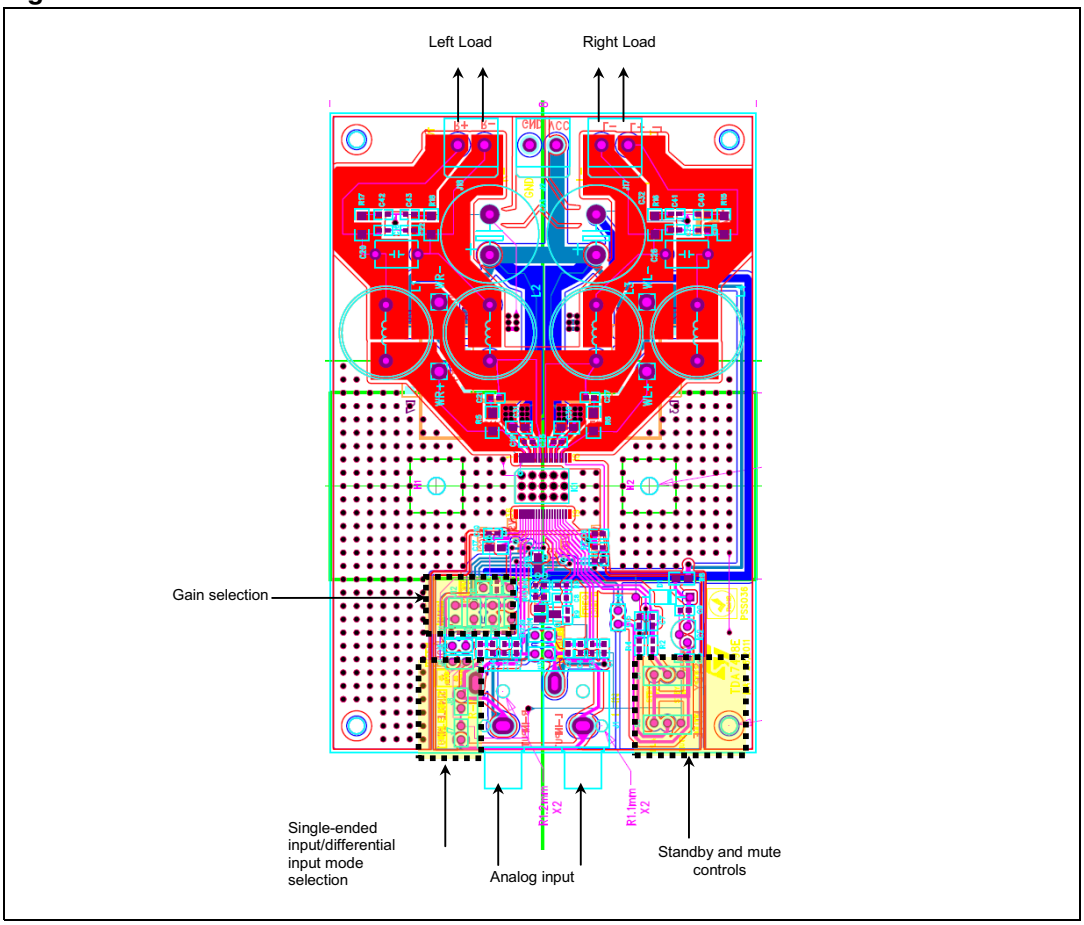
## 2.2 Output configuration

The TDA7498E demonstration board has been configured in 2-channel BTL output.

## 2.3 Connections

The board terminals (top view of demonstration board) are visible in *Figure 2*.

**Figure 2. TDA7498E demonstration board connections**



# 3 Schematic diagram and PCB layout

**Figure 3. TDA7498E schematic**

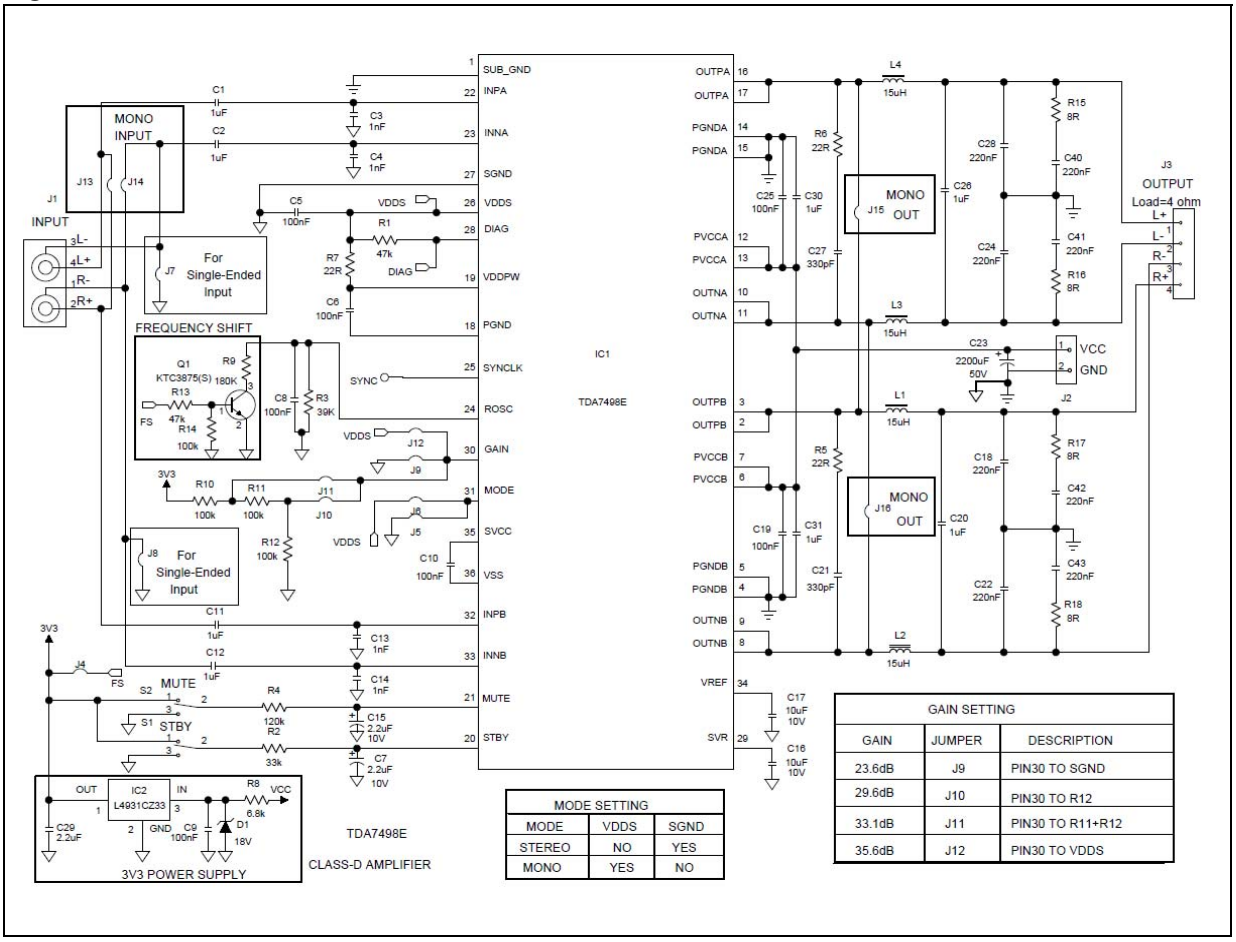


Figure 4. PCB layout - top side

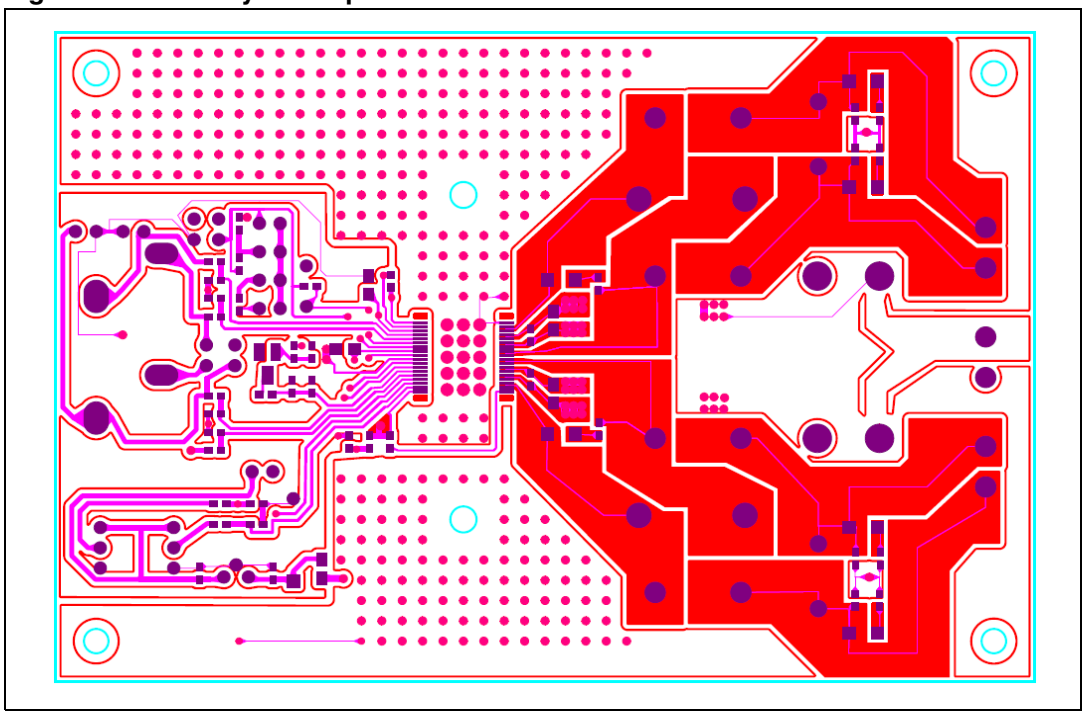


Figure 5. PCB layout - bottom side

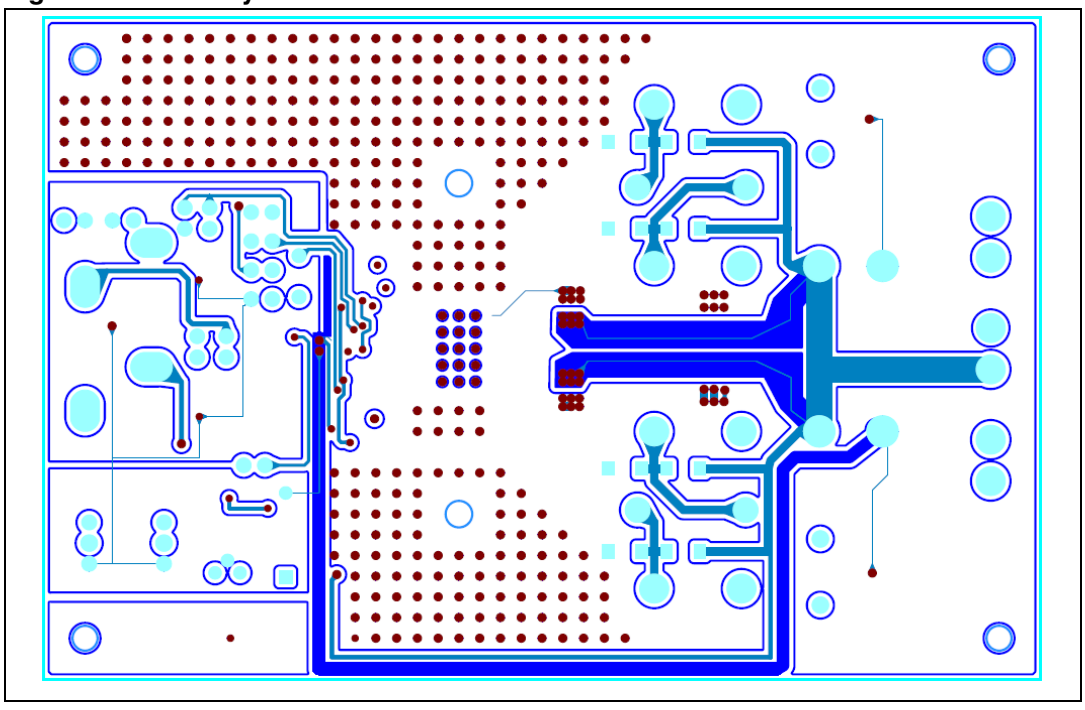
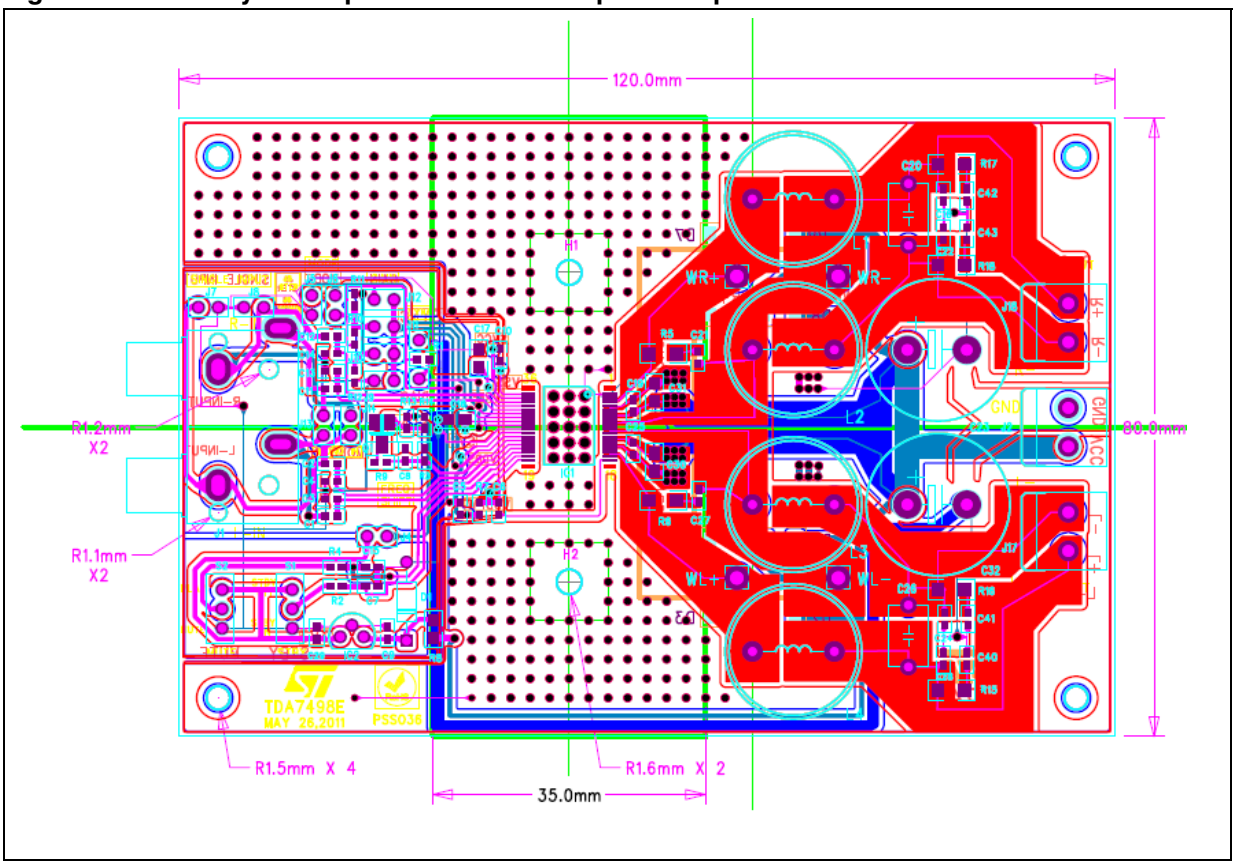


**Figure 6. PCB layout - top and bottom sides plus components**



# 4 Electrical characteristics

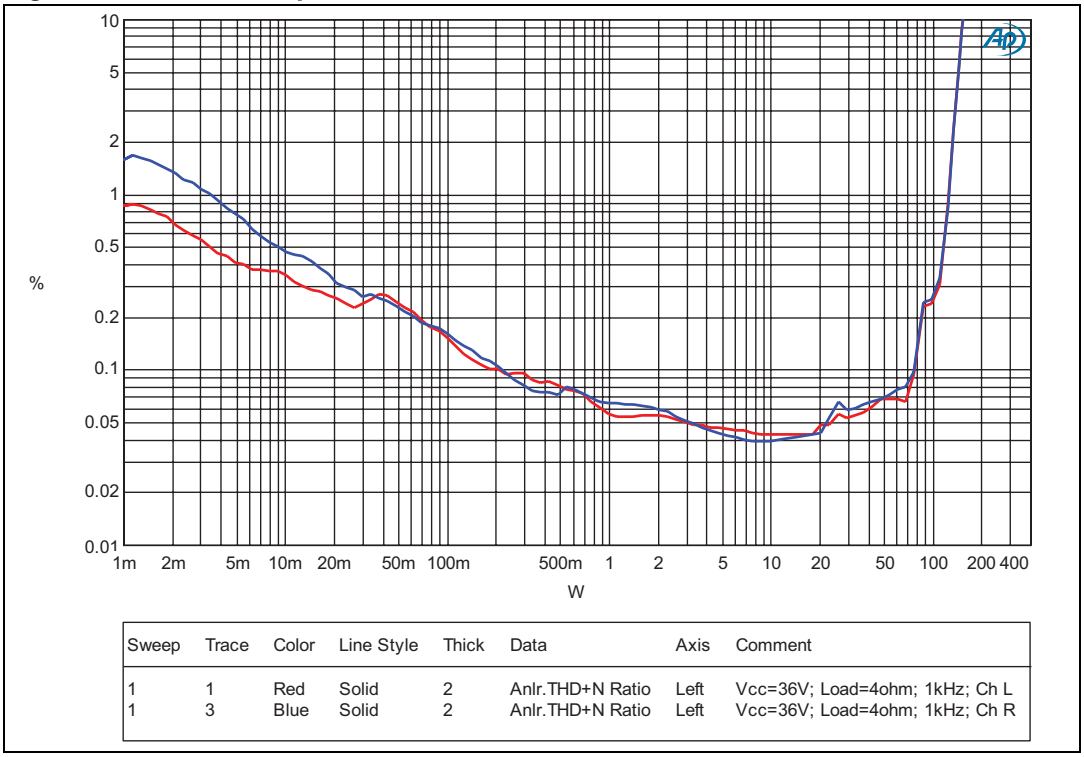
Referring to *Figure 3: TDA7498E schematic*, the Left (L) and Right (R) channels are the output for a stereo configuration. $V_{CC}$ = +36 V, Gain 23.6 dB; Tamb = 25.5 °C; InputFreq = 1 kHz; RefLevel = 1 W (0 dBr), Load = 4 Ω (resistive dummy load).

**Table 1. Electrical characteristics**

| | | |
|---|---|---|
| THD+N vs. power | Pout = 1 W | 0.0555% |
| $I_{OCP}$ | | 12 A |
| SNR | No filter | -74.3 dB |
| | AW - filter | -77.5 dB |
| DNR | No filter | -94 dB |
| | AW - filter | -98 dB |
| Xtalk | 1 kHz | -85.9 dB |

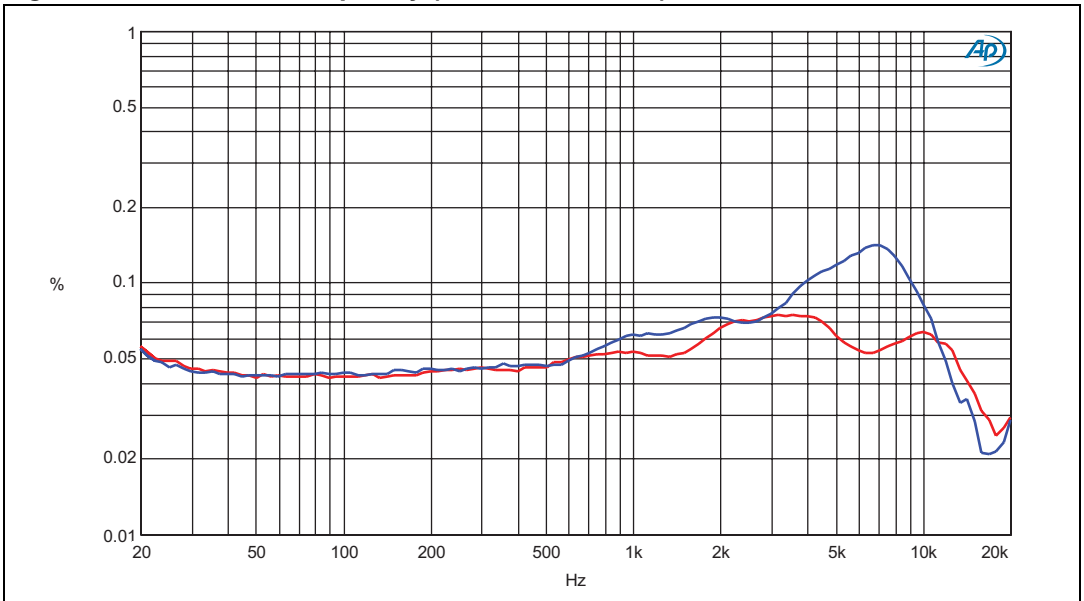
# 5 Test curves

**Figure 7. THD+N vs. power**



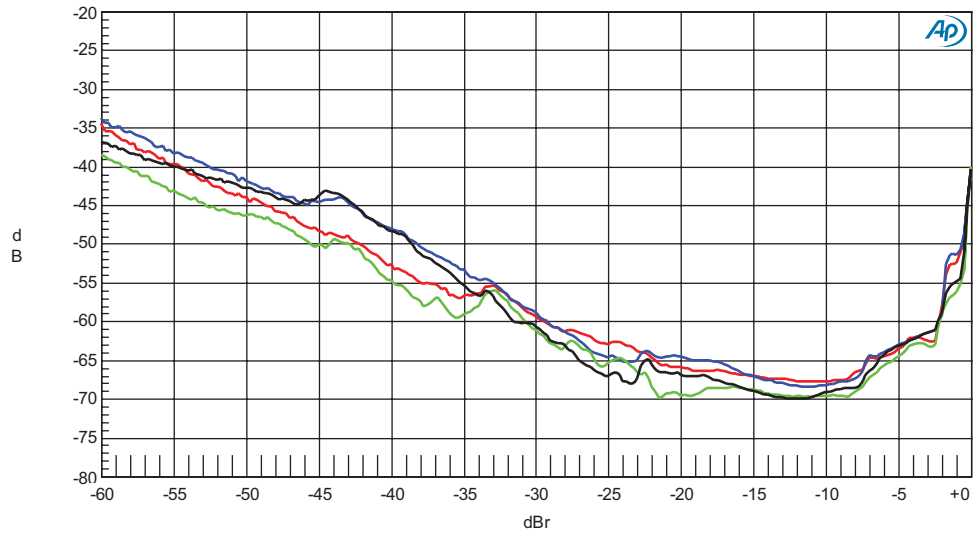

| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Red | Solid | 2 | Anlr.THD+N Ratio | Left | Vcc=36V; Load=4ohm; 1kHz; Ch L |
| 1 | 3 | Blue | Solid | 2 | Anlr.THD+N Ratio | Left | Vcc=36V; Load=4ohm; 1kHz; Ch R |

**Figure 8. THD+N vs. frequency (ref = 1 W at 1 kHz)**



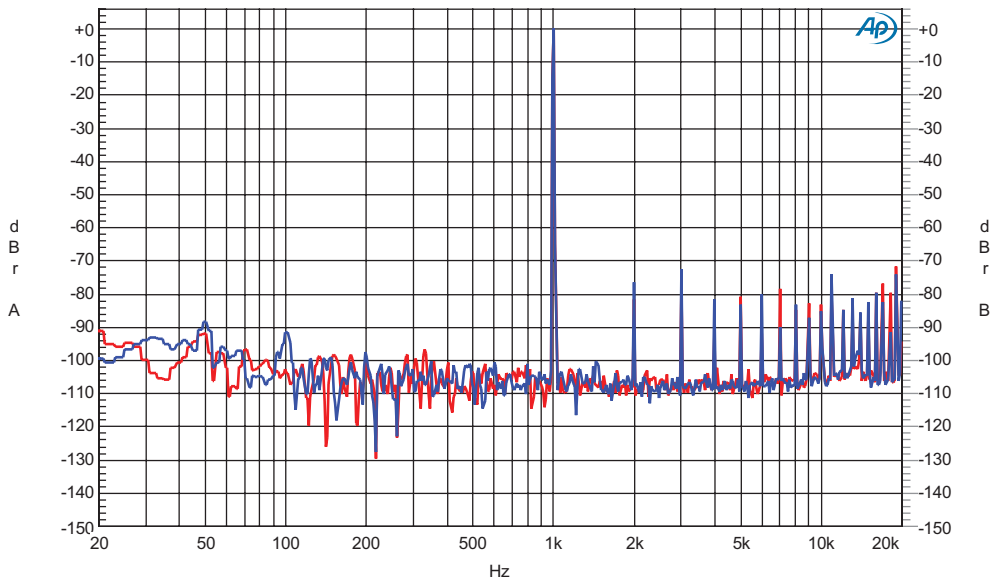

| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Red | Solid | 2 | Anlr.THD+N Ratio | Left | Vcc=36V; 1W@1kHz; Ch L |
| 1 | 2 | Blue | Solid | 2 | Anlr.THD+N Ratio | Left | Vcc=36V; 1W@1kHz; Ch R |

**Figure 9. DNR**



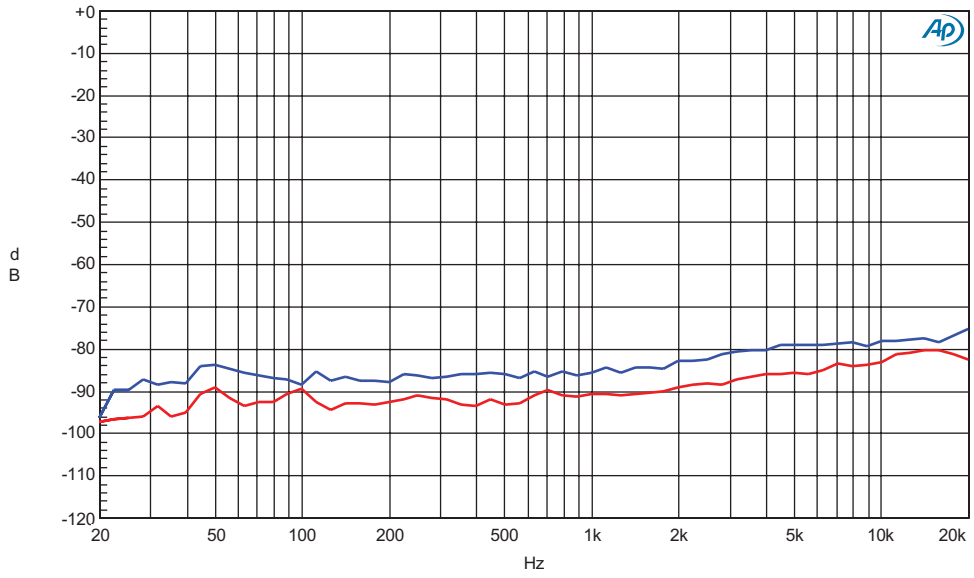

| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Red | Solid | 2 | Anlr.THD+N Ratio | Left | Vcc=36V_1kHz_4 ohm; Ch L |
| 1 | 2 | Blue | Solid | 2 | Anlr.THD+N Ratio | Left | Vcc=36V_1kHz_4 ohm; Ch R |
| 2 | 1 | Green | Solid | 2 | Anlr.THD+N Ratio | Left | Vcc=36V_1kHz_4 ohm; Ch R - AW Filter |
| 2 | 2 | Black | Solid | 2 | Anlr.THD+N Ratio | Left | Vcc=36V_1kHz_4 ohm; Ch L - AW Filter |

**Figure 10. FFT (0 dBr at 1 W)**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Red | Solid | 2 | Fft.Ch.1 Ampl | Left | Vcc=36V; Ref: 1W@1kHz: Ch L |
| 1 | 2 | Blue | Solid | 2 | Fft.Ch.2 Ampl | Right | Vcc=36V; Ref: 1W@1kHz: Ch R |

**Figure 11. Crosstalk**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Red | Solid | 2 | S2C.Anlr.Crosstalk | Left | Vcc=36V; 1W; 4ohm; (Ch L on) |
| 1 | 2 | Blue | Solid | 2 | S2C.Anlr.Crosstalk | Left | Vcc=36V; 1W; 4ohm; (Ch R on) |

**Figure 12. Linearity**

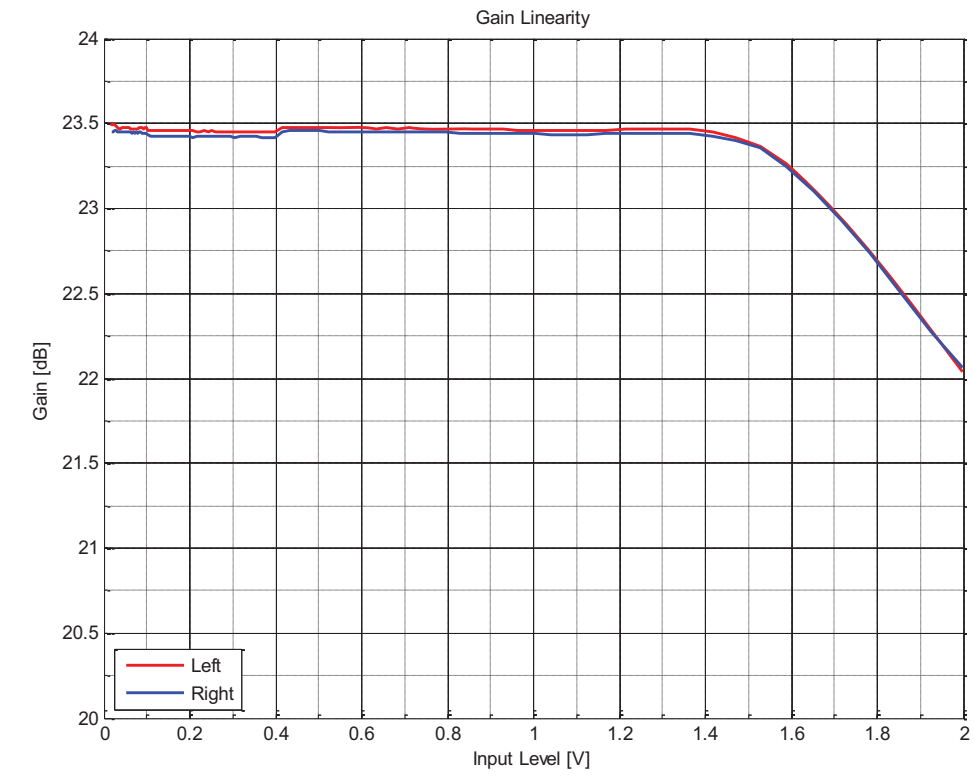
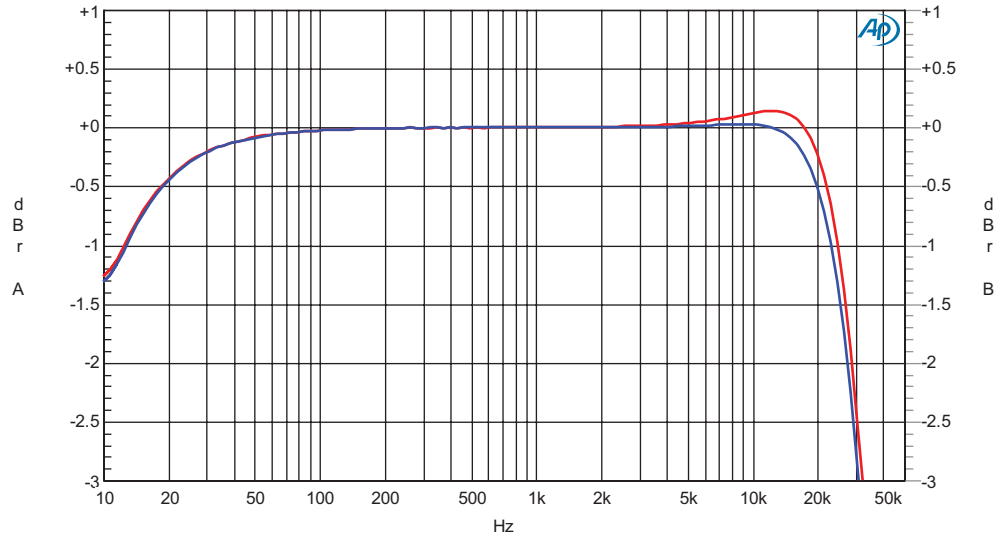
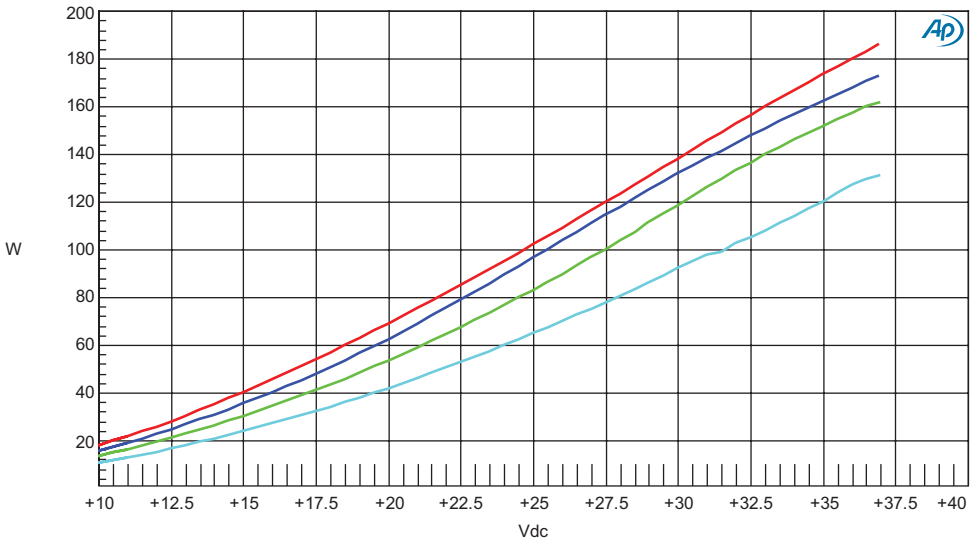


**Figure 13. Bandwidth**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Red | Solid | 2 | Anlr.Level A | Left | Vcc=36V; 1W; Ch L |
| 1 | 2 | Blue | Solid | 2 | Anlr.Level B | Right | Vcc=36V; 1W; Ch R |

**Figure 14. Pout vs. $V_{CC}$ and THD level**




| Sweep | Trace | Color | Line Style | Thick | Data | Axis | Comment |
|---|---|---|---|---|---|---|---|
| 1 | 1 | Cyan | Solid | 2 | Anlr.Level A | Left | Pout vs. Vcc; Load=4ohm; THD=1% |
| 2 | 1 | Green | Solid | 2 | Anlr.Level A | Left | Pout vs. Vcc; Load=4ohm; THD=10% |
| 3 | 1 | Blue | Solid | 2 | Anlr.Level A | Left | Pout vs. Vcc; Load=4ohm; THD=20% |
| 4 | 1 | Red | Solid | 2 | Anlr.Level A | Left | Pout vs. Vcc; Load=4ohm; THD=30% |

# 6 Design guidelines for PCB schematic and layout

## 6.1 Schematic

### 6.1.1 Main driver for the selection of components

- Absolute maximum rate (input $V_{CC}$ supply): 40 V
- Bypass capacitor 100 nF in parallel to 1µF for each power $V_{CC}$ branch. Dielectric X7R is suggested.
- Coil saturation current must be compatible with the peak current of application

### 6.1.2 Decoupling capacitors

There are two different ways to use the decoupling capacitors:

- The decoupling capacitor(s) can be shared among channels; the layout must be designed to implement a "star route" for the $V_{CC}$ paths.
- One decoupling capacitor can be used for each channel. It is mandatory that each decoupling capacitor be placed as close as possible to the IC pins. This solution is implemented on the TDA7498E demonstration board.

### 6.1.3 Output filter

- Snubber network: the key function of a snubber network is to absorb energy from the inductive component in the power circuit (the output coils and the speaker). The purpose of the snubber RC network is to dissipate the unnecessary high pulse energy, such as a high voltage spike, in the power circuit which is dangerous to the system.
- Main filter (low-pass filter): The purpose of the main filter is to remove the carrier frequency (≈310 kHz) and to cut off the frequency higher than the audible range of 20 kHz. The LPF filter is implemented by a passive Butterworth topology. In order to have a clean and flat frequency response, it is mandatory to design the filter to fix the cutoff frequency a little bit above 20 kHz.
- Damping network: The purpose of the damping network is to avoid the high-frequency oscillation issue on the output circuit. When the load is disconnected from the amplifier, the frequency response of the main filter is not flat and there is the possibility of adding gain in a frequency band. The damping network also improves the THD performance. The damping network can also avoid the inductive effect of the PCB tracks when the system is working at high frequency with PWM.

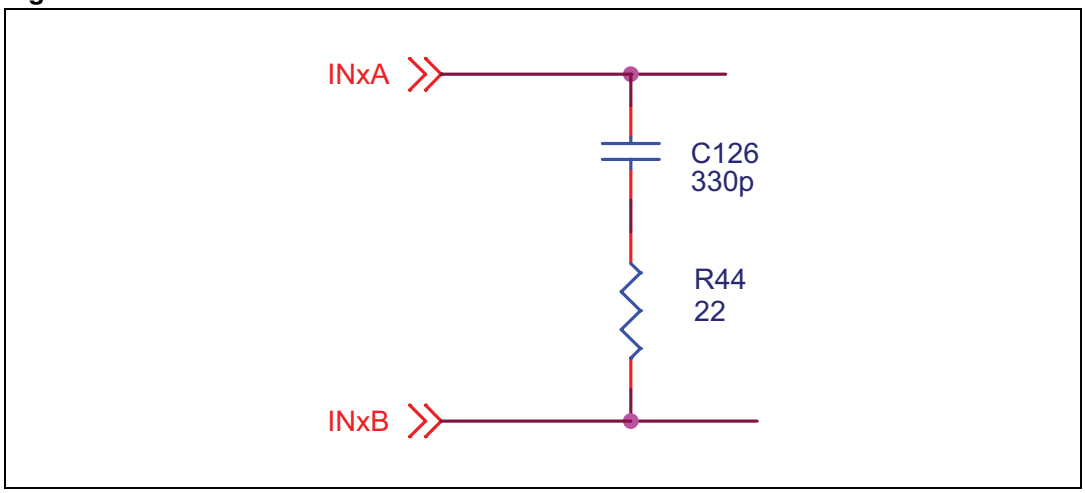
### Snubber filter

The snubber circuit must be optimized for the specific application. Starting values are 330 pF in series to 22 ohm. The power dissipation of this network (resistor) depends on the power supply, frequency and capacitor values using following formula:

$$P = C \cdot f \cdot (2 \cdot V)^2$$

This power is dissipated on the series resistance.

**Figure 15. Snubber filter - solution 1**

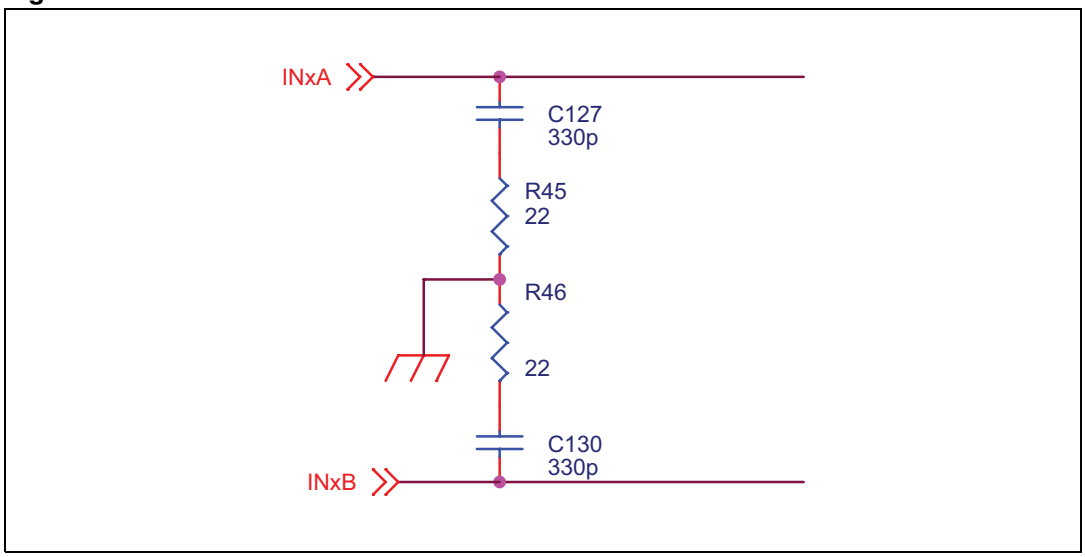



To increase the efficiency, it is possible to use two equal snubber networks toward GND. In this case, the formula to evaluate power is:

$$P = C \cdot f \cdot 2 \cdot V^2$$

This power is dissipated on the resistance.

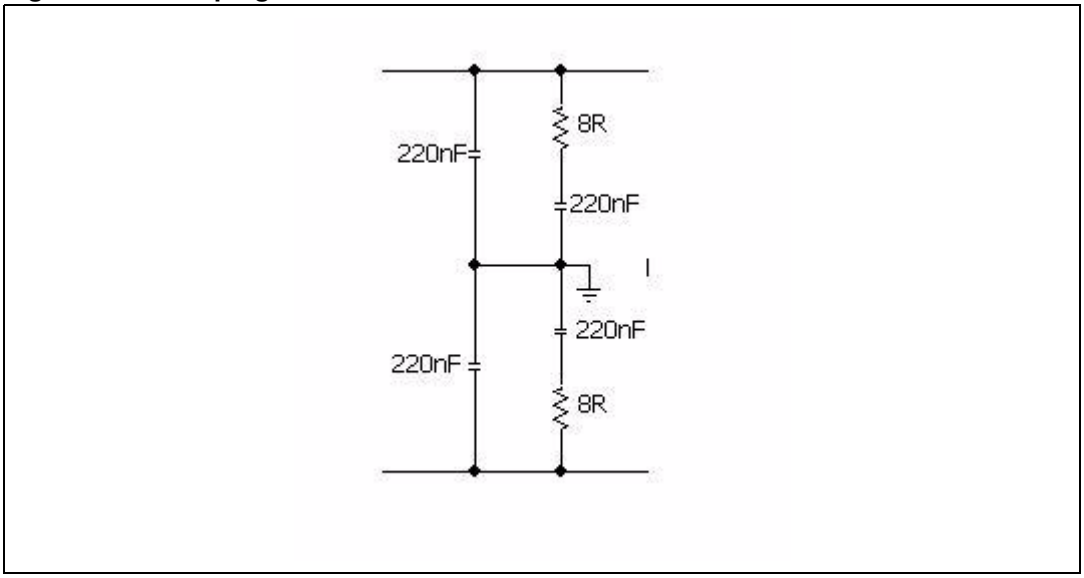
**Figure 16. Snubber filter - solution 2**



### Dumping network

The C-R-C is a dumping network. It is mainly intended for high inductive loads and for common-mode noise attenuation.

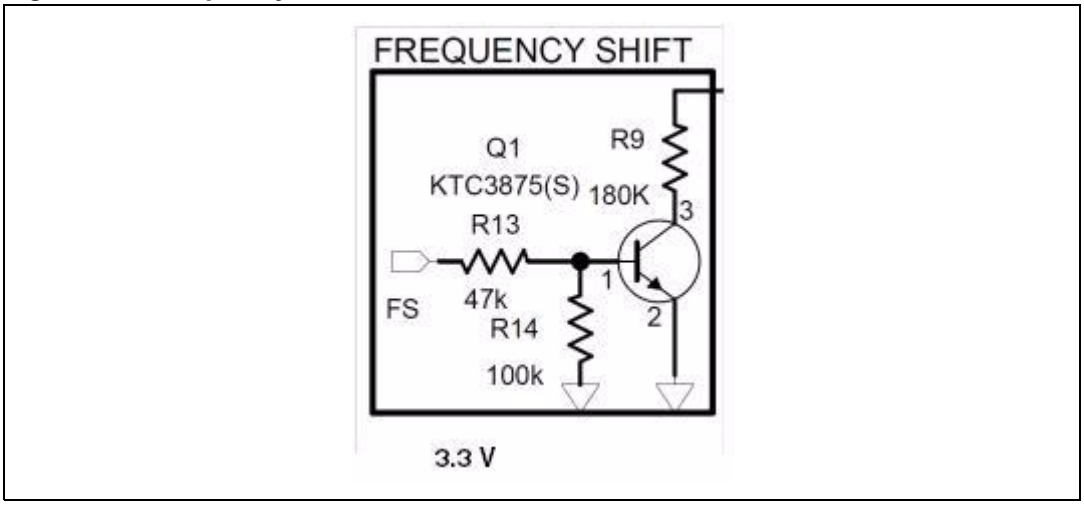
**Figure 17. Dumping network**




### PWM output frequency shifting for AM band radio sensitivity improvement

Using a logic control signal (FS) from MCU or from a DSP (3.3 V) it is possible to modify the PWM output frequency.[b]

**Figure 18. Frequency shift**

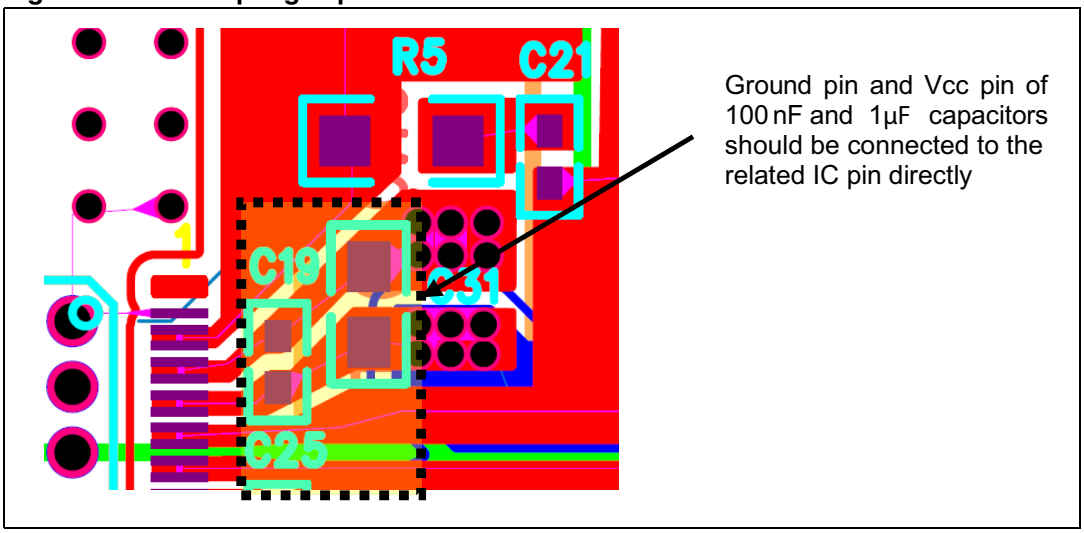



b. For the PWM frequency calculation formula please refer to the datasheet.

## 6.2 Layout

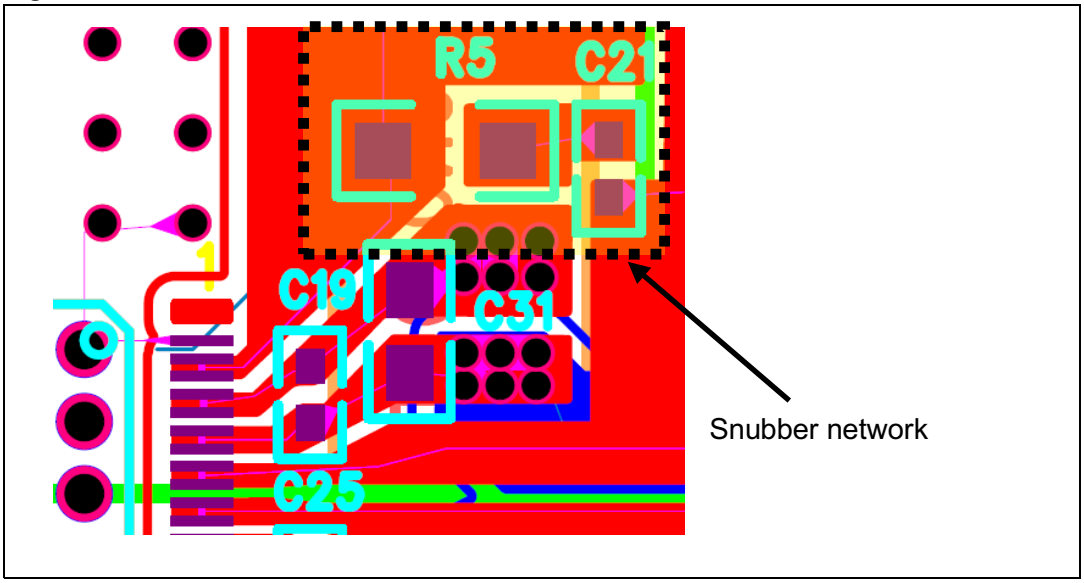
- Solder 100 nF and 1µF bypass ceramic capacitors as close as possible to the related IC pin
- To avoid the effect due to the parasitic inductive coil generated by the copper wires, it is suggested to use the ceramic capacitor to balance the reactance. It's mandatory to place the ceramic capacitor as close as possible to the related pins. The distance between the capacitor to the related pins is recommended to be within 5 mm.

**Figure 19. Decoupling capacitors**



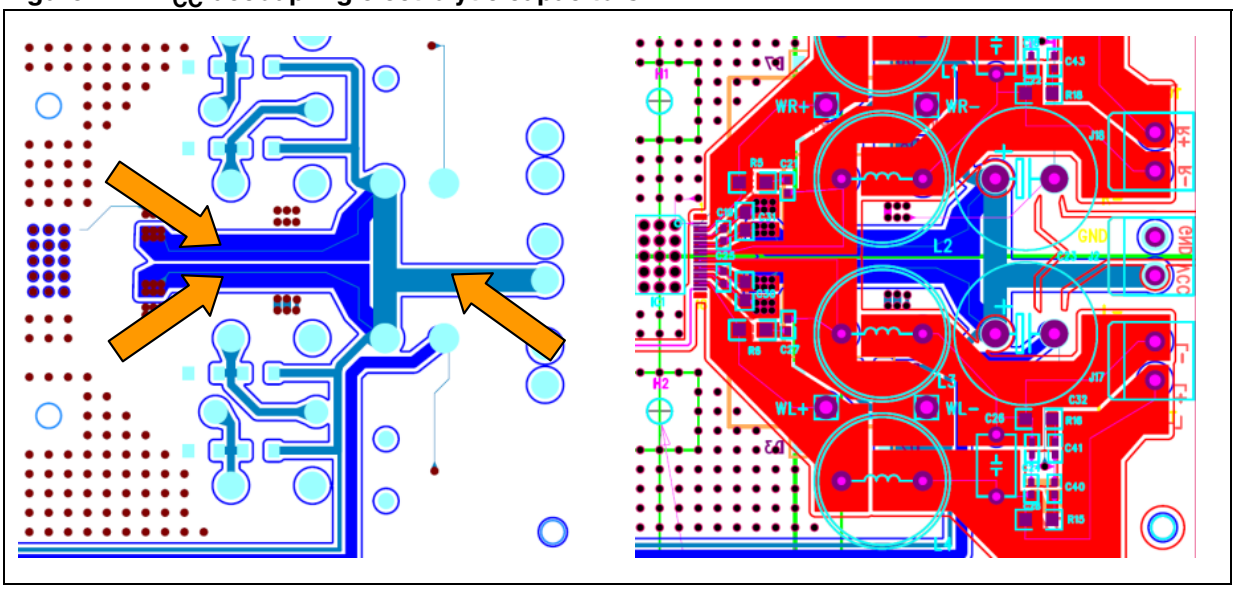

- Solder the snubber networks as close as possible to the related IC pin. A high level spike may occur if the snubber network is placed too far from the pins. It's recommended that the distance from the snubber network be within 3 mm which takes into consideration the width of the copper wire.

**Figure 20. Snubber network**



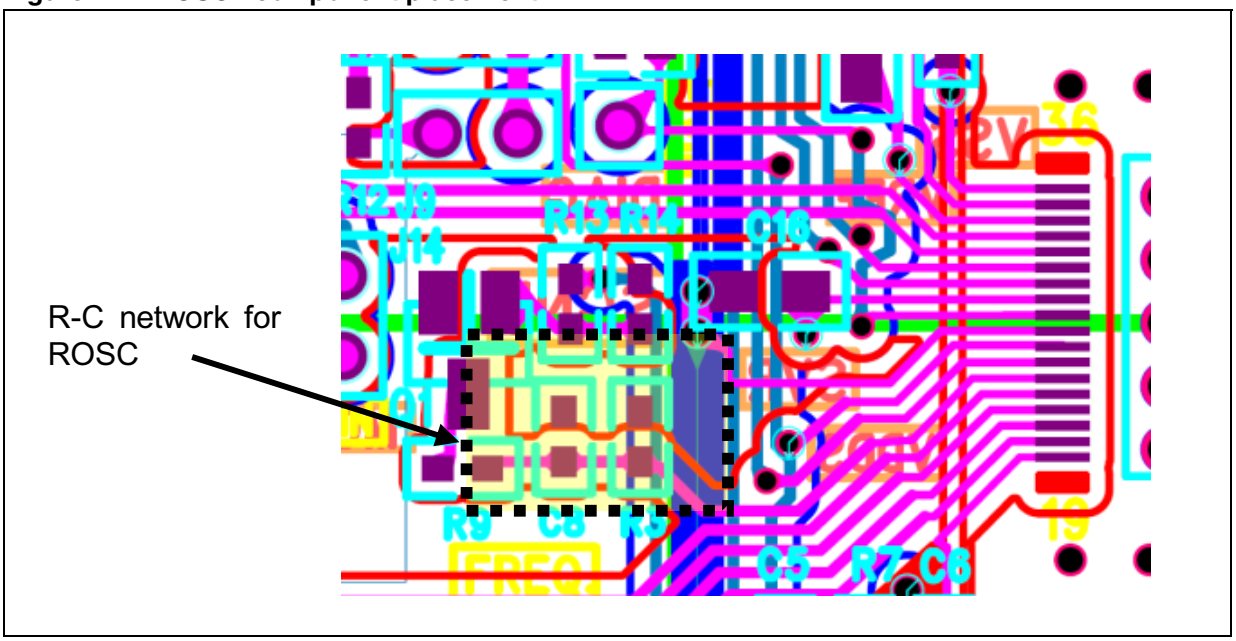
- Use electrolytic capacitors first to separate the $V_{CC}$ branches. A "star route" for the $V_{CC}$ supply is suggested to avoid interference between the channels such as when one channel is idle while the other channel is working with a full load. In applications with high output power, another approach is to filter the two channels separately. This solution is implemented in this demonstration board.

**Figure 21. $V_{CC}$ decoupling electrolytic capacitors**



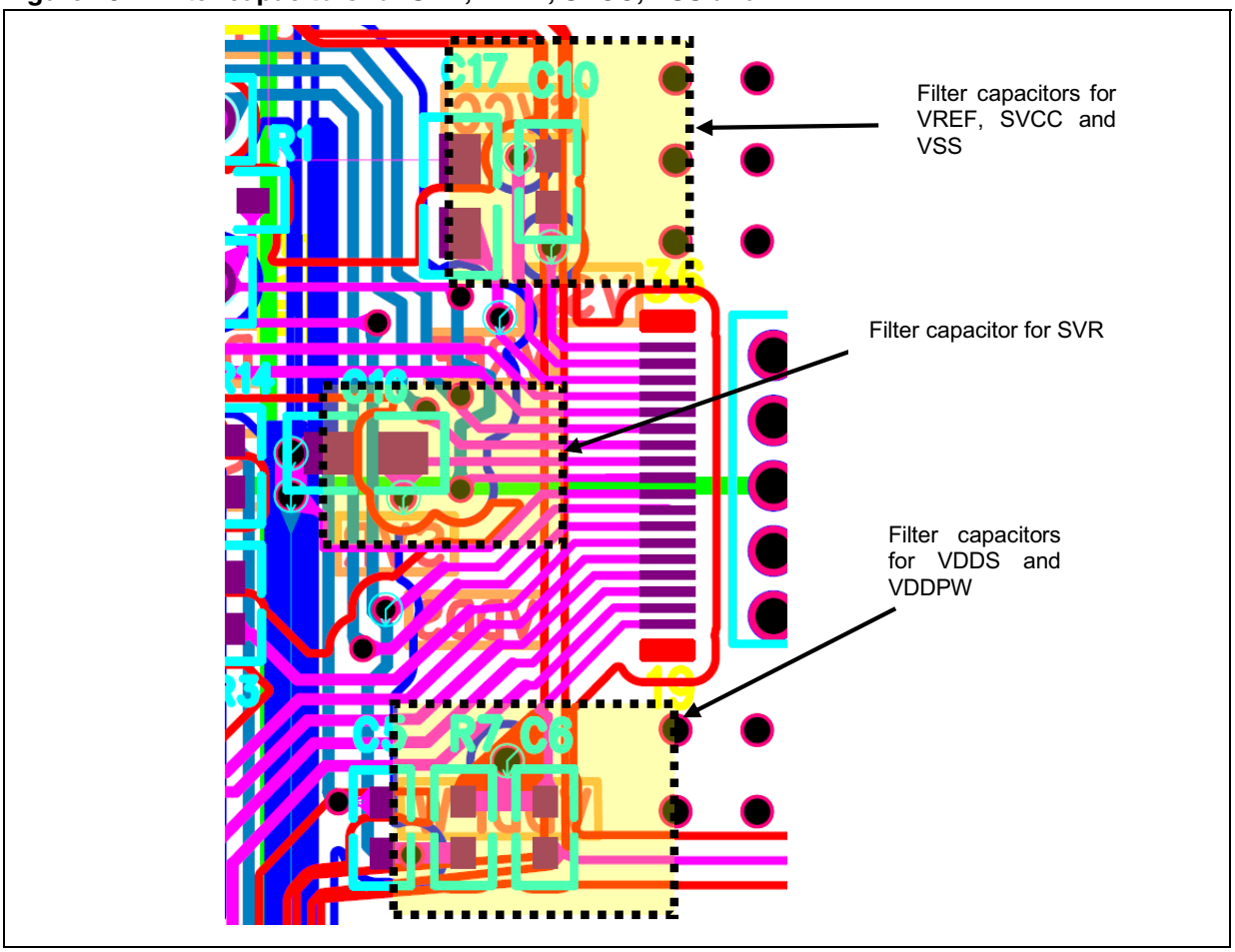

- ROSC network: Place the RC filter for the ROSC pin close to the IC

**Figure 22. ROSC - component placement**



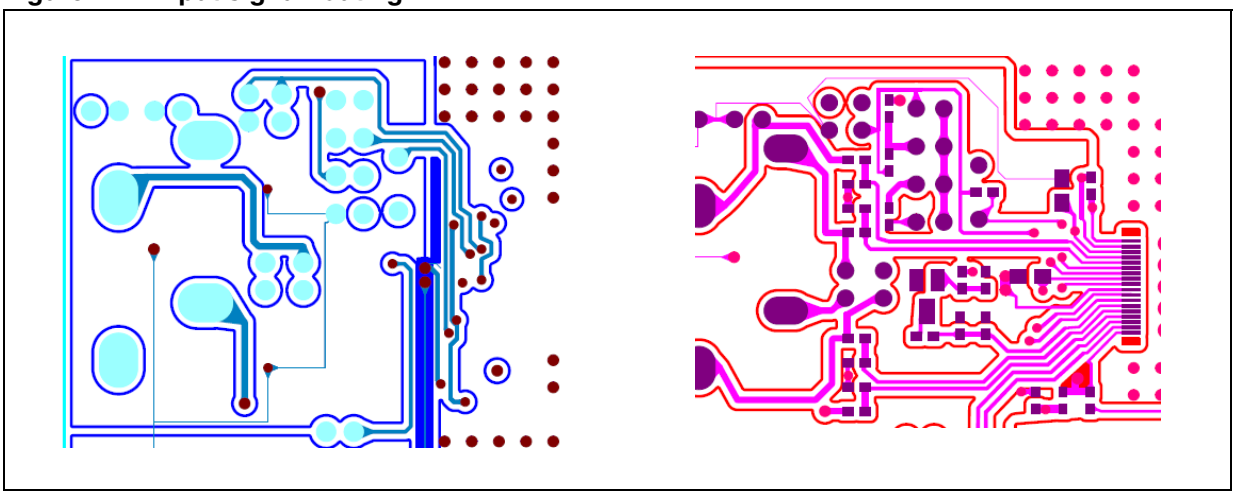
- Place the filter capacitors for SVR, VREF, SVCC, VSS and VDDPW close to the IC.

**Figure 23. Filter capacitors for SVR, VREF, SVCC, VSS and VDDPW**



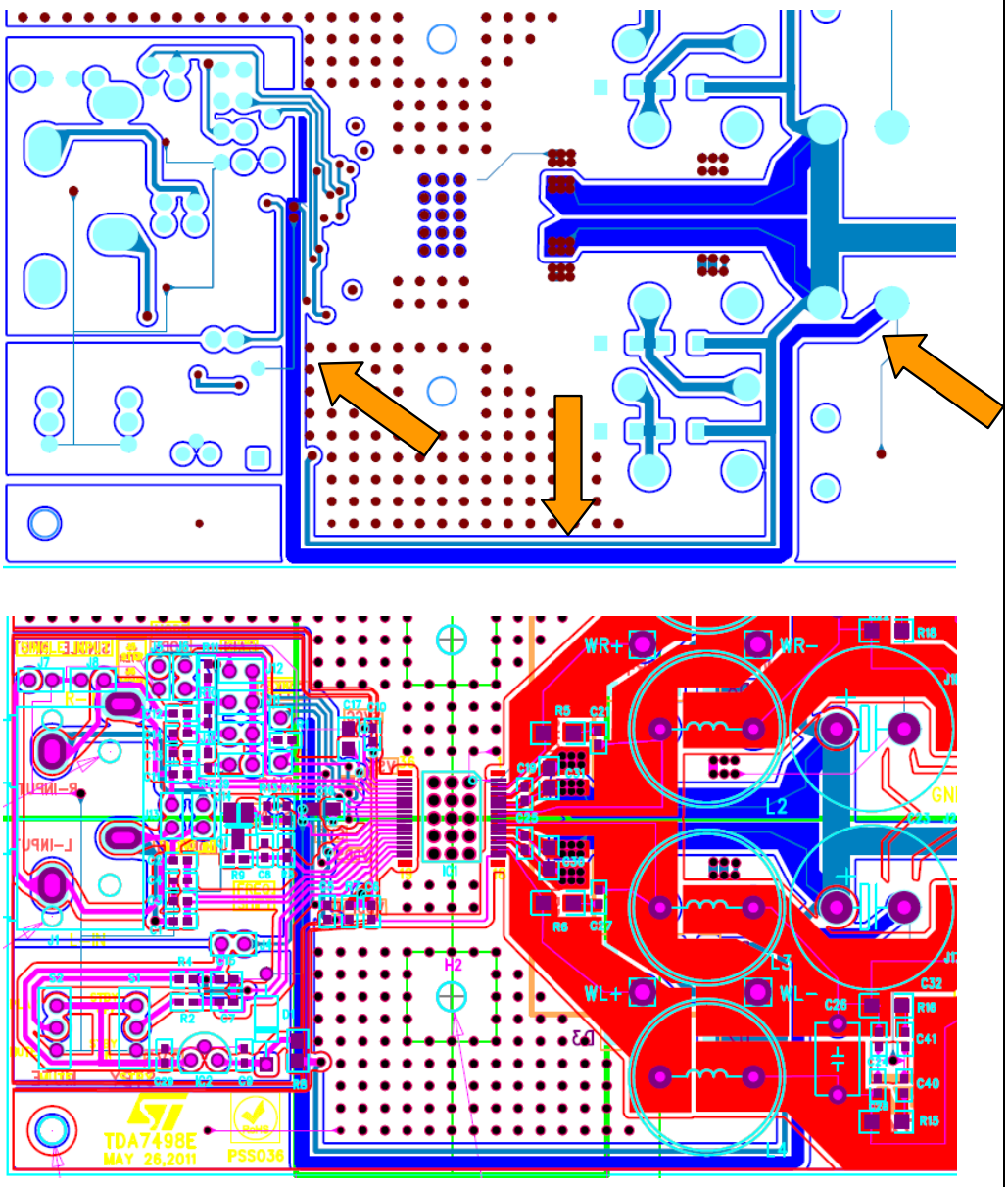

- Input signal routing

**Figure 24. Input signal routing**



- Signal ground and power ground routing: the signal ground should be connected to the bulk capacitor negative terminal via a dedicated copper track; no vias must be present in the connection path.

**Figure 25. Signal ground and power ground routing**



# 7 Revision history

Table 2. Document revision history

| Date | Revision | Changes |
|---|---|---|
| 09-Jan-2012 | 1 | Initial release. |