AN886
APPLICATION NOTE

SELECTING BETWEEN ROM, FASTROM AND OTP FOR A MICROCONTROLLER

by Microcontroller Division Applications

INTRODUCTION

A customer who develops an MCU-based application needs various levels of flexibility in order to perform code modifications at different times in the life cycle of the product (these levels are explained on the next page). To satisfy these requirements, STMicroelectronics supports several device types within two main groups of microcontroller product families:

– EPROM, OTP, FASTROM and ROM microcontroller families

– Flash, FASTROM and ROM microcontroller families

This Application Note discusses the first group of families. For information on the second group, refer to Application Note AN1068.

Rev. 1.0

DEFINITION OF TERMS

Windowed EPROM (Erasable Programmable Read Only Memory): this type of MCU device can be programmed then erased using UV light. EPROM MCU devices are sold in ceramic packaging with a quartz window. They are reprogrammable outside systems.

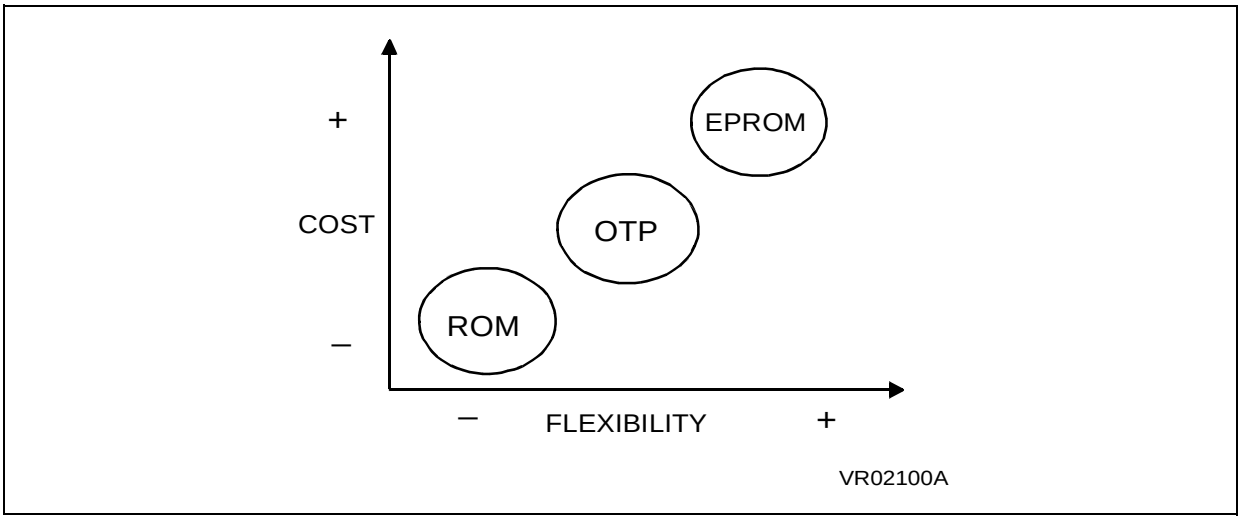
OTP (One Time Programmable EPROM): OTP is a type of **EPROM** sold in plastic packaging. Unlike UV EPROMs that have a quartz window in the package above the chip to allow erasure by UV light, OTP Memory **cannot be erased** once it has been programmed. OTPs are typically programmed by the customer.

FASTROM (Factory Advanced Service Technique Read Only Memory): this type of MCU is a OTP device pre-programmed by STMicroelectronics with the customer's code and selected options. The advantage of FASTROM, compared to OTP, is improved programming efficiency for large quantities (10,000+) and compared to ROM, it has the advantage of a shorter lead-time.

ROM (Read Only Memory): ROM devices are programmed at the fabrication step using a special mask containing the customer code. Therefore, the code can't be modified after that step.

Costs are highly depending on the **flexibility** given to the device (ability to be easily erased or programmed). ROM is the cheapest technology but provides little flexibility whereas OTP and EPROM are more flexible but their manufacturing cost is higher. The high cost of EPROM MCU devices is due to the price of ceramic packages.

Figure 1. Cost versus Flexibility for different MCU types



1 TYPICAL APPLICATION DEVELOPMENT FLOW

	Design Phase	Validation Phase	Pre-production Phase	Production Phase	
ST Solution	EPROM	OTP	OTP	OTP	ROM
Code Updates	••••	•••	••	•	None
Number of Units	•	••	•••	••••	•••••

When a new application is developed, different device versions will be used at each step of the development, depending on the required **programming flexibility**.

During the **design phase**, a high flexibility is required and only a small number of parts are necessary, therefore the use of UV erasable EPROM is recommended. Then, fewer code corrections (and a significant number of parts) are needed during **validation phase**: at this point OTP is the best solution.

The next step is **pre-production phase**: only a few code updates are needed at a reasonable device cost. Again, the best choice is to use OTP memory. Finally, when the **mass production phase** begins, there is no more need for corrections since the product has been fully optimized, so ROM is the most adapted if very high volumes are needed. Otherwise (low to medium volumes) the most effective solution is to continue using STMicroelectronics' competitively priced OTP.

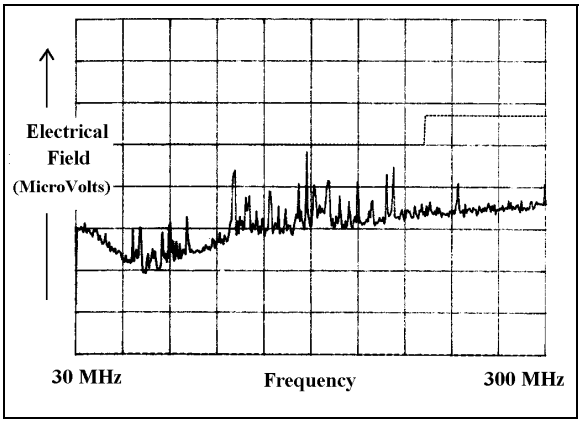
The following table summarizes the main benefits and drawbacks of using ROM, OTP or windowed EPROM MCU devices.

	ROM	OTP	EPROM
+	**Cheaper than OTP** (simpler process and testing) **Lower failure rate** **(**less handling, no programming)	**Lower cost** compared to windowed EPROM (use of cheaper plastic packages) Ability to be programmed **directly** by the **final user**	**High flexibility** (Programming, Code check and Erasure cycle in less than 60 minutes)
-	**Limited flexibility** (customer code implemented at masking stage) Higher inventory risks	Higher failure rate compared to ROM due to customer handling and programming	Expensive ceramic packages

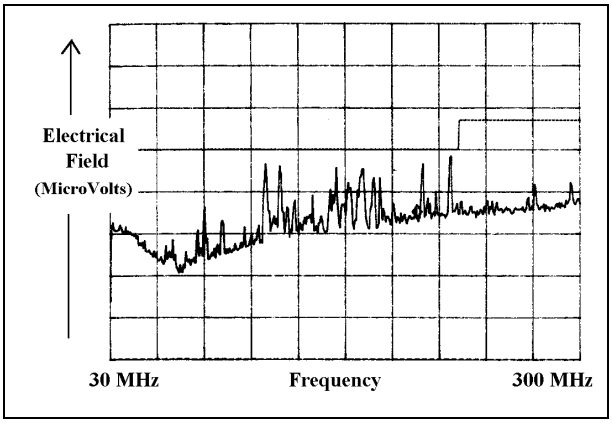
2 COMPARISON OF PRODUCTION FLOWS FOR ROM AND OTP

ROM and OTP devices have exactly the same functional and electrical behaviour in an application because STMicroelectronics designs the two products with the same methodology. ROM and OTP devices are qualified using the same procedures. They are tested using the **same test flows** (see further) and with the **same parameter limits**. A good indication of device similarity is EMC (electromagnetic noise immunity) measurements performed on both versions (ROM and OTP) for the same MCU device.

ST6220 (ROM version)



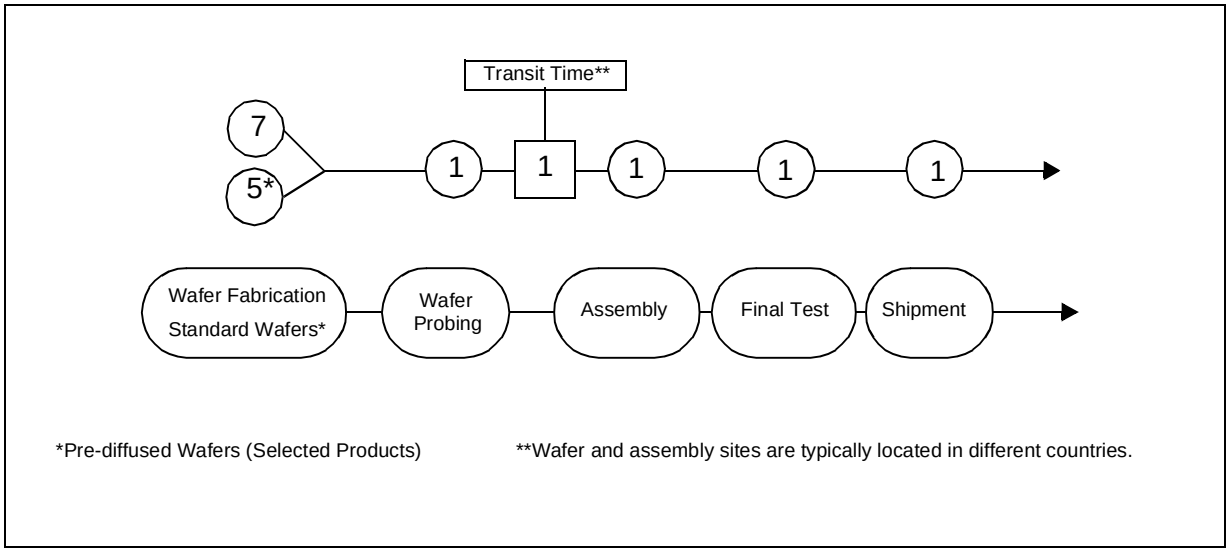
ST62T20 (OTP version)



3 TYPICAL MANUFACTURING LEAD TIME FOR ROM AND OTP

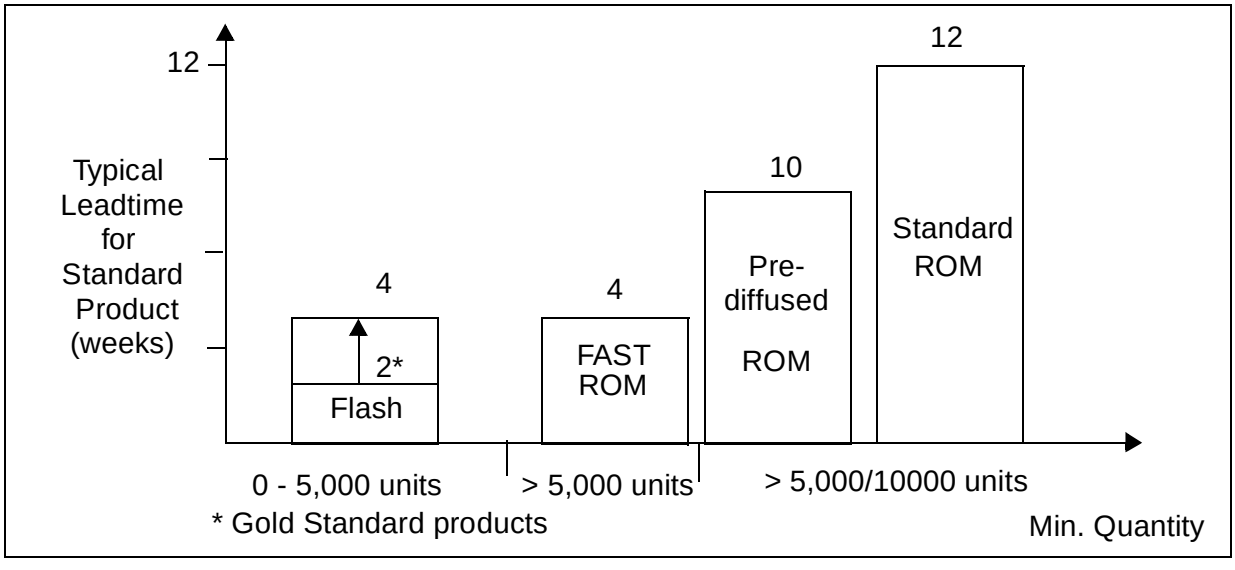
The complexity of all the operations needed to manufacture a component implies a certain time period. Understanding STMicroelectronics' MCU manufacturing cycle is important in order to establish good relationships with customers. The numbers given here are typical and subject to change in the future

Figure 2. Typical Fabrication Leadtime in weeks.



In order to limit lead time on ROM products, STMicroelectronics has introduced pre-diffusion technology on selected products. This allows a two weeks reduction in total cycle time. Also notice that MCU devices have to be ordered in specified minimum quantities for ROM version.

Figure 3. Typical Leadtime for Standard Products



4 MINIMUM ORDER QUANTITIES FOR ROM AND FASTROM

The following minimum order quantities apply to ROM and FASTROM microcontroller devices:.

	ROM			FASTROM
	Minimum quantity per year	**Minimum order quantity**	**Minimum quantity per line item**	**Minimum quantity per year and per line item**
ST6 Family	100000	50000	10000	5000
ST7 and ST9 Families	50000	25000	5000	5000

5 OTP RELIABILITY

Why do ROM devices have very low failure rates?

For ROM parts, the customer program is included at a **specific mask level** of the wafer fabrication. Therefore, the complete product functionality is present in both the die and the assembled product. This functionality can be fully evaluated at both **wafer probing** and **final electrical test**, thus ensuring a **low reject rate** at customer manufacturing stage.

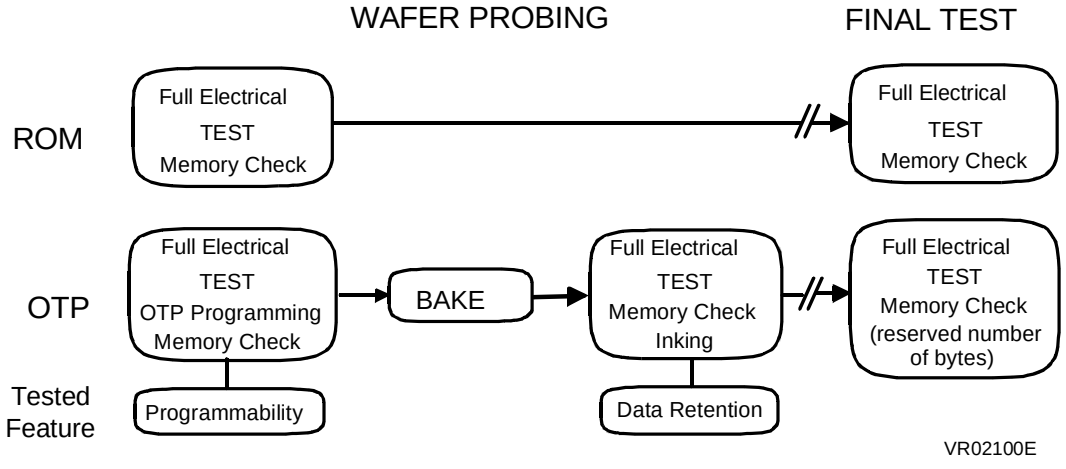
Testing Programmability and Data Retention for OTP devices

To ensure optimal OTP quality, STMicroelectronics tests two important device characteristics: **programmability** and **data retention**. The program memory of an OTP should be seen as a number of cells that will be activated during programming. These cells can be “deactivated” by lighting the die with UV light. This recovery is **no longer possible** once the OTP die has been **encapsulated** in an opaque plastic package. Therefore **programmability** and **data retention** can only be fully tested at **wafer probing**.

At this step the dice are electrically tested and the memory is programmed to verify **programmability**. Then the wafers are placed in high temperature **bake** to accelerate any possible memory retention defects. The dice are then tested again to check **data retention**. After this test, UV light is used to deactivate the cells and the good dice are assembled.

Description of OTP programmability test

Figure 4. Details about the electrical tests performed on OTP and ROM



Although the programmability of the OTP die is verified as fully functional at probe test, the assembly process can **affect this parameter** in the finished product (for example by damaging some cells). It is therefore necessary to make a **final test** to check **programmability**. But since UV light cannot be used to restore OTP's programmed bytes once the die has been en-

capsulated, it is not possible to test 100% of the user program area. For this reason the final test is **limited to a reserved number of bytes** which are programmed and then verified.

OTP rejects rates due to programmability failures

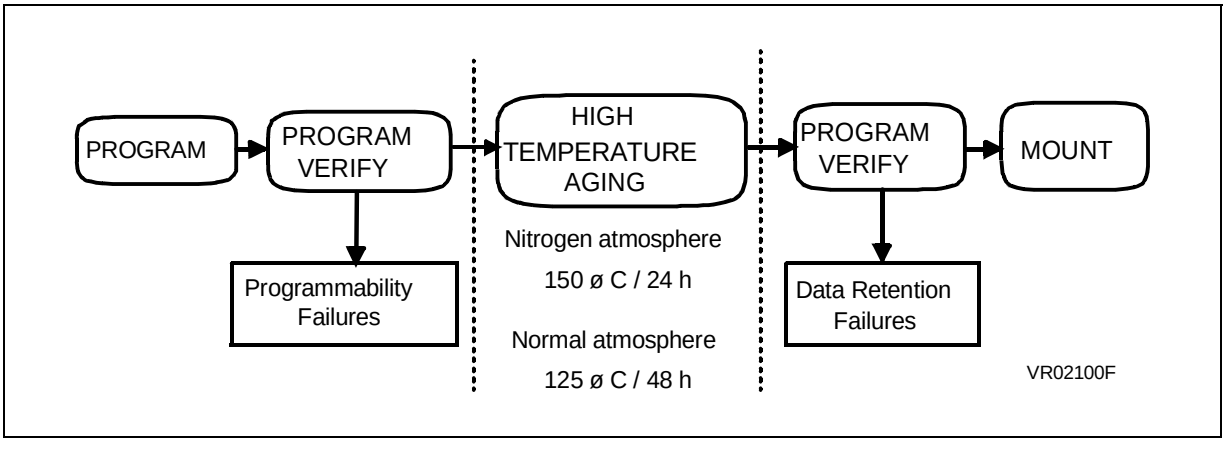
As the programmability of the OTP cannot be fully tested once the die has been encapsulated, a customer is likely to find a **programming reject rate below 1%** when programming is performed using **qualified programming tools**. This rate **should be considered as normal for OTPs and should not generate** customer quality returns. If higher failure rates are observed, it is recommended to check the programming equipment.

Recommended screening conditions for OTP (data retention failures)

Programmability failures can be fully screened because gang programmers check the content of OTP devices after programming. But gang programmers cannot perform **data retention** tests.

High temperature aging is recommended for screening microcontrollers that use OTP devices and performing data retention tests. The well-known retention failure mechanism corresponds to charge losses during the component life time. The customer is likely to find a **data retention failure rate below 0.5%** when programming is performed using **qualified programming tools.** Therefore, it is strongly recommended to screen these potential failures as described hereafter:

Figure 5. Recommended Screening Conditions for OTP



Screening devices that are subject to data retention failures will allow customers to obtain OTP devices with a similar quality level compared to ROM devices.

In order to further lower the reject levels for programmability and data retention, STMicroelectronics is continuously pursuing technology improvements in areas as soft die mounting, low stress mold compounds and passivation layer enhancements.