PYRAMID SEMICONDUCTOR CORPORATION

# P4C1041L

## LOW POWER 256K X 16 (4 MEG) STATIC CMOS RAM

## FEATURES

- **Fast Access Time - 55 ns**
- **Low Power Operation**
- **Single 5V±10% Power Supply**
- **2.0V Data Retention**
- **Easy Memory Expansion Using $\overline{CE}$ and $\overline{OE}$ Inputs**
- **Fully TTL Compatible Inputs and Outputs**
- **Advanced CMOS Technology**
- **Fast $t_{OE}$**
- **Automatic Power Down when deselected**
- **Packages**
  - **– 44-Pin 400 mil TSOP II**

## DESCRIPTION

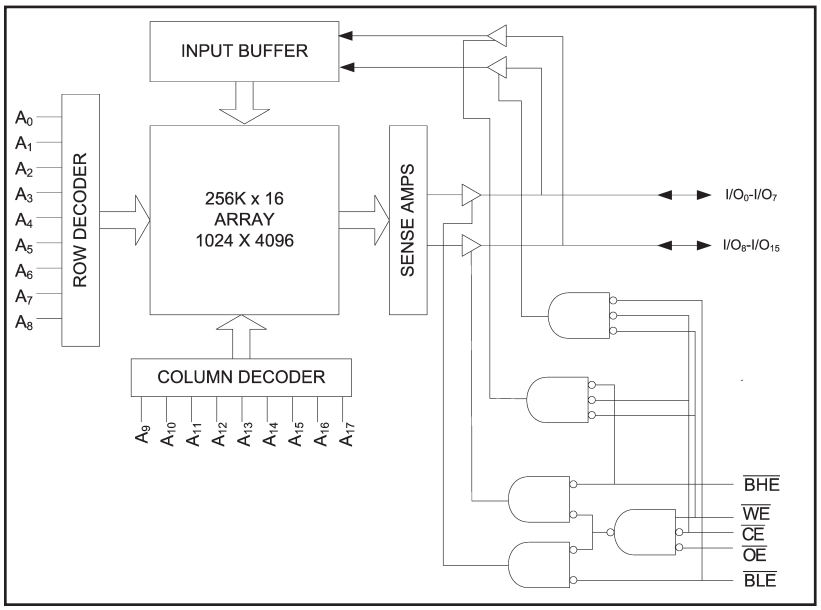
The P4C1041L is a 262,144 words by 16 bits high-speed CMOS static RAM. The CMOS memory requires no clocks or refreshing, and has equal access and cycle times. Inputs are fully TTL-compatible. The RAM operates from a single 5.0V ± 10% tolerance power supply.

Access times of 55 nanoseconds permit greatly enhanced system operating speeds. CMOS is utilized to reduce power consumption to a low level.

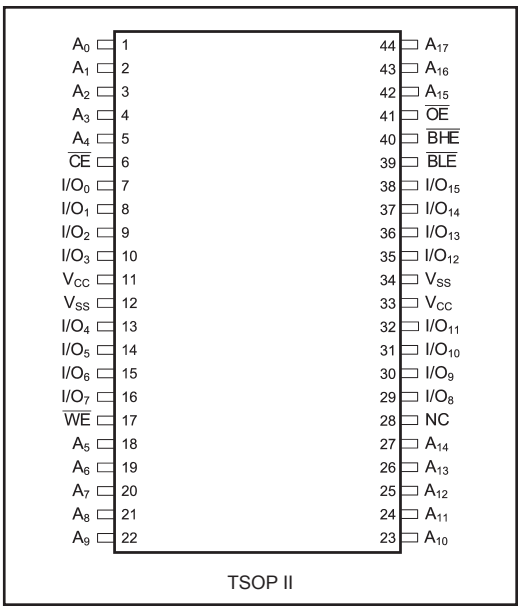
The P4C1041L device provides asynchronous operation with matching access and cycle times. Memory locations are specified on address pins $A_0$ to $A_{17}$. Reading is accomplished by device selection ($\overline{CE}$) and output enabling ($\overline{OE}$) while write enable ($\overline{WE}$) remains HIGH. By presenting the address under these conditions, the data in the addressed memory location is presented on the data input/output pins. The input/output pins stay in the HIGH Z state when either $\overline{CE}$ or $\overline{OE}$ is HIGH or $\overline{WE}$ is LOW.

The P4C1041L comes in a 44-Pin 400 mil TSOP II package.

## FUNCTIONAL BLOCK DIAGRAM




## PIN CONFIGURATION




TSOP II

## MAXIMUM RATINGS[1]

| Sym | Parameter | Value | Unit |
|---|---|---|---|
| $V_{CC}$ | Power Supply Pin with Respect to GND | -0.5 to +7.0 | V |
| $V_{TERM}$ | Terminal Voltage with Respect to GND | -0.5 to $V_{CC}$ + 0.5 | V |
| $T_A$ | Operating Temperature | -40 to +85 | °C |
| $T_{BIAS}$ | Temperature Under Bias | -40 to +85 | °C |
| $T_{STG}$ | Storage Temperature | -65 to +150 | °C |
| $I_{OUT}$ | DC Output Current | 20 | mA |

## RECOMMENDED OPERATING CONDITIONS

| Grade[2] | Ambient Temp | GND | $V_{cc}$ |
|---|---|---|---|
| Commercial | 0°C to 70°C | 0V | 5.0V ± 10% |
| Industrial | -40°C to +85°C | 0V | 5.0V ± 10% |

## CAPACITANCES[4]

($V_{CC}$ = 5.0V, $T_A$ = 25°C, f = 1.0MHz)

| Sym | Parameter | Conditions | Typ | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $V_{IN}$=0V | 6 | pF |
| $C_{OUT}$ | Output Capacitance | $V_{OUT}$=0V | 8 | pF |

## DC ELECTRICAL CHARACTERISTICS

(Over Recommended Operating Temperature & Supply Voltage)[2]

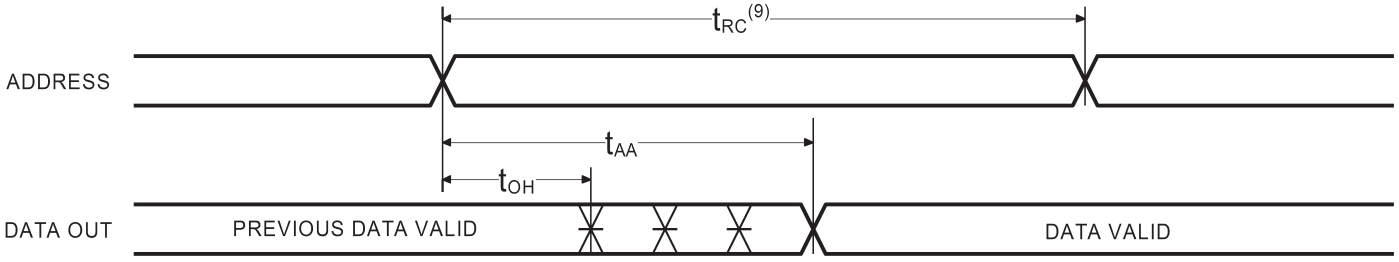
| Sym | Parameter | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 2.4 | $V_{CC}$ + 0.3 | V |
| $V_{IL}$ | Input Low Voltage | | -0.2 | 0.6 | V |
| $V_{OL}$ | Output Low Voltage (TTL Load) | $I_{OL}$ = +2 mA, $V_{CC}$ = Min | | 0.4 | V |
| $V_{OH}$ | Output High Voltage (TTL Load) | $I_{OH}$ = -1 mA, $V_{CC}$ = Min | 2.4 | | V |
| $I_{LI}$ | Input Leakage Current | $V_{CC}$ = Max, $V_{IN}$ = GND to $V_{CC}$ | -1 | +1 | µA |
| $I_{LO}$ | Output Leakage Current | $V_{CC}$ = Max,<br>$\overline{CE}$ = $V_{IH}$,<br>$V_{OUT}$ = GND to $V_{CC}$ | -1 | +1 | µA |
| $I_{SB1}$ | Standby Power Supply Current (CMOS Input Levels) | $\overline{CE}$ ≥ $V_{CC}$ - 0.2V,<br>$V_{CC}$ = Max,<br>f = 0, Outputs Open,<br>$V_{IN}$ ≥ $V_{CC}$ - 0.2V or<br>$V_{IN}$ ≤ 0.2V | — | 50 | µA |
| $I_{CC}$ | Dynamic Operating Current | Cycle Time = Min,<br>$\overline{CE}$ = $V_{IL}$,<br>$I_{I/O}$ = 0 mA,<br>Other pins at $V_{IH}$ or $V_{IL}$ | | 60 | mA |
| $I_{CC1}$ | Dynamic Operating Current (CMOS) | Cycle Time = 1 µs,<br>$\overline{CE}$ ≤ 0.2V,<br>$I_{I/O}$ = 0 mA,<br>Other pins at 0.2V or $V_{CC}$ - 0.2V | | 10 | mA |

## AC ELECTRICAL CHARACTERISTICS—READ CYCLE

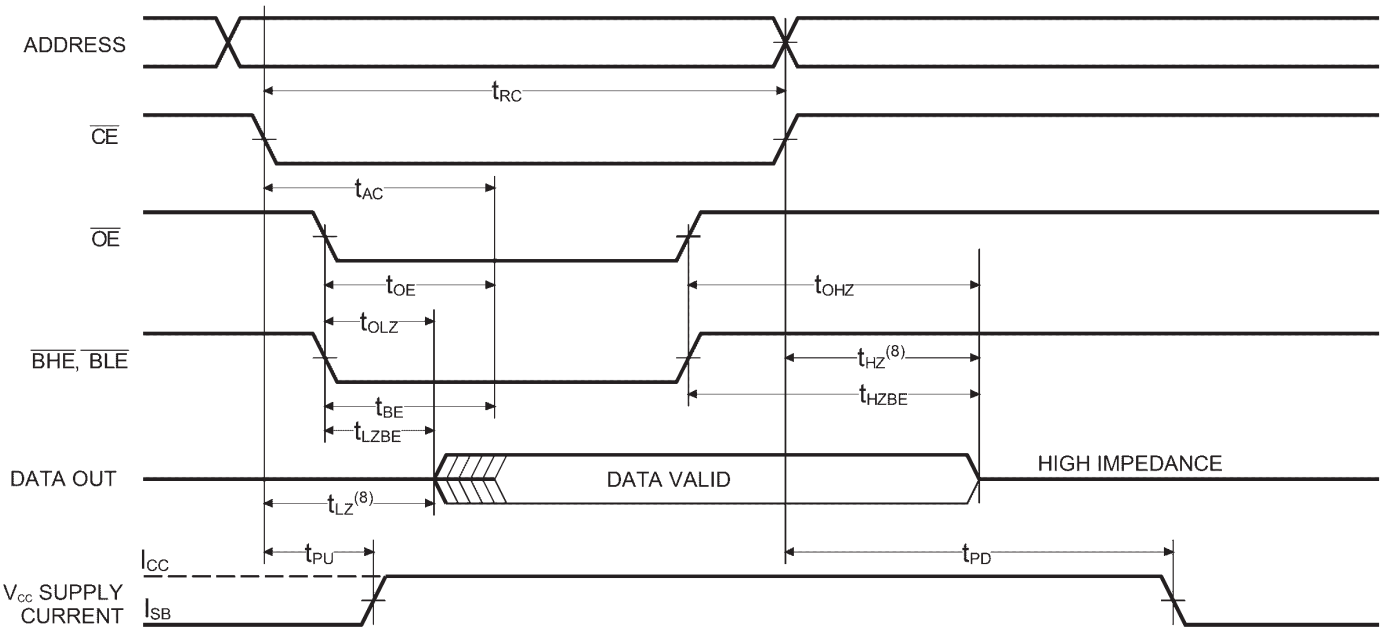
($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym | Parameter | -55 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{RC}$ | Read Cycle Time | 55 | | ns |
| $t_{AA}$ | Address Access Time | | 55 | ns |
| $t_{AC}$ | Chip Enable Access Time | | 55 | ns |
| $t_{OE}$ | Output Enable Access Time | | 30 | ns |
| $t_{LZ}$ | Chip Enable to Output in Low-Z | 10 | | ns |
| $t_{OLZ}$ | Output Enable to Output in Low-Z | 5 | | ns |
| $t_{HZ}$ | Chip Disable to Output in High-Z | | 20 | ns |
| $t_{OHZ}$ | Output Disable to Output in High-Z | | 20 | ns |
| $t_{OH}$ | Output Hold from Address Change | 10 | | ns |
| $t_{BE}$ | Byte Access Time | | 55 | ns |
| $t_{HZBE}$ | Byte Disable to High-Z Output | | 25 | ns |
| $t_{LZBE}$ | Byte Enable to Low-Z Output | 10 | | ns |

## TIMING WAVEFORM OF READ CYCLE NO. 1




## TIMING WAVEFORM OF READ CYCLE NO. 2 ($\overline{OE}$ CONTROLLED)(5,6)




**Notes:**

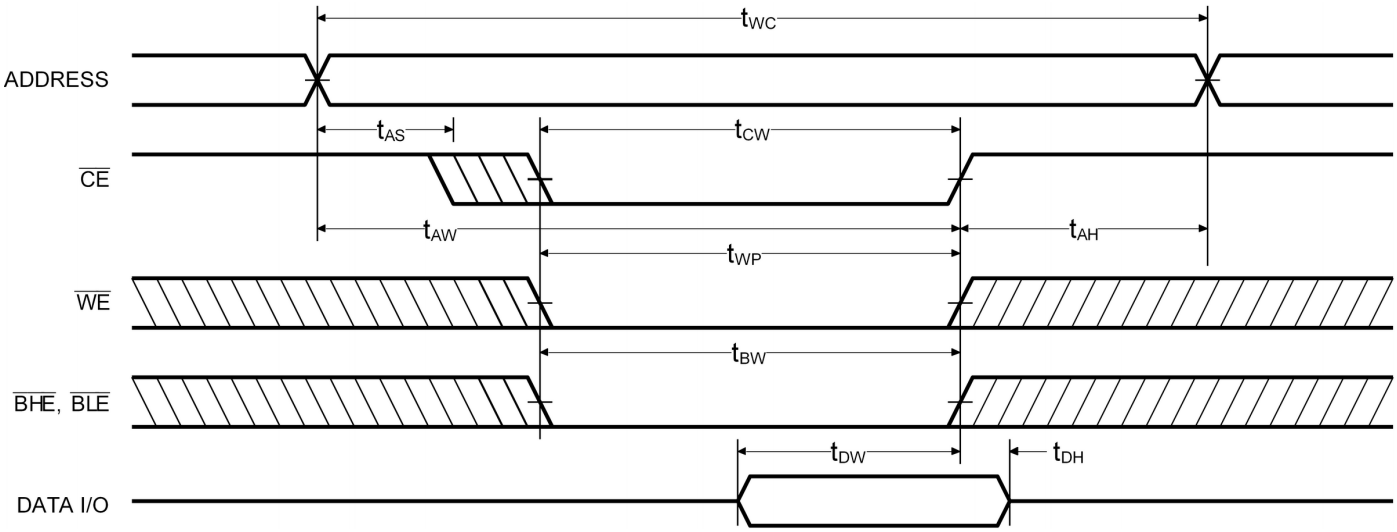
1. Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to MAXIMUM rating conditions for extended periods may affect reliability.
2. Extended temperature operation guaranteed with 400 linear feet per minute of air flow.
3. Transient inputs with $V_{IL}$ and $I_{IL}$ not more negative than –2.0V and –100mA, respectively, are permissible for pulse widths up to 20ns.
4. This parameter is sampled and not 100% tested.
5. $\overline{WE}$ is HIGH for READ cycle.
6. $\overline{CE}$ is LOW and $\overline{OE}$ is LOW for READ cycle.
7. ADDRESS must be valid prior to, or coincident with $\overline{CE}$ transition LOW.
8. Transition is measured ± 200 mV from steady state voltage prior to change, with loading as specified in Figure 1. This parameter is sampled and not 100% tested.
9. Read Cycle Time is measured from the last valid address to the first transitioning address.

## AC CHARACTERISTICS—WRITE CYCLE

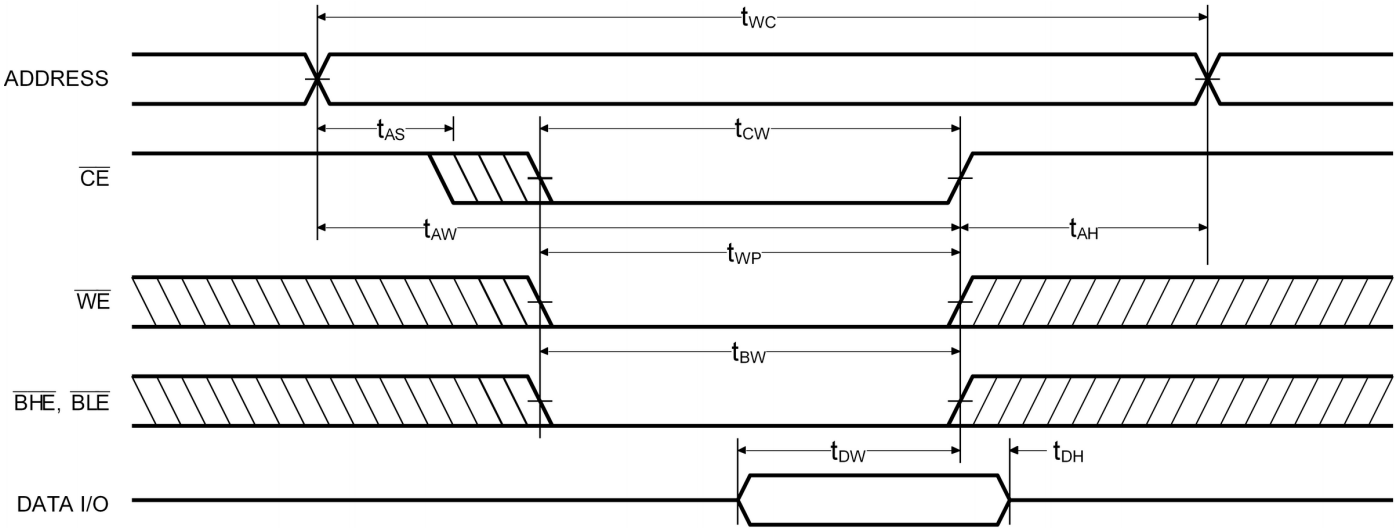
($V_{CC}$ = 5V ± 10%, All Temperature Ranges)[2]

| Sym | Parameter | -55 | | Unit |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{WC}$ | Write Cycle Time | 55 | | ns |
| $t_{AW}$ | Address Valid to End of Write | 50 | | ns |
| $t_{CW}$ | Chip Enable to End of Write | 50 | | ns |
| $t_{AS}$ | Address Setup Time | 0 | | ns |
| $t_{WP}$ | Write Pulse Width | 45 | | ns |
| $t_{WR}$ | Write Recovery Time | 0 | | ns |
| $t_{DW}$ | Data to Write Time Overlap | 25 | | ns |
| $t_{DH}$ | Data Hold from End of Write Time | 0 | | ns |
| $t_{OW}$ | Output Active from End of Write | 5 | | ns |
| $t_{WZ}$ | Write to Output in High-Z | | 20 | ns |
| $t_{BW}$ | Byte Enable to End of Write | 45 | | ns |

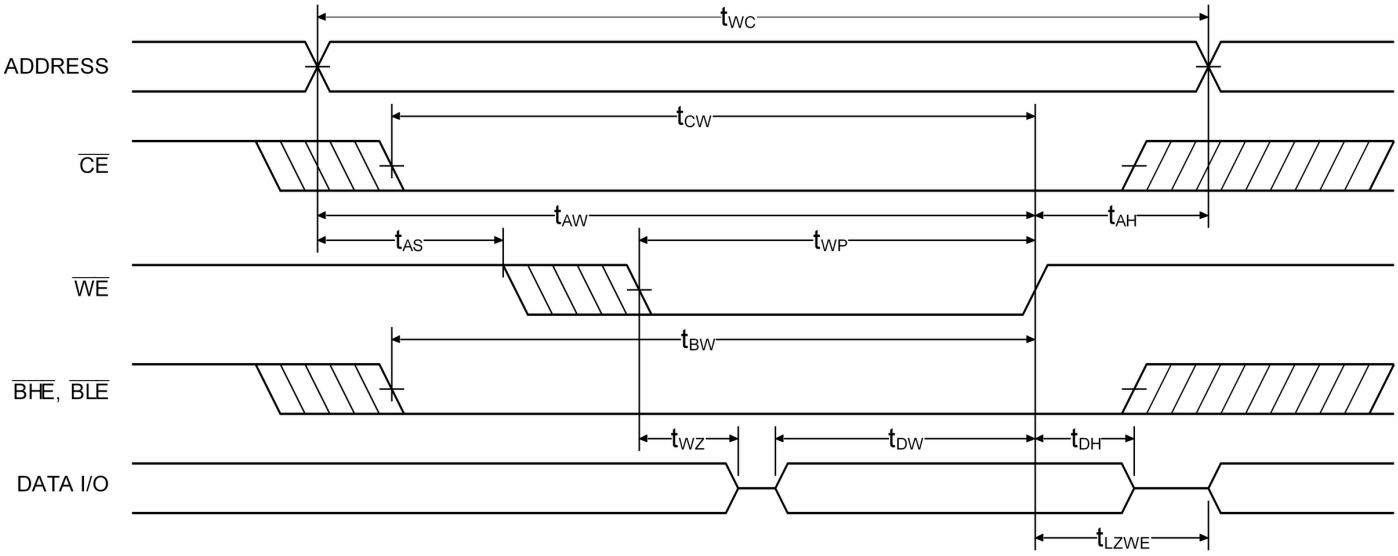
## TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{CE}$ CONTROLLED)



## TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{BLE}$ OR $\overline{BHE}$ CONTROLLED)




## TIMING WAVEFORM OF WRITE CYCLE NO. 3 ($\overline{WE}$ CONTROLLED, $\overline{OE}$ LOW)



## AC TEST CONDITIONS

| | |
|---|---|
| Input Pulse Levels | GND to 3.0V |
| Input Rise and Fall Times | 3ns |
| Input Timing Reference Level | 1.5V |
| Output Timing Reference Level | 1.5V |
| Output Load | See Figures 1 and 2 |

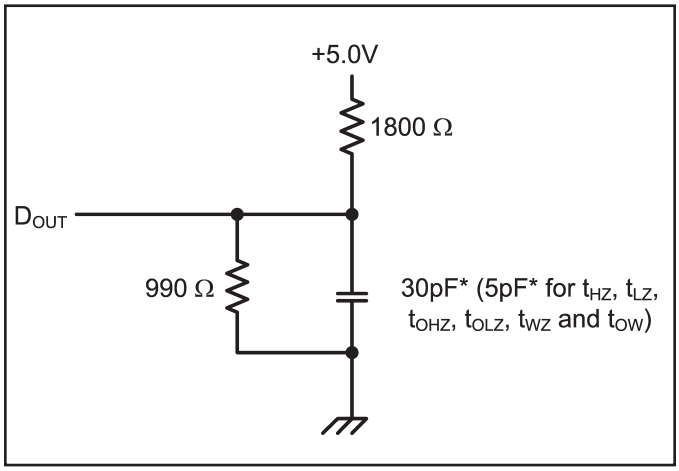



**Figure 1. Output Load**

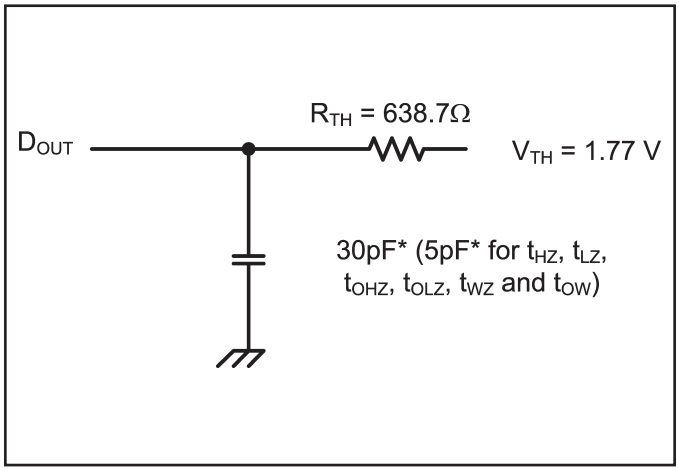



**Figure 2. Thevenin Equivalent**

* including scope and test fixture.

**Note:**
Because of the ultra-high speed of the P4C1041L, care must be taken when testing this device; an inadequate setup can cause a normal functioning part to be rejected as faulty. Long high-inductance leads that cause supply bounce must be avoided by bringing the $V_{CC}$ and ground planes directly up to the contactor fingers. A 0.01 µF high frequency capacitor is also required between $V_{CC}$ and ground. To avoid signal reflections, proper termination must be used; for example, a 50Ω test environment should be terminated into a 50Ω load with 1.77V (Thevenin Voltage) at the comparator input, and a 589Ω resistor must be used in series with $D_{OUT}$ to match 639Ω (Thevenin Resistance).

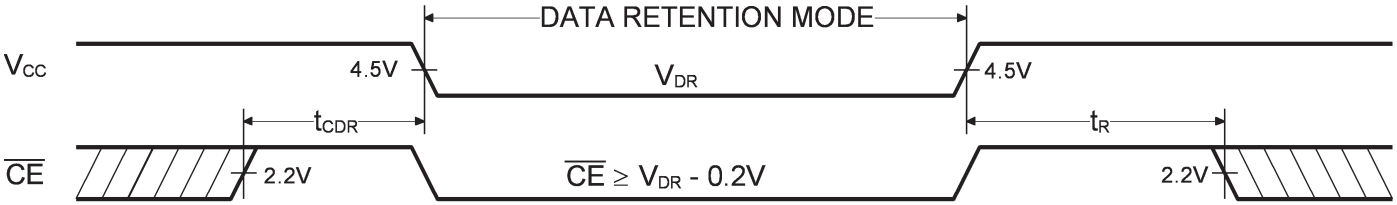
## TRUTH TABLE

| Mode | $\overline{CE}$ | $\overline{OE}$ | $\overline{WE}$ | $\overline{BLE}$ | $\overline{BHE}$ | $I/O_0$ - $I/O_7$ | $I/O_8$ - $I/O_{15}$ | Power |
|---|---|---|---|---|---|---|---|---|
| Powerdown | H | X | X | X | X | High Z | High Z | Standby |
| Read All Bits | L | L | H | L | L | $D_{OUT}$ | $D_{OUT}$ | Active |
| Read Lower Bits Only | L | L | H | L | H | $D_{OUT}$ | High Z | Active |
| Read Upper Bits Only | L | L | H | H | L | High Z | $D_{OUT}$ | Active |
| Write All Bits | L | X | L | L | L | $D_{IN}$ | $D_{IN}$ | Active |
| Write Lower Bits Only | L | X | L | L | H | $D_{IN}$ | High Z | Active |
| Write Upper Bits Only | L | X | L | H | L | High Z | $D_{IN}$ | Active |
| Selected, Outputs Disabled | L | H | H | X | X | High Z | High Z | Active |

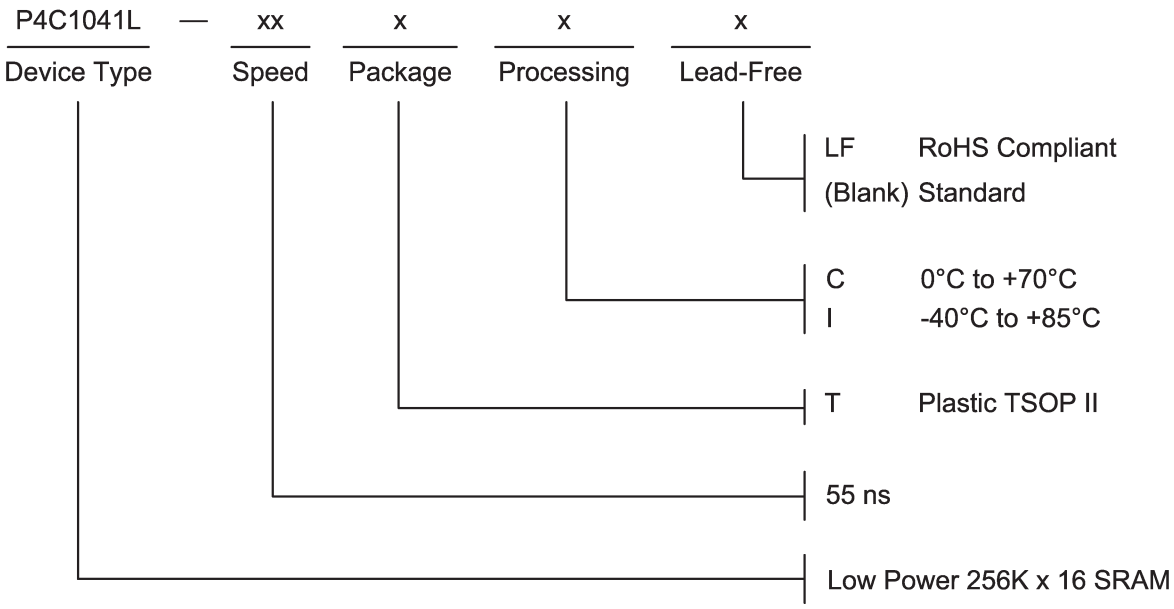
## DATA RETENTION

| Sym | Parameter | Test Conditions | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{DR}$ | VCC for Data Retention | $\overline{CE} \geq V_{CC}$ - 0.2V, $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq 0.2V$ | 2.0 | 5.5 | V |
| $I_{CCDR}$ | Data Retention Current | $V_{DR}$=2.0V | | 30 | µA |
| $t_{CDR}$ | Chip Deselect to Data Retention Time | See Retention Waveform | 0 | | ns |
| $t_R$ | Operating Recovery Time | | $t_{RC}$ | | ns |

## LOW $V_{CC}$ DATA RETENTION WAVEFORM

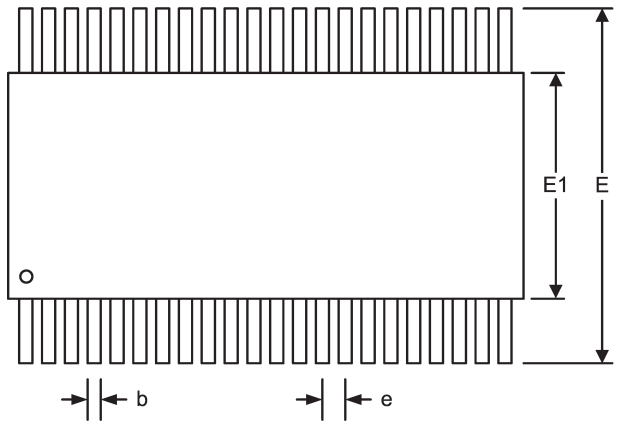


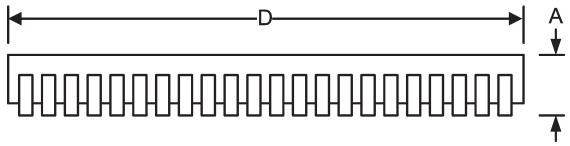
## ORDERING INFORMATION

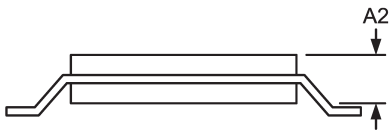


| Pkg # | T2 | |
|---|---|---|
| # Pins | 44 | |
| Symbol | **Min** | **Max** |
| A | 0.039 | 0.047 |
| $A_2$ | 0.033 | 0.045 |
| b | 0.012 | 0.017 |
| D | 0.717 | 0.733 |
| e | 0.0315 BSC | |
| E | 0.453 | 0.473 |
| E1 | 0.392 | 0.408 |

## TSOP II SMALL OUTLINE PACKAGE



## REVISIONS

| | |
|---|---|
| **DOCUMENT NUMBER** | SRAM 142 |
| **DOCUMENT TITLE** | P4C1041L - LOW POWER 256K X 16 STATIC CMOS RAM |

| REV | ISSUE DATE | ORIGINATOR | DESCRIPTION OF CHANGE |
|---|---|---|---|
| OR | Mar-2011 | JDB | New Data Sheet |