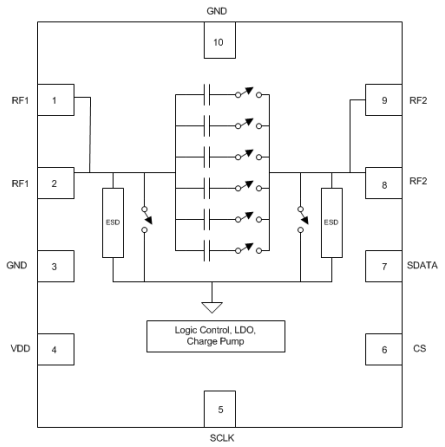
RFAC3612

6-Bit, PAC (Programmable Array of Capacitors)

The RFAC3612 is a 6-bit, 64-state PAC (Programmable Array of Capacitors) for tunable RF applications. The RFAC3612 is optimized for series configuration but can also be applied in shunt configuration. The high power handling, high Q and excellent linearity makes it ideal for use in antenna tuning, tunable filters and tunable matching networks.

The RFAC3612 includes an integrated LDO (Low Drop Out) regulator, which enables operation from a very wide supply range from 2.4V to 3.5V. The state of the RFAC3612 PAC is controlled by a 3 wire SPI compatible interface. All pins are ESD protected to ensure 2kV HBM ESD tolerance. RFAC3612 is packaged in a very compact 2.0mm x 2.5mm, 10-pin package.



Functional Block Diagram

Ordering Information

RFAC3612SQ	Sample bag with 25 pieces
RFAC3612SR	7" Reel with 100 pieces
RFAC3612TR7	7" Reel with 2500 pieces
RFAC3612PCK-410	0.5GHz to 3GHz PCBA with 5-piece sample bag

Package: 10-pin,
2.0mm x 2.5mm

Features

- 6-Bit, 64-state Programmable Capacitor Array
- 3 Wire SPI Compatible Control
- Programmable Shunt Switches on Both RF Ports for High Isolation Operation
- Wide Tuning Range (0.47pF to 13pF)
- High RF Voltage Handling (≤44VPK)
- High Linearity
- Wide Voltage Supply Range (2.4V to 3.5V)
- Low Current Consumption (64µA Typical)
- 2kV HBM EDS Tolerance on All Ports
- Simulate in Your Design with ADS or AWR S-parameter Model Kit, available on request

Applications

- Antenna Tuning Networks
- Tunable RF Filters
- Tunable RF Matching Networks
- Phase Shifters

RF Micro Devices Inc. 7628 Thorndike Road, Greensboro, NC 27409-9421
For sales or technical support, contact RFMD at +1.336.678.5570 or customerservice@rfmd.com.

DS140530

Absolute Maximum Ratings

Parameter	Rating	Unit
Power Supply Voltage (V_{DD})	-0.3 to 3.9	V
Logic Input DC Voltage (V_{CB})	-0.3 to 2.8	V
ESD Voltage HBM	2	kV
Storage Temperature	-40 to 150	°C
Max peak Single-ended RF Voltage Between RF1/RF2 and Ground, Shunt Switches Disabled	RF1 = 45	V_{PK}
	RF2 = 43	V_{PK}
CW Input Power, 50Ω Systems, RF1 or RF2, Cmin, Shunt Switches Disabled	37	dBm
CW Input Power, 50Ω Systems, Shunt, RF1, Cmin, Shunt Switches Disabled	42.5	dBm
CW Input Power, 50Ω Systems, RF1 or RF2, Shunt Switches Enabled	29	dBm

Caution! ESD sensitive device.

RFMD Green: RoHS status based on EU Directive 2011/65/EU (at time of this document revision), halogen free per IEC 61249-2-21, < 1000ppm each of antimony trioxide in polymeric materials and red phosphorus as a flame retardant, and <2% antimony in solder.

Exceeding any one or a combination of the Absolute Maximum Rating conditions may cause permanent damage to the device. Extended application of Absolute Maximum Rating conditions to the device may reduce device reliability. Specified typical performance or functional operation of the device under Absolute Maximum Rating conditions is not implied.

Recommended Operating Condition

Parameter	Specification			Unit
	Min	Typ	Max	
Operating Temperature Range	-40		+85	°C
Operating Junction Temperature				°C
Supply Voltage	2.4		3.5	V

Electrical Specifications

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Operating Ranges					
Power Supply Current (I_{DD})		63	85	µA	RF1 = -10dBm
Input Logic Control Voltage High (V_{IH})	1.2		2.8	V	
Input Logic Control Voltage Low (V_{IL})	0		0.63	V	
Max Peak Single-ended RF Voltage Between RF1/RF2 and GND ($V_{RF\ PK}$)			44	V_{PK}	RF1
			42	V_{PK}	RF2
Input Power with RF1 and/or RF2 Shunt Switches Enabled			27	dBm	
DC Voltage at RF1 and RF2 Ports ($V_{RF,\ DC}$) [1]		0		V	
Operating Frequency Range	0.5		3	GHz	
Series Configuration, Linear Parameters					**Nominal Conditions: V_{HIGH} ≥1.8V, V_{LOW} ≤0.3V, VDD = 2.85V, Temp = 25°C, RF1 and RF2 ports terminated to Z0 = 50Ω**
Cs [2]					
Min Series Capacitance, State 0	0.41	0.46	0.51	pF	

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Series Capacitance, State 1	0.59	0.66	0.72	pF	
Series Capacitance, State 2	0.77	0.86	0.91	pF	
Series Capacitance, State 4	1.13	1.26	1.38	pF	
Series Capacitance, State 8	1.85	2.05	2.26	pF	
Series Capacitance, State 16	3.28	3.64	4.01	pF	
Series Capacitance, State 32	6.15	6.83	7.51	pF	
Max Series Capacitance, State 63	11.7	13	14.3	pF	
Capacitance Step ($C_{STEP\ SERIES}$)		0.2		pF	
Port Capacitance to Ground (Cp) [2]		0.4		pF	
Total Series Inductance – Two Sided (Ls) [2]		0.8		nH	
Series Self-resonance Frequency ($f_{RES\ SERIES}$)					
State 16		2700		MHz	
State 32		2130		MHz	
State 63		1625		MHz	
Rp1[2]		2.5		Ω	
Rp2[2]		16		Ω	When either shunt switch is on, the Rp2 on that side reduces to this value
		4800		Ω	Normal operation with shunt switches open
Quality Factor (RF2 Port Grounded, Inductance Removed) (Q)					
State 0		23			f = 1GHz
State 31		17			
State 63		15			
State 0		42			f = 2GHz
State 31		8			
Series Configuration, Nonlinear Parameters					
Second Harmonic, 2-f_0 ($P_{2H\ SERIES}$)					
States 0 to 3		-72	-43	dBm	P_{FWD} = 35dBm, f_0 = 900MHz
States 4 to 63		-55	-40	dBm	P_{FWD} = 36dBm, f_0 = 900MHz
States 0 to 63		-70		dBm	P_{FWD} = 33dBm, f_0 = 1910MHz
Third Harmonic, 3-f_0 ($P_{3H\ SERIES}$)					
States 0 to 7		-60	-34	dBm	P_{FWD} = 35dBm, f_0 = 900MHz
States 8 to 63		-59	-40	dBm	P_{FWD} = 36dBm, f_0 = 900MHz

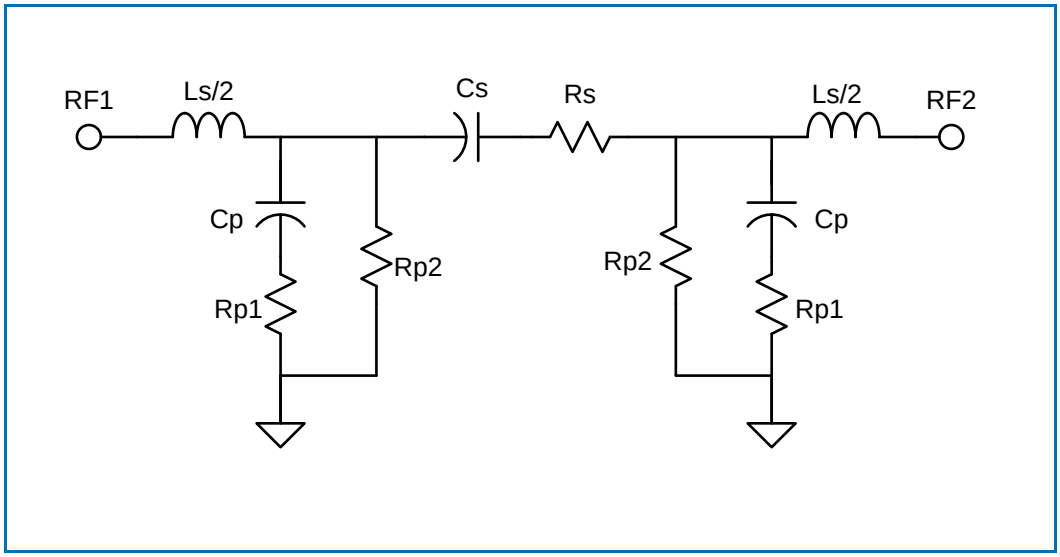
Parameter	Specification			Unit	Condition
	Min	Typ	Max		
States 0 to 63		-65		dBm	P_{FWD} = 33dBm, f_0 = 1910MHz
Series Configuration, Nonlinear Parameters – Cont.					
Input IP2 – States 0 to 63 ($IP2_{SERIES}$)					
Cell Low		115		dBm	See IP2 / IP3 test conditions table below
Cell High		132		dBm	
IMT Low		129		dBm	
IMT High		130		dBm	See IP2 / IP3 test conditions table below
GPS Test 1		140		dBm	
GPS Test 2		140		dBm	
Band 8 (800MHz to 960MHz)		126		dBm	Tone 1 at 20dBm
Bands 2, 4, 7, 11 (1428MHz to 2690MHz)		128		dBm	Tone 2 at -15dBm
Input IP3 (States 0 to 63 ($IP3_{SERIES}$)					
Cell (B5)		75		dBm	See IP2 / IP3 test conditions table below
IMT (B1)		76		dBm	
SV – LTE Test 1		77		dBm	
SV – LTE Test 2		85		dBm	
Band 8 (800MHz to 960MHz)		76		dBm	**Tone 1 at 20dBm**
Bands 2, 4, 7, 11 (1428MHz to 2690MHz)		70		dBm	Tone 2 at -15dBm
RF1 to RF2 Spurious (all States					
No RF		-120		dBm	400MHz to 2700MHz
915MHz at 35dBm		-112		dBm	925MHz to 960MHz
1910MHz at 33dBm		-113		dBm	1930MHz to 1990MHz
General Electrical Specifications					
Power-up Time ($t_{POWER-UP}$)		75		µs	Time from VDD within specification to all specifications is met.
Switching Time-Small Signal ($t_{SWITCH, SS}$)		15		µs	Time from programming (falling edge of SCLK of the 16th bit) to 90% of capacitance change achieved
Stitching Time – Large Signal ($t_{SWITCH, LS}$)		75		µs	Time from programming (falling edge of SCLK of the 16th bit) to power handling and linearity specifications are met
3-Wire Interface Timing Characteristics					
Serial Clock Frequency ($f_{SCLK} = 1/t_{SCLK}$) [3]			26	MHz	
Clock High and Low Time ($t_{SCLKHIGH}$, $t_{SCLKLOW}$)	0.45 x t_{SCLK}		0.55 x t_{SCLK}		
Falling Edge of CS to Rising Edge of SCLK Set-up Time, Start of Telegram (t_{CS_SCLK})	10			ns	

Parameter	Specification			Unit	Condition
	Min	Typ	Max		
Falling Edge of SCLK to Rising Edge of CS Set-up Time, End of Telegram (t_{SCLK_SC})	20			ns	
3-Wire Interface Timing Characteristics – Cont.					
SDATA to Falling Edge of SCLK Set-up Time (t_{SDATA_SCLK})	10			ns	
SDATA Hold Time After Falling Edge of SCLK (t_{SDATA})	10			ns	
CS High Time for Activation of Programmed Bits (t_{CSHIGH})	100			ns	

NOTES:

1. RF1 and RF2 ports are internally DC coupled and should not have any non-zero DC bias voltage during operation.
2. Equivalent circuit below for C_S, Cp, R_S, $L_{S/2}$, Rp1, and Rp2
3. Corresponds to a minimum clock cycle time of 38.5ns.

Equivalent Model

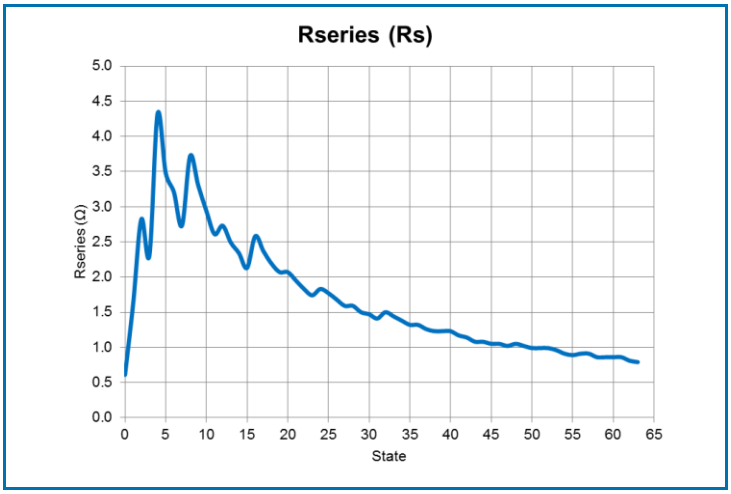


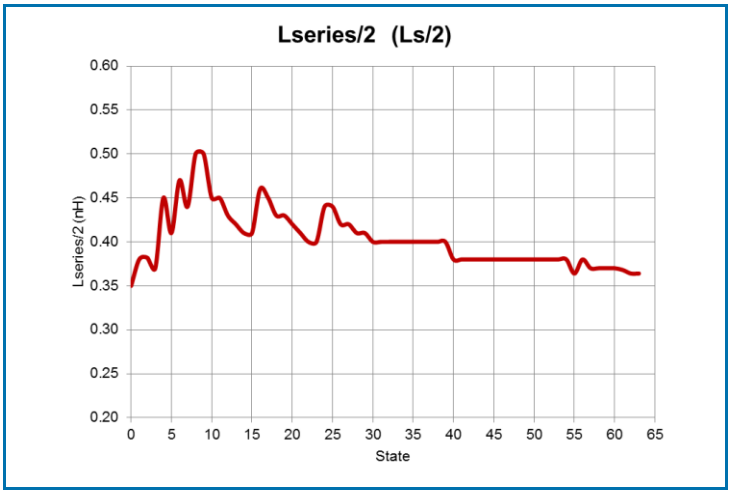
Equivalent Circuit Model Parameters

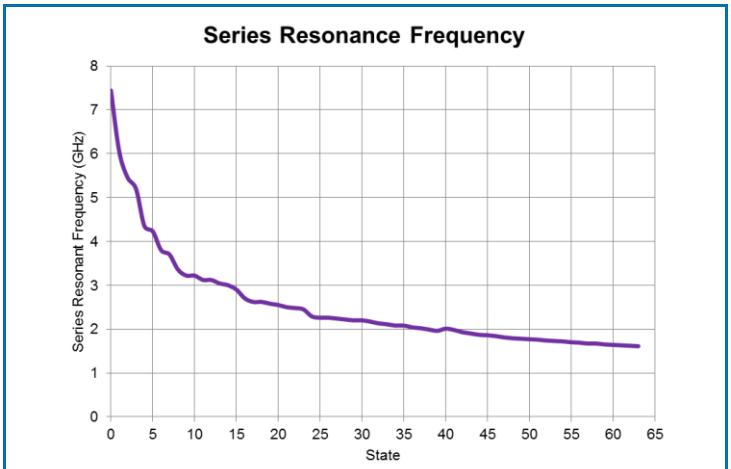
Variable	Equation (State = 0, 1, ..., 63	Units
Cs	0.199 * state + 0.46	pF
Rs	37 / (State + 35 / (state + 0.3)) +0.25	Ω
Rp1	2.5	Ω
Rp2	4800	Ω
Cp	0.4	pF
Ls/2	0.4	nH

NOTE: Equivalent circuit will provide simulation results very close to actual, but for best accuracy request s-parameters kit.

Typical Performance: T = 25°C, V_{DD} = 5V unless otherwise noted





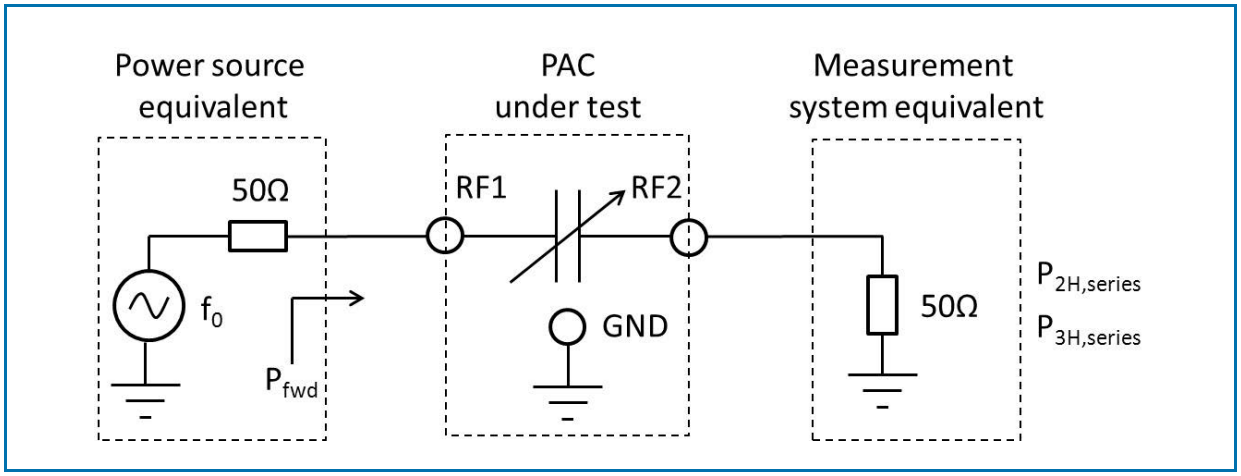


IP2 / IP3 Test Conditions

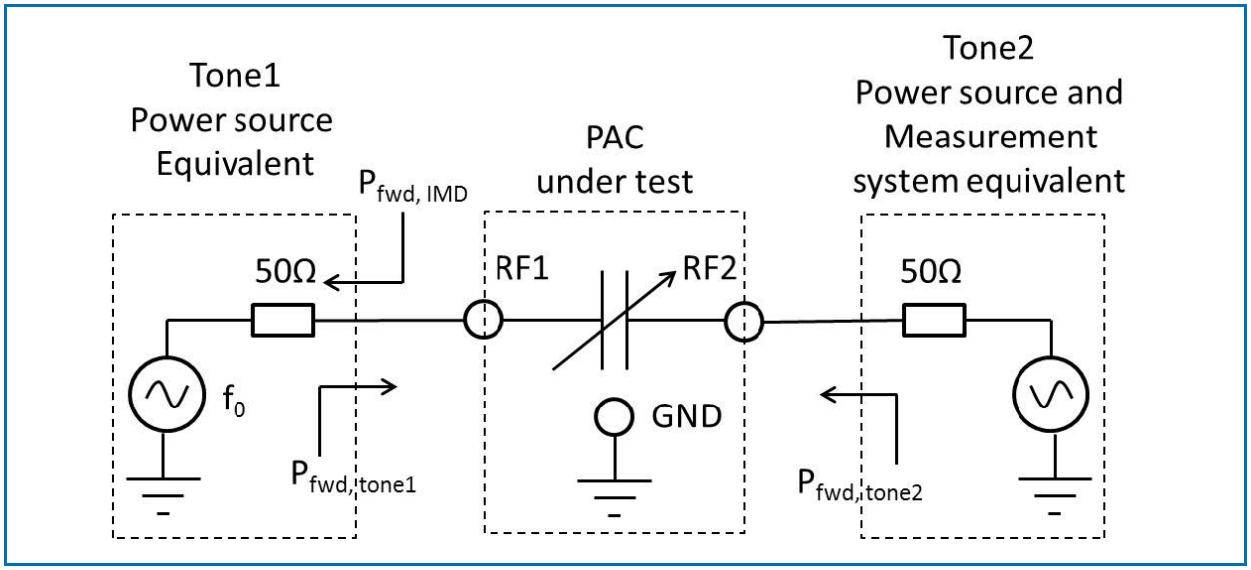
Band	In-band Frequency	CW Tone 1		CW Tone 2	
	MHz	MHz	dBm	MHz	dBm
IP2 Test Conditions					
Cell Low (Band V)	881.5	836.5	+20	45	-15
Cell High (Band V)	881.5	836.5	+26	1718	-20
IMT Low (Band I)	2140	1950	+20	190	-15
IMT High (Band I)	2140	1950	+26	4090	-20
GPS Test Conditions					
GPS Test 1	1575	909	+21	2484	+1.5
GPS Test 2	1575	909	+14	2484	+1.5
IP3 Test Conditions					
Cell (Band V)	881.5	836.5	+26	791.5	-20
IMT (Band I)	2140	1950	+26	1760	-20
SV-LTE Test Conditions					
SV-LTE Test 1	747	825	+11	786	+24
SV-LTE Test 2	872	827	+11	782	+24

Test Set-up

Series Configuration Harmonics Measurement Set-up



Series Configuration IMDs Measurement Set-up



Test Set-up

The RFAC3612 is controlled by a single direction 3-wire SPI compatible interface. The RFAC3612 has 3 logic input pins for:

SCLK: Serial Input, **SDATA:** Serial Data Input; **CS:** Chip Select

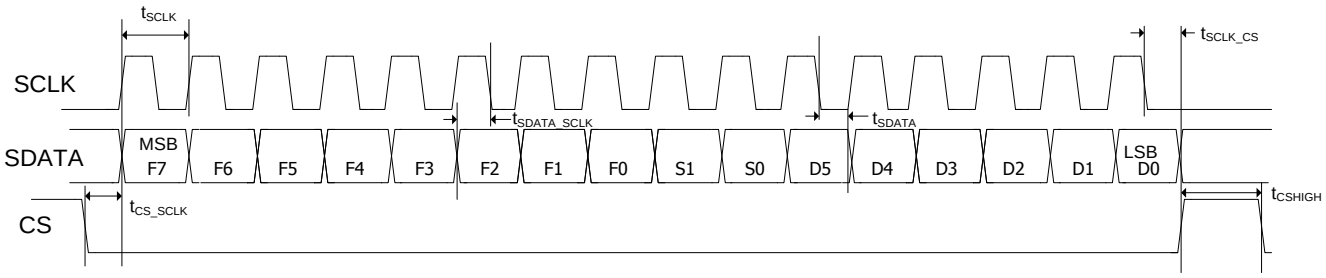
The serial master initiates the start of the telegram by driving the chip select signal CS low. Each bit in the 16-bit telegram is clocked in by the slave on the falling edge of SCLK.

SDATA bits consist of 3 groups:

F0 to F7: are fixed bits, these do not change.

S0 to S1: controls the RF1 and RF2 shunt switches

D5 to D0: is the 6-bit data word, used for controlling the PAC. SDATA bits are clocked in the order shown below, with D5 being the first bit. The PAC activates the clocked values of SDATA on the falling edge of SCLK of the 16th bit.



A quick overview of the telegram bits is shown below.

Telegram Bits	Function and Description
F0-F7	8-bit set of fixed bits, must be set to 00100000
S1	Data bit S1, controls shunt switch on port RF2. 0 = shunt switch is Off, 1 = shunt switch is On. After power-up the value of S1 is 0, i.e. shunt switch is Off.
S0	Data bit S0, controls shunt switch on port RF1. 0 = shunt switch is Off, 1 = shunt switch is On. After power-up the value of S0 is 0, i.e. shunt switch is Off.
D0-D5	Data bit D0-D5, controls the state of PAC. (D5 is most significant bit, D0 is least significant bit). After power-up the value of D0-D5 is 000000, i.e. state 0.

Equivalent Circuit Parameters

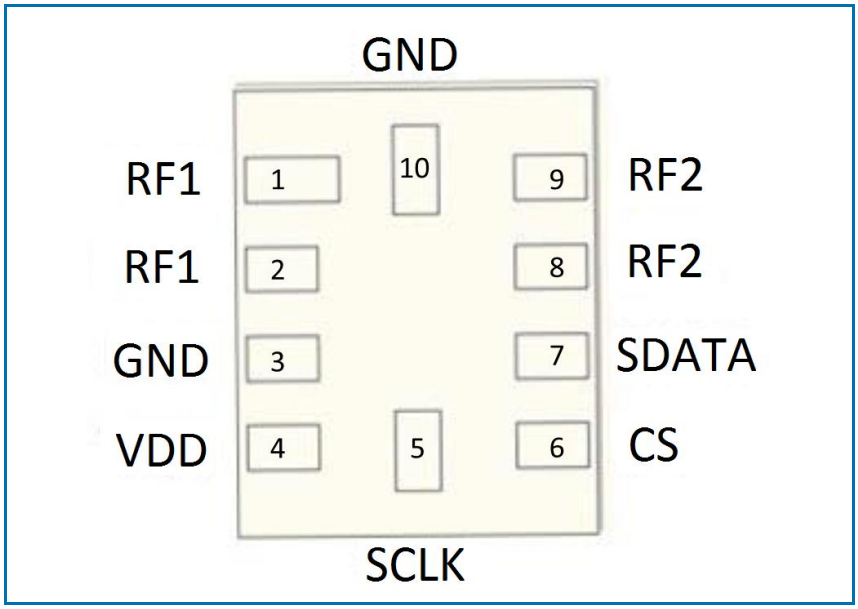
	S1	S0	D5	D4	D3	D2	D1	D0	Rs (Ω)	Ls/2 (nH)	Cs (pF)
State 0	0	0	0	0	0	0	0	0	0.61	0.35	0.46
State 1	0	0	0	0	0	0	0	1	1.62	0.38	0.66
State 2	0	0	0	0	0	0	1	0	2.82	0.38	0.86
State 3	0	0	0	0	0	0	1	1	2.31	0.37	1.06
State 4	0	0	0	0	0	1	0	0	4.32	0.45	1.26
State 5	0	0	0	0	0	1	0	1	3.48	0.41	1.46
State 6	0	0	0	0	0	1	1	0	3.21	0.47	1.65
State 7	0	0	0	0	0	1	1	1	2.73	0.44	1.85
State 8	0	0	0	0	1	0	0	0	3.72	0.50	2.05
State 9	0	0	0	0	1	0	0	1	3.30	0.50	2.25
State 10	0	0	0	0	1	0	1	0	2.94	0.45	2.45
State 11	0	0	0	0	1	0	1	1	2.61	0.45	2.65
State 12	0	0	0	0	1	1	0	0	2.73	0.43	2.85
State 13	0	0	0	0	1	1	0	1	2.49	0.42	3.05
State 14	0	0	0	0	1	1	1	0	2.34	0.41	3.25
State 15	0	0	0	0	1	1	1	1	2.13	0.41	3.45
State 16	0	0	0	1	0	0	0	0	2.58	0.46	3.64
State 17	0	0	0	1	0	0	0	1	2.37	0.45	3.84
State 18	0	0	0	1	0	0	1	0	2.19	0.43	4.04
State 19	0	0	0	1	0	0	1	1	2.07	0.43	4.24
State 20	0	0	0	1	0	1	0	0	2.07	0.42	4.44
State 21	0	0	0	1	0	1	0	1	1.95	0.41	4.64
State 22	0	0	0	1	0	1	1	0	1.83	0.40	4.84
State 23	0	0	0	1	0	1	1	1	1.74	0.40	5.04
State 24	0	0	0	1	1	0	0	0	1.83	0.44	5.24
State 25	0	0	0	1	1	0	0	1	1.77	0.44	5.44
State 26	0	0	0	1	1	0	1	0	1.68	0.42	5.63
State 27	0	0	0	1	1	0	1	1	1.59	0.42	5.83
State 28	0	0	0	1	1	1	0	0	1.59	0.41	6.03
State 29	0	0	0	1	1	1	0	1	1.50	0.41	6.23
State 30	0	0	0	1	1	1	1	0	1.47	0.40	6.43
State 31	0	0	0	1	1	1	1	1	1.41	0.40	6.63
State 32	0	0	1	0	0	0	0	0	1.50	0.40	6.83
State 33	0	0	1	0	0	0	0	1	1.44	0.40	7.03
State 34	0	0	1	0	0	0	1	0	1.38	0.40	7.23

	S1	S0	D5	D4	D3	D2	D1	D0	Rs (Ω)	Ls/2 (nH)	Cs (pF)
State 35	0	0	1	0	0	0	1	1	1.32	0.40	7.43
State 36	0	0	1	0	0	1	0	0	1.32	0.40	7.62
State 37	0	0	1	0	0	1	0	1	1.26	0.40	7.82
State 38	0	0	1	0	0	1	1	0	1.23	0.40	8.02
State 39	0	0	1	0	0	1	1	1	1.23	0.40	8.22
State 40	0	0	1	0	1	0	0	0	1.23	0.38	8.42
State 41	0	0	1	0	1	0	0	1	1.17	0.38	8.62
State 42	0	0	1	0	1	0	1	0	1.14	0.38	8.82
State 43	0	0	1	0	1	0	1	1	1.08	0.38	9.02
State 44	0	0	1	0	1	1	0	0	1.08	0.38	9.22
State 45	0	0	1	0	1	1	0	1	1.05	0.38	9.42
State 46	0	0	1	0	1	1	1	0	1.05	0.38	9.61
State 47	0	0	1	0	1	1	1	1	1.02	0.38	9.81
State 48	0	0	1	1	0	0	0	0	1.05	0.38	10.01
State 49	0	0	1	1	0	0	0	1	1.02	0.38	10.21
State 50	0	0	1	1	0	0	1	0	0.99	0.38	10.41
State 51	0	0	1	1	0	0	1	1	0.99	0.38	10.61
State 52	0	0	1	1	0	1	0	0	0.99	0.38	10.81
State 53	0	0	1	1	0	1	0	1	0.96	0.38	11.01
State 54	0	0	1	1	0	1	1	0	0.91	0.38	11.21
State 55	0	0	1	1	0	1	1	1	0.89	0.36	11.41
State 56	0	0	1	1	1	0	0	0	0.91	0.38	11.60
State 57	0	0	1	1	1	0	0	1	0.91	0.37	11.80
State 58	0	0	1	1	1	0	1	0	0.86	0.37	12.00
State 59	0	0	1	1	1	0	1	1	0.86	0.37	12.20
State 60	0	0	1	1	1	1	0	0	0.86	0.37	12.40
State 61	0	0	1	1	1	1	0	1	0.86	0.37	12.60
State 62	0	0	1	1	1	1	1	0	0.81	0.36	12.80
State 63	0	0	1	1	1	1	1	1	0.79	0.36	13.00

Shunt Switch Table

RF1 Shunt Switch	RF2 Shunt Switch	S1	S0
Off	Off	0	0
On	Off	0	1
Off	On	1	0
On	On	1	1

Pin Configuration Top View

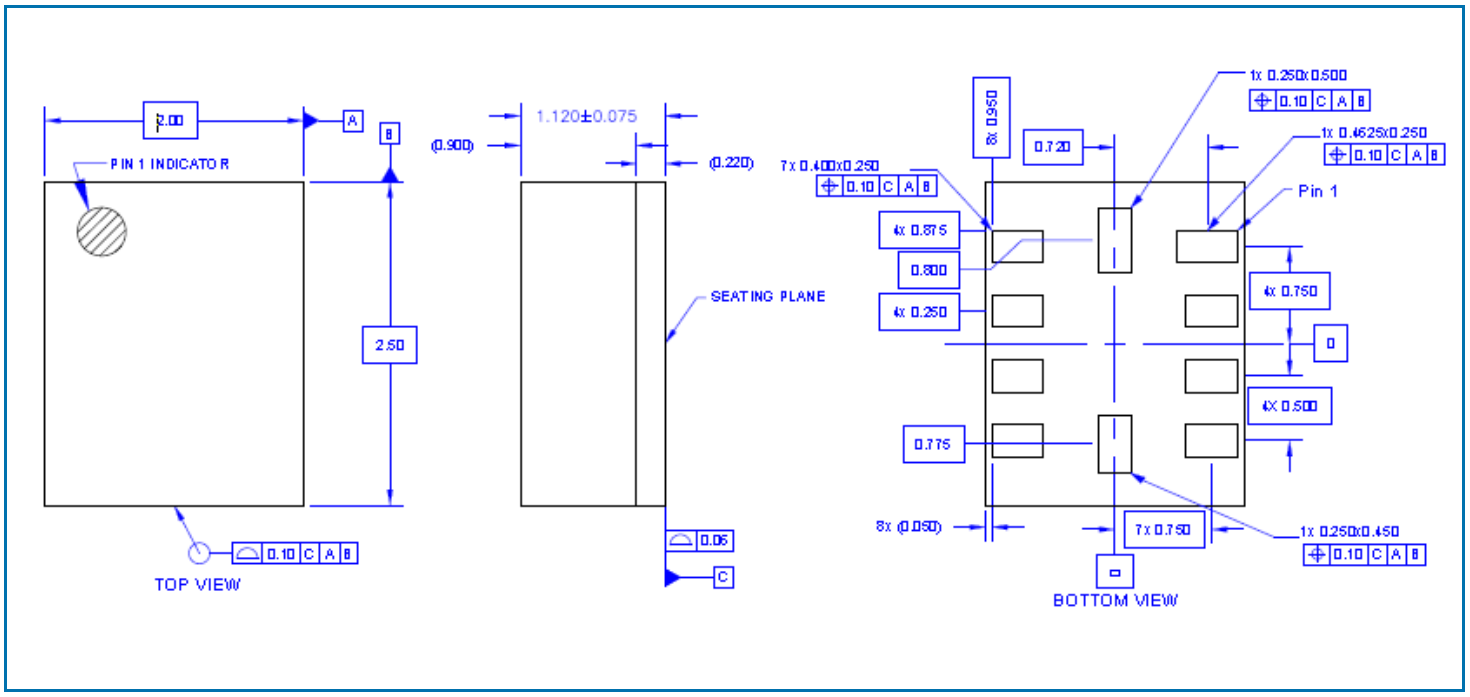


Pin Names and Descriptions

Pin	Name	Description
1	RF1	RF Terminal 1 of PAC
2	RF1	RF Terminal 1 of PAC
3[1]	GND	Ground Pins
4	VDD	Power Supply Pin
5	SCLK	Serial Interface Clock Signal
6	CS	Enable Pin
7	SDATA	Serial Interface Data Signal
8	RF2[2]	RF Terminal 2 of PAC
9	RF2[2]	RF Terminal 2 of PAC
10[1]	GND	Ground Pins

Notes:
1. 2 ground pins are connected internally on die. The 2 pins should all be connected to PCB GND.
2. When operating the PAC in shunt configuration, it is recommended to ground RF2 rather than RF1.

Package Outline Drawing (Dimensions in millimeters)



Evaluation Board Available with 1 Port Shunt and 2 Port Series Configurations

Application Guidelines

A decoupling capacitor on VDD may be used for noise reduction. The one directional 3-wire SPI compatible interface with chip select is a very robust interface for on-board inter chip signaling. To further improve the robustness of the interface RFMD uses input level hysteresis on the 3 logic inputs. This gives good immunity to noise on the input lines.

The PAC is DC coupled on RF1 and RF2 ports, with a bias voltage of 0V. This means that the RF ports can be DC shorted to GND, by e.g. an inductor, but they cannot be connected to any other device with a non-zero bias voltage without a DC blocking capacitor.

Application Note

Turn On Sequence = VDD → SPI→ RF

Turn Off Sequence = RF → SPI → VDD

Branding Diagram