FEATURES

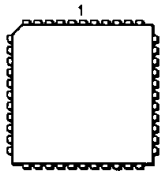
- ☐ Direct interface to SC11024 or SC11006 single chip modem
- ☐ Complete "AT" command set in internal firmware
- ☐ Built-in UART
- ☐ Direct IBM PC bus interface
- ☐ CMOS technology
- ☐ G3 Fax added with SC11074,75
- ☐ External ROM/RAM addressable
- ☐ 40 mW Power-Down Mode
- ☐ Four-bit general I/O port
- ☐ RS-232 interface
- ☐ Synchronous and asynchronous communication supported

GENERAL DESCRIPTION

The Modem Advanced Controller (MAC) is a specialized controller which interfaces directly to SC11006 or SC11024 Modem Analog Processor (MAP) to implement a 2400 bps full duplex intelligent modem. The two-chip set performs all the modem functions as well as automatic control features compatible to the Hayes "AT" Command Set. The chip set conforms to CCITT V.22 bis with V.22 fallback, Bell 212A with 103 fallback, as well as V.21 standards.

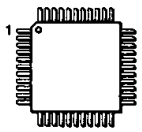
The SC11019 and SC11023 interface to a parallel system bus, such as that in the IBM PC, while the SC11020 interfaces to an RS-232 port. Both SC11019 and SC11023 have an onboard 16C450 equivalent UART. The new SC11074,75 versions are programmed to support the 9600 Sendfax MAC (SC11054). They are available in 44 pin PLCC, 44 pin QFP or 48 pin DIP packages.

44-PIN PLCC PACKAGE



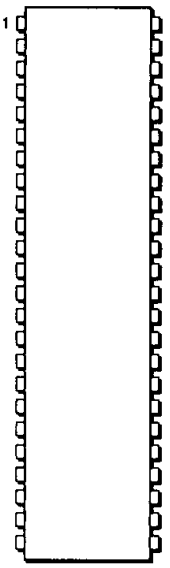
SC11019/SC11020/SC11023/SC11074/
SC11075CV

44-PIN QFP (10mm) PACKAGE



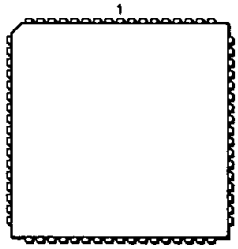
SC11074/SC11075CQ

48-PIN DIP PACKAGE



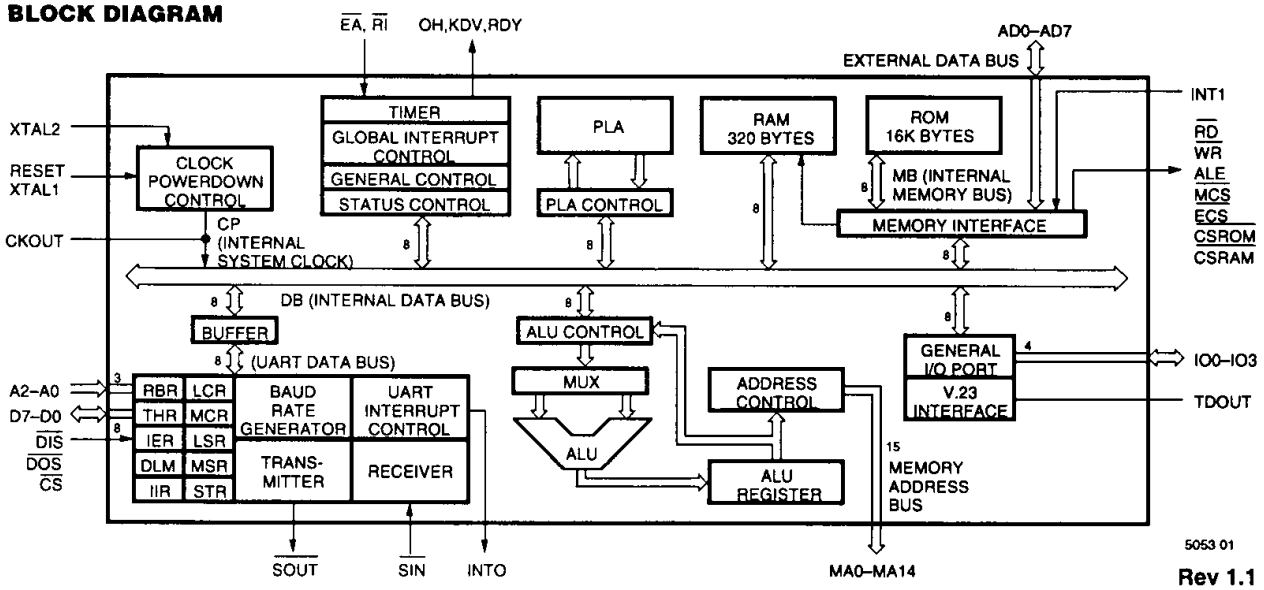
SC11019/SC11020/SC11022/
SC11074/SC11075CN

68-PIN PLCC PACKAGE



SC11021/SC11022CV

BLOCK DIAGRAM



Rev 1.1

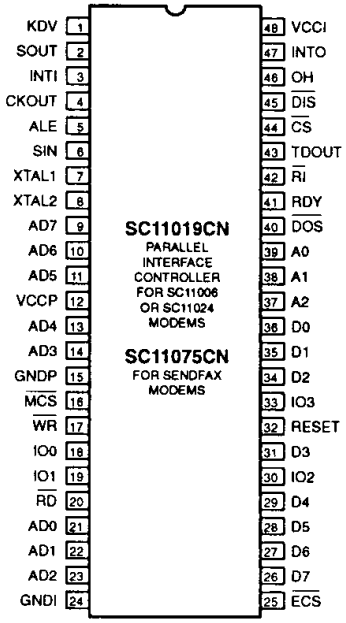
GENERAL DESCRIPTION (continued)

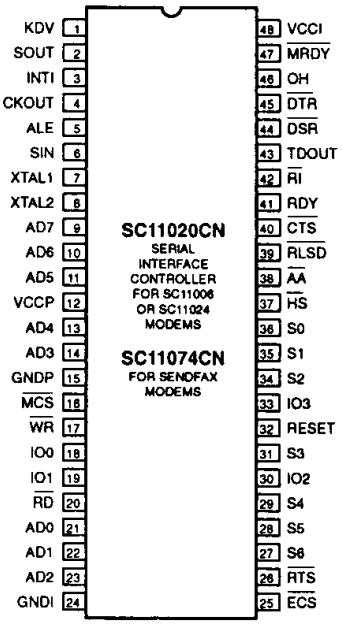
The SC11021 is the ROMless version capable of addressing 32k bytes of external memory and is available in a 68-pin PLCC package.

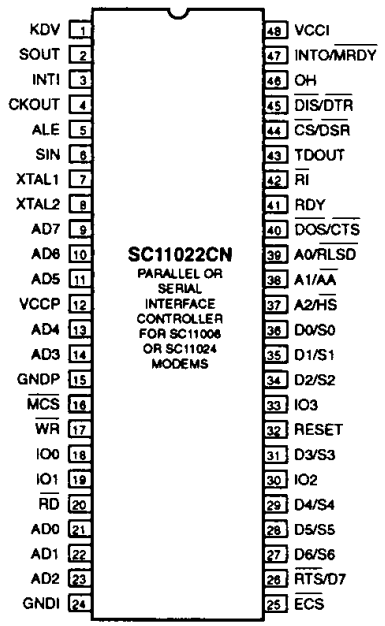
The SC11022 is the fully configurable version of both controllers and is available in 48-pin DIP and 68-pin PLCC package. The 68-pin version is capable of addressing up to 24k bytes of external memory.

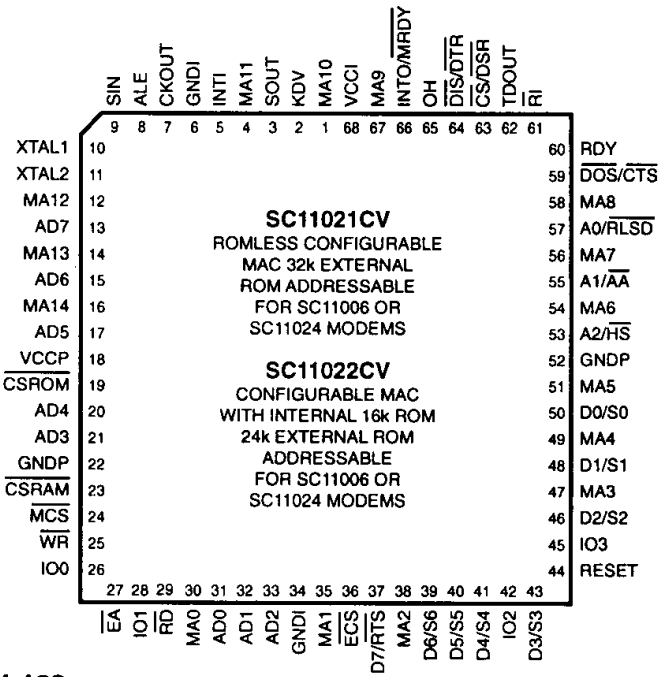
This MAC is similar to, and pin compatible with, the SC11011. The major differences are the addition of a 16k internal ROM containing all the DSP and Hayes compatible commands, plus a four bit I/O port which may be used to communicate with a low cost serial E^2 memory. The I/O port is also used to select the modem configuration—RS-232 or parallel interface, internal or external hybrid, SC11006 or SC11024 MAP. This port is not available in the 44-pin PLCC for parallel applications so these versions are factory programmed for internal hybrid. The SC11019CV is set for use with SC11006 MAP while SC11023CV is set for SC11024 MAP.

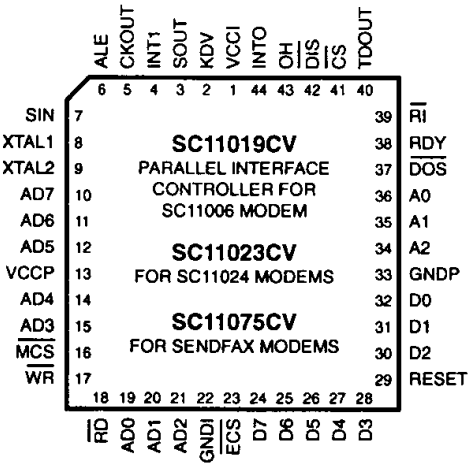
CONNECTION DIAGRAMS



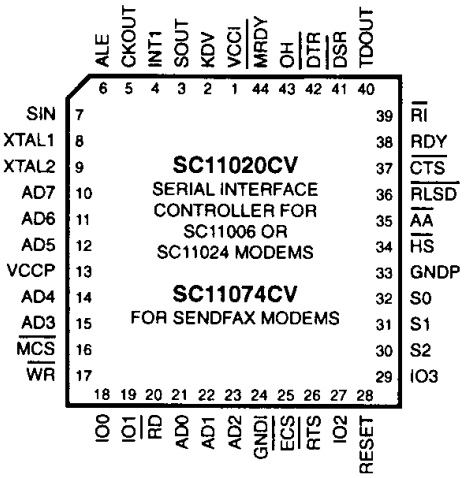


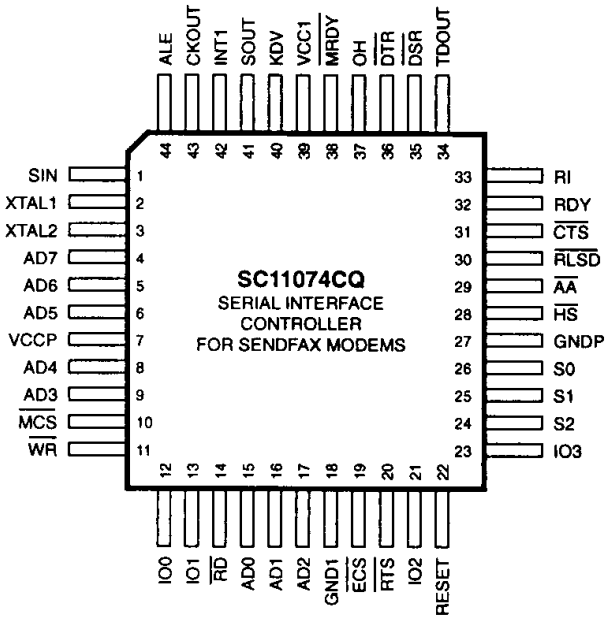


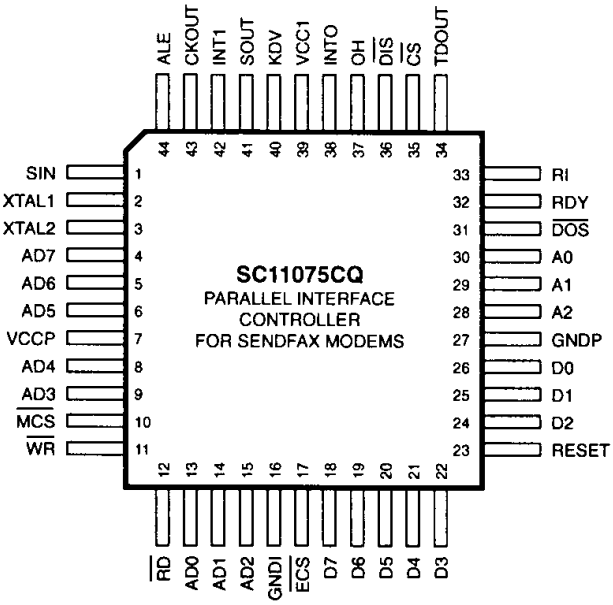




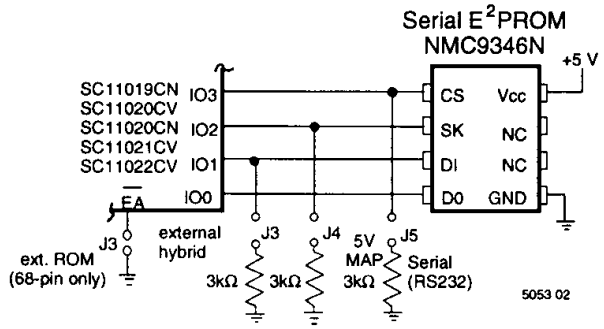
CONNECTION DIAGRAMS (continued)







CONFIGURATIONS FOR SC11019CN, 20CN, 20CV, 22CV BIG MACS



All models listed above can operate with either serial or multiplexed E²PROMs for configuration and number storage. The internal ROM program automatically determines which kind of E²PROM is connected and adapts accordingly.

Note that the SC11022 pin configuration matches that of the SC11011 controller except five new pins are used that were formerly not connected. Four of these are the I/O pins described above. One is the TDOUT pin which will be used with SC11026 for V.23 signalling.

When substituting SC11022 for SC11011 it is only necessary to open the EA pin and remove the external EPROM. Connect the jumpers as shown if required to operate with SC11024 MAP, external hybrid or in serial mode.

Three of the four I/O pins on the specified models of the internal ROMed MAC are programmed to set the configuration at power-up or reset. Internal weak pull-up re-

CONFIGURATIONS FOR SC11019CN, 20CN, 20CV, 22CV BIG MACS (continued)

sistors will set the default configuration to internal hybrid, ±5 V SC11006 MAP interface and Parallel mode if there is no external pull-down.

External pull-down resistors must be added to select other options as indicated in the table. The I/O drivers will overcome these pull-up or pull-down resistors in normal operation to operate the serial E²PROM. The I/O pins may be directly grounded if the serial E²PROM is not used. The SC11074 and SC11075 do not support E²PROM.

In the 44-pin version of SC11019, the I/O pins are not externally available. The SC11023 is internally bonded to select the 5 V only MAP (SC11024) configuration.

MAC PART NO.	PACKAGE	INT. ROM	EXT. ROM	UART MODE	MAP
SC11019CV	44-PLCC	16 k	–	Parallel	SC11006
SC11019CN	48-DIP	16 k	–	Parallel	SC11006
SC11020CV	44-PLCC	16 k	–	Serial	SC11006/24
SC11020CN	48-DIP	16 k	–	Serial	SC11006/24
SC11021CV	68-PLCC	0	32 k*	Serial/Par.	SC11006/24
SC11022CV	68-PLCC	16 k	24 k	Serial/Par.	SC11006/24
SC11022CN	48-DIP	16 k	–	Serial/Par.	SC11006/24
SC11023CV	44-PLCC	16 k	–	Parallel	SC11024
SC11074CN	44-PLCC	16 k	–	Serial	SC11044/54
SC11074CN	48-DIP	16 k	–	Serial	SC11044/54
SC11074CQ	44-QFP	16 k	–	Serial	SC11044/54
SC11075CV	44-PLCC	16 k	–	Parallel	SC11044/54
SC11075CN	48-DIP	16 k	–	Parallel	SC11044/54
SC11075CQ	44-QFP	16 k	–	Parallel	SC11044/54

INTERFACE BLOCK DIAGRAMS

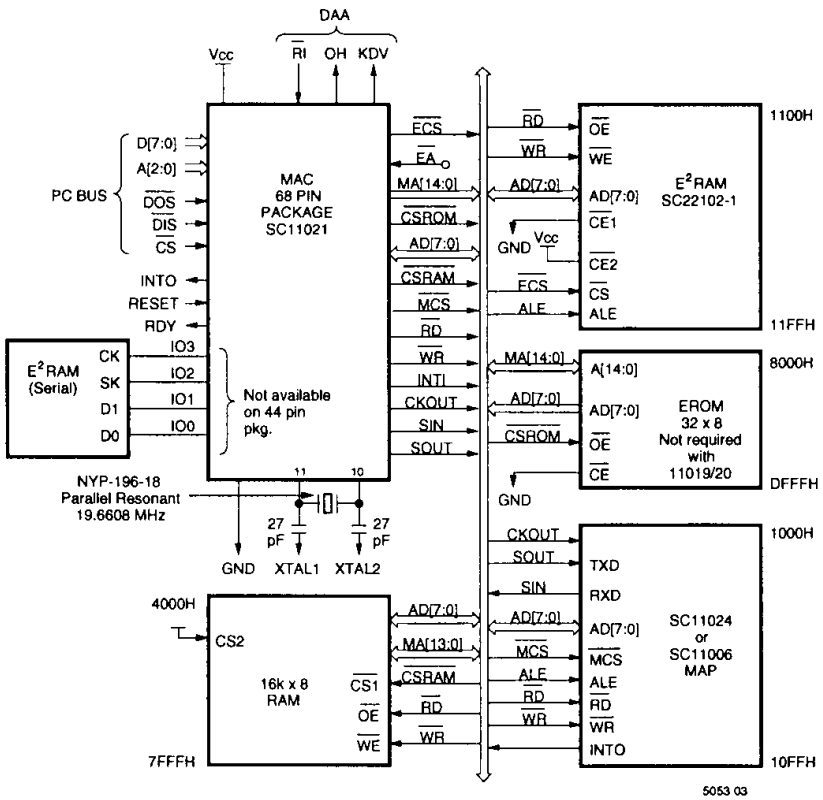


Figure 2. MAC 68 Pin Package Interfaces to E²PROM, ROM Map

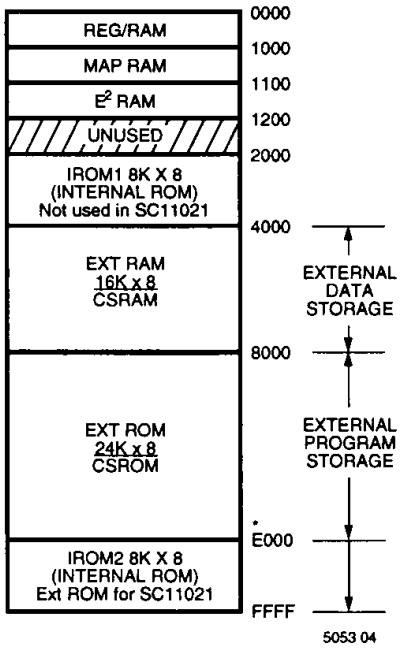


Figure 3. MAC Address Map

PIN DESCRIPTION

SC11019/21/22/23/75 Pin Description (Interfaces to Parallel System Bus)

I Parallel System Interface (to PC Bus)

$\overline{CS}$	Chip select, active low, input, TTL.
A2–A0	Address lines for UART register select, input, TTL.
INTO	Interrupt, output, CMOS/TTL, three-state. Pin is high impedance after reset.
D7–D0	8-bit data port, input-output, TTL, three-state.
$\overline{DOS}$	Data out strobe (PC writes into UART registers), active low, input, TTL.
$\overline{DIS}$	Data in strobe (PC reads from UART registers), active low, input, TTL.

II MAP Interface

AD7–AD0	8-bit bidirectional multiplexed address/data bus, CMOS.
$\overline{RD}$	RAM read, output, CMOS/TTL, normally high, data on AD7–AD0 must be valid at the rising edge of this pulse.
$\overline{WR}$	RAM write, output, CMOS/TTL, normally high, data on AD7–AD0 is valid at the rising edge of this pulse.
ALE	Address Latch Enable, output, CMOS/TTL, the address on $\overline{ECS}$, $\overline{MCS}$, AD7–AD0 are valid at the falling edge of this normally low pulse.
SOUT	Transmit data, output, CMOS/TTL. Serial data to be transmitted by the modem.
SIN	Received data, input; TTL. Serial data received from the MAP.
INTI	Interrupt input, TTL; interrupt received from the MAP at 600 Hz. Interrupt is detected when this pin has a low to high transition. The line has to stay high for at least 200 ns.
$\overline{MCS}$	Map chip select for MAP interface, output, TTL/CMOS, addressing space is from 1000H to 10FFH.
$\overline{ECS}$	External EERAM chip select or for second MAP chip select, output, TTL/CMOS, addressing space is fom 1100H to 11FFH.

III DAA Interface

$\overline{RI}$	Ring indicator, input, Schmitt, when low, indicates the modem is receiving a ringing signal.
OH	Off-hook, output, TTL/CMOS, when high, indicates the DAA should go off-hook.
KDV	Data/voice Relay Control, output, TTL/CMOS. When high, indicates the voice (telephone set) relay is closed and the modem is in the voice mode.

IV Other Pins

RESET	Master reset Schmitt input, TTL, active high. When RESET is high, MAC program counter resets to location 2000H. It resumes counting after RESET goes low.
XTAL1	Together with XTAL2 for crystal input (19.6608 MHz).
XTAL2	Crystal output pin (19.6608 MHz).
CKOUT	Clock output pin, TTL/CMOS, from MAC (9.8304 MHz, ~100 ns. cycle time).
VCCI	+5 V
GNDI	Ground
VCCP	Second Vcc pin
GNDP	Second Gnd pin
TDOUT	Output, TTL/CMOS, CCITT V.23 Transmit Data Output (General I/O Port), three-state. Controlled by General I/O Port.
PD	Power Down Output, TTl/CMOS, Low indicates power down mode. SC11074, 75 only.
RDY	Ouput, ready signal for high speed PC-AT interface.

V Extra Pins For 48 Pin Package (SC11019/21/22)

IO3–0	General I/O Port, TTL/CMOS, three-state All these pins have weak internal 30 kΩ pull-ups to Vcc.
IO0	Serial E^2PROM data out Each I/O pin can be configured as either input or output under control of GIO (page 16). The internal ROM uses these pins as follows:
IO1	Serial E^2PROM D1/External 3 kΩ pull-down selects external hybrid configuration.
IO2	Serial E^2PROM clock/External 3 kΩ pull-down selects 5 V MAP (SC11024).
1O3	Serial E^2PROM $\overline{CS}$/External 3 kΩ pull-down selects serial mode.

VI Extra Pins For 68 Pin Package Only (SC11021/22)

MA0–MA14	Output, TTL/CMOS, 15 bit address bus for external program/data access.
$\overline{CSROM}$	Output, TTL/CMOS, chip select for external ROM, address from 8000H to DFFFH.
$\overline{CSRAM}$	Output, TTL/CMOS, chip select for external RAM, address from 4000H to 7FFFH.

PIN DESCRIPTION (Cont.)

VI Extra Pins For 68 Pin Package Only (SC11021/22)

$\overline{EA}$	Input, External access enable. Low will cause the chip to jump to external vector 8000H after a 2000H reset. Also when this pin is low, the chip will use external interrupt vector. These functions are controlled by internal ROM code. $\overline{EA}$ pin has a weak internal 30 kΩ pull-up to Vcc.
GNDI	Third Gnd pin for 68 pin package.

SC11020/21/22/74 Pin Description

(Interfaces to RS-232 port)

I MAP Interface

16 pins identical to SC11019 including: AD7–AD0, $\overline{RD}$, $\overline{WR}$, ALE, SOUT, SIN, INTI, $\overline{MCS}$, $\overline{ECS}$.

II RS-232 (Data Set Mode) and Display Interface

$\overline{DTR}$	Data terminal ready, input, TTL.
$\overline{AA}$	Automatic answer enable (low), output, TTL/CMOS.
$\overline{HS}$	High speed indicator, output, TTL/CMOS. Low when operating at 2400 bps rate. High otherwise.
$\overline{MRDY}$	Modem ready.
$\overline{RLSD}$	Carrier detect, output, TTL/CMOS.
$\overline{DSR}$	Data set ready, output, TTL/CMOS.
$\overline{RTS}$	Request to send, input, TTL.
$\overline{CTS}$	Clear to send, output, TTL/CMOS.

III DAA Interface

3 pins the same as SC11019 namely: OH, RI, KDV.

IV Switch Port Pins

S0–S4	5-bit input port for sensing switch setting inputs. External pull-up resistors (10 kΩ) must be used on these inputs or they may be hard wired to +5 V if not used. See Firmware release notes for functions supported.
S0	When low, selects dumb mode. Modem will not accept commands.

V Switch Port Pins for SC11074

S0	Dumb Mode (if pulled down)
S1	Auto Answer (if pulled down)
S2	&C0 if pulled high (&C1 if pulled down)
IO1	INT/EXT Hybrid (external hybrid if pulled down)
IO2	&D2 if pulled down (&D0 if pulled high)
IO3	T.I.E.S./Hayes Escape Sequence (Hayes if pulled down)

VI Other Pins

10 pins, the same as SC11019 namely: RESET, XTAL1, XTAL2, CKOUT, VCC, GND1, VCCP, GND0, TDOUT, RDY, IO3–0.

VII Extra Pins For 48 Pin Package

S6–S8	3-bit input port for sensing switch setting inputs. External pull-up resistors (10 kΩ) must be used on these inputs or they may be hard wired to +5 V if not used. See Firmware release notes for functions supported.

VIII Extra Pins For 68 Pin Package Only

MA0–MA14	Output, TTL/CMOS, 15 bit address bus for external program/data access.
$\overline{CSROM}$	Output, TTL/CMOS, chip select for external ROM, address from 8000H to DFFFH.
$\overline{CSRAM}$	Output, TTL/CMOS, chip select for external RAM, address from 4000H to 7FFFH.
$\overline{EA}$	Input, External access enable . Low will cause the chip to jump to external vector 8000H after a 2000H reset. Also when this pin is low, the chip will use external interrupt vector. These functions are controlled by internal ROM code. $\overline{EA}$ pin has a weak internal 30 kΩ pull-up to Vcc.
GNDI	Third gnd pin for 68 pin package.

MAC Operation

The MAC is interrupted once every 1.667 ms (600 Hz). It reads two I channel samples and two Q channel samples (T/2 sampling) within 100 µs of receiving the interrupt.

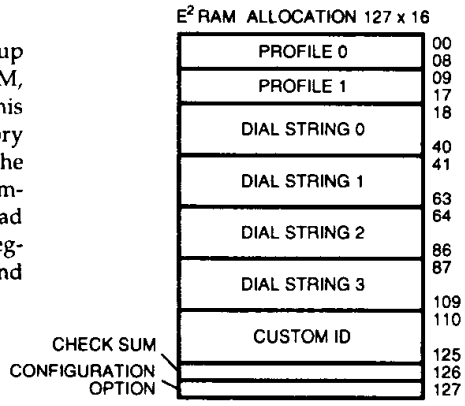
After the samples are processed a quadbit (4 bits) descrambled of data is written back to the MAP. The MAP will perform the synch to asynch conversion function, if operating in asynchronous mode, and outputs received data on SIN pin.

Manufacturer Identification

The optional external E²PROM may be used to store your manufacturer's ID in bytes 6EH thru 7DH (16 characters). This ID will be returned on command ATI3. The manufacturer's ID must be pre-written to the E²PROM. Only the phone numbers and settings are user programmable.

Dial strings are packed 5 bits per character.

Checksum is monitored at power up reset. If it does not match internal ROM, the E²RAM is assumed to be new. This causes the program to write the factory default values into the E²ROM. If the checksum matches the internal number, the configuration profile is read from the E²PROM into the modem registers before going to the command state.



SOFTWARE ARCHITECTURE

Operand Types

1. **Short Integers:** Short integers are 8-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –128 and +127 will set the overflow bit in the Program Status Byte (PSB). There are no alignment restrictions on short integers.

2. **Integers:** Integers are 16-bit signed 2's complement variables. Arithmetic operations which generate results outside the range –32768 and +32767 will set the overflow bit in the PSB. The least significant byte of the integers is in the even byte address and the next most significant byte is in the next higher (odd) address. Therefore, the integers must be aligned at even byte boundaries in the address space. The address of a word is the address of its least significant byte (always an even address).

3. **Bits:** The bits within the bytes of the register file are numbered from 0 to 7 with 0 referring to the LSB. The only instructions that use bit addressing are JBC and JBS.

4. **Long Integers:** Long integers are 32-bit signed 2's complement variables. The result of a 16 x 16-bit multiply will be stored in a long integer. Only SHRL and SHLL manipulate this data type. Long integers are addressed by the address of their least significant byte in the register file. They should be aligned such that their address is evenly divisible by 4. The most significant byte of a long integer resides on "address" +3, where "address" is the long integer's address.

Operand Addressing

Three types of addressing are allowed:

1. **Immediate Addressing:** This is a direct field within the instruction. For short integers, this is an 8-bit field, whereas, for the integers this is a 16-bit field. Only one operand within an instruction can be immediate reference type. This operand must always be the last (right most) operand within an instruction.

   e.g. ADD AX, #340H is allowed

   ADD AX, #340H, BX is NOT allowed

2. **Register Direct Addressing:** In this mode an 8-bit field is used to access a register from the 320 byte register file. The regiter address must conform to the alignment rules.

   e.g. ADD AX, BX :AX, BX must be "even" numbers

   ADDB AX, BX :AX, BX can be "odd" or "even"

3. **Indirect Addressing:** A memory location can be addressed indirectly by placing its 16-bit address in the register file. Only one operand (the right most operand) within an instruction can be indirect.

   e.g. ADDB AL, BL, [CX] is allowed

   ADDB AL, [CX], BL is NOT allowed

Program Status Byte (PSB), location 0192H

This is an 8-bit register storing the condition flags of arithmetic, shift, and compare instructions (see the following table). The programmer can access these bits by using address 0192H.

Firmware Revisions:

Firmware may be upgraded from time to time to add features and improve performance. Please call Sierra sales office for the current firmware documentation.

Program Status Byte (PSB) Location 0192H

BIT	NAME	FUNCTION
7	PD	Power-Down enable bit. Set HIGH to power-down. Set LOW to power-up. CKOUT slows down 32 times during power-down. Hardware reset on RI, DTR off ton in serial mode or RI, DIS, CS off to in parallel mode.
6	Unused	N/A
5	IP	Global interrupt pending bit. Set upon receipt of interrupt. Cleared when interrupt service begins.
4	IE	Global interrupt enable bit; when zero, all interrupts are disabled.
3	Z	Zero bit; indicates the last arithmetic or compare instruction produced a zero result.
2	N	Negative bit; indicates the last arithmetic or compare instruction produced a negative result.
1	C	Carry bit; indicates the state of the arithmetic carry from the most significant bit of the ALU for an arithmetic operation or the state of the last bit shifted out of the operand for a shift. Arithmetic "Borrow" after a subtract is the complement of the C flag (i.e. if borrow generated then C = 0).
0	V	Overflow bit; indicates the last arithmetic operation produced an overflow.

SOFTWARE ARCHITECTURE (Cont.)

Power-Down Feature

This MAC has the ability to operate in a standby or power-down mode in which the internal bus clock is divided by 32. This allows the CPU to continue to operate and monitor certain lines in readiness to resume normal operation. The process is fully automatic and transparent to the user.

When the SC11024 MAP is used with this MAC, it too is placed in the power-down mode. Together, the two chips consume typically 8.5 mA in this mode.

The MAC enters the power-down mode when the modem is off line and the DTE interface is inactive. Power-down is disabled in the test modes.

Normal operation resumes upon one or more of the following: DTR goes high (serial mode), $\overline{RI}$ goes true, SIN goes low (serial mode) or $\overline{CS}$ goes true (parallel mode). These inputs are hardwired to the power down register—bit 7 of program status byte.

(Note: Check with sales office listed for ROM code revision which supports power-down.)

Interrupt Structure

Four interrupt sources exist in the MAC, namely the external interrupt, timer interrupt, ring leading edge interrupt, and UART interrupt. The interupt service routine address is 2004H.

1) External interrupt: A low to high transition on the INTI pin initiates this interrupt.

2) Timer interrupt: Timer overflow interrupt—4.8 kHz frequency.

3) Ring leading edge: Interrupt generated by leading edge of ring input.

4) UART interrupt: Interrupt from UART.

   a) Parallel version: From UMR register. Any one of the following can generate this interrupt.

      RBR was read by external processor

      Data was transferred from THR to TSR

      LCR was changed

      MCR was changed

      DLL or DLM was changed

   b) Serial version: In this configuration the interrupt signal from 16C450 compatible UART is brought in as an interrupt source to the internal CPU.

INTERRUPT CONTROL REGISTER (ICR), location 0193H

This is an 8 bit register to enable or disable each of the four interrupt sources and to record the interrupt sources. The upper four bits are read/write registers while the lower four bits are read only registers. A read operation to the register will automatically clear the lower four bits.

BIT0: "1" indicates UART requested an interrupt.

BIT1: "1" indicates RING leading edge requested an interrupt.

BIT2: "1" indicates TIMER overflow requested an interrupt.

BIT3: "1" indicates EXTERNAL source requested an interrupt.

BIT4: "1" to enable UART interrupt.

BIT5: "1" to enable RING leading edge interrupt.

BIT6: "1" to enable TIMER overflow interrupt.

BIT7: "1" to enable EXTERNAL interrupt.

Any one of these four interrupts will drive the processor to address 2004H. From there the software can check interrupt sources and do priority control to branch to different service routines.

INSTRUCTION SET

The MAC instruction set is a subset of Intel 8096 instruction set. The object codes, formats and the flags they effect are identical to those of 8096. The differences are:

- No VT or ST flags exist in the MAC.
- Register locations in the UART section can only be accessed by using indirect addressing.
- The operands refer to one or more bytes of the register file. ROM locations can only be addressed using indirect addressing.
- If a memory location is addressed between 1000H and 11FFH, an external six clock multiplexed bus operation is initiated. The multiplexed address/data will use AD7–AD0 bus.
- When using ST or STB operations, the destinations are always considered to be indirect addresses.

  e.g. ST, AX, [BX] is allowed

  ST, AX, BX is NOT allowed

INSTRUCTION SET (Cont.)

Instruction Set Table

MNEMONIC	NO. OF OPERANDS	OPERATION	BYTES[1]	TIME[2]
ADD/ADDB	2	B ← A + B	3	10
ADD/ADDB	3	D ← A + B	4	10
AND/ANDB	2	B ← A AND B	3	10
AND/ANDB	3	D ← A AND B	4	10
CMP/CMPB	2	D – A	3	10
DJNZ	1	Decrement & JNZ	3	9/12
EXTB	1	Sign Extend Byte	2	7
JBC	0	Jump if bit clear	3	10/13
JBS	0	Jump if bit set	3	10/13
JC	0	Jump if Carry Set	2	5/8
JNC	0	Jump if no carry	2	5/8
JE	0	Jump if =	2	5/8
JNE	0	Jump if not =	2	5/8
JGT	0	Jump if >	2	5/8
JGE	0	Jump if >=	2	5/8
JLE	0	Jump if < or =	2	5/8
JLT	0	Jump if <	2	5/8
JV	0	Jump if Overflow	2	5/8
JNV	0	Jump if no overflow	2	5/8
JH	0	Jump if higher	2	5/8
JNH	0	Jump if not higher	2	5/8
LCALL	0	Long Call	3	11
LD/LDB	2	Load	3	10
MUL	3	D ← A * B	5	33
NOP	0	NO Operation	1	2
OR/ORB	2	D ← D OR A	3	10
XOR/XORB	2	D ← D XOR A	3	10
PUSHF	0	Push PSB	1	5
POPF	0	Pop PSB	1	5
RET	0	Return	1	10
SHL/SHLB	1	Shift Left	3	11 + N[3]
SHLL	1	Shift Left Long	3	15 + N[3]
SHR/SHRB	1	Shift Right	3	11 + N[3]
SHRL	1	Shift Right Long	3	15 + N[3]
SHRA	1	Arith. Right Shift	3	10 + N[3]
SHRAL	1	Arith. Right Long	3	15 + N[3]
SJMP	0	Short Jump	2	7
LJMP	0	Long Jump	3	9
ST/STB	2	Store to Memory	3	13[4]
SUB/SUBB	2	B ← B – A	3	10
SUB/SUBB	3	D ← B – A	4	10

[1]Add one for immediate words.
[2]Add 9 for indirect mode and 2 or 0 for immediate mode—see table. (Cycle times @ 100 ns)
[3]N is number of bit shifts.
[4]Indirect Mode.

HARDWARE ARCHITECTURE

The MAC device is organized with two buses that interconnect four main logic sections. The two buses are the internal data bus (DB) and address bus (Y). The four sections of the device are the internal processor, registers, memory, and dual port UART.

The two bus architecture was chosen to allow the MAC to execute the 8096 instruction set as fast or faster than the 8096 itself. The device is intended to run at 9.8304 MHz. A typical three operand instruction effectively executes in 10 clock cycles. The signed 16 x 16 multiply operation requires 34 clock cycles.

The internal data bus (DB) is the main bus of the device. It is an 8-bit bus that interconnects all four sections of the device. All intenal data travels on DB. The Y bus is a 16-bit output only bus from the internal processor that provides addresses to the memory and register sections of the device. This bus allows memory control to be resident inside the internal processor without degrading performance.

The internal processor controls MAC operations and performs all of the required computation functions. The internal processor consists of a microcontrol PLA and a 16-bit registered arithmetic/logic unit (RALU). The microcontrol PLA accepts as input 8096 instruction opcodes and generates the control sequences necessary to implement the instructions. The RALU performs instruction execution, operand address calculation, jump address calculation, program sequencing, and stack control. The program counter (PC) and stack pointer (SP) are contained within the RALU. The RALU is implemented with the 2901 silicon compiler.

The register section of the MAC includes RAM and the ports of the device. These locations are all treated as registers and may be accessed in register direct mode. Code can't be executed from registers. The UART registers are functionally, but not physically, part of the register section. The UART registers are accessed via indirect addressing mode only. There are 320 bytes of RAM to support DSP functions and the Hayes Smartmodem command set. The memory section of the MAC includes the program ROM and the external memory interface. The device contains 16K bytes of program ROM. The external memory interface allows the MAC to access program storage or data storage from external memory.

The UART section of the device implements the industry standard 16C450 UART. In its parallel version the MAC appears as a 16C450 to the user. The UART contains dual-port capability to allow the user and the internal processor access to its internal registers.

MEMORY DESCRIPTION

Internal ROM:

The 16K bytes of internal ROM is organized into 2 separate blocks of 8K bytes each: IROM1 and IROM2.

The SC11019/20/21/22/23 controllers are built with the same architecture as the SC11011 so that firmware will be upward compatible.

External Read/Write:

Three different types of external memory operations are defined.

A) For address from 1000H to 11FFH:

These external operations occur through the AD bus. These operations take six clock cycles, four more than internal operations. These are mainly for MAP & EEROM interfaces, however, instructions and data can also be fetched from these memory spaces.

B) For address from 4000H to 7FFFH: 68 pin only.

These memory spaces are reserved for external DATA storage. The MAC can access external RAM through MA address bus and AD data bus. There are six clock memory cycles for each access.

C) For address from 8000H to FFFFH: 68 pin only.

For 68 pin package the chip fetches instructions from external program storage by MA0–MA14 and AD0–AD7. These operations are exactly the same as internal ROM fetch and they take 2 clock cycles. For the SC11021 ROMless version, the 8k bytes from E000H to FFFFH are also mapped for external access.

Memory Address MAP

NAME	ABV	ADDRESS	R/W	SIZE (bytes)
INTERNAL RAM/REG	RAM*	0000H–013FH	R/W	320
	REG*	0180H–0193H	R/W	19 registers
EXTERNAL MAP/EERAM	MAP	1000H–10FFH	R/W	256
	EERAM	1100H–11FFH	R/W	256
INTERNAL ROM***	IROM1	2000–3FFFH	RO	8K
	IROM2	E000H–FFFFH	RO	8K
EXTERNAL RAM**	RAM	4000H–7FFFH	R/W	16K
EXTERNAL ROM**	ROM	8000H–DFFFH	RO	24K

* These may only be accessed as memory locations (16-bit address) in an indirect mode. For direct addressing a 9th bit (GCR [1], called Page Bit) must be set to switch from the first 256 bytes to the rest of the RAM.

** For 68 pin package only. Memory address has 15 bits (MA14–MA0); 16th bit is accessed through $\overline{\text{CSROM}}$ and $\overline{\text{CSRAM}}$.

*** The ROMless SC11021 uses external ROM E000H–DFFFH for a total 32 kbytes. Also, the SC11022CV when used with external ROM disables the upper 8k internal ROM and addresses 32k external (Eng. version uses only 24k).

REGISTER DESCRIPTION

This section contains a description of each of the registers in the MAC device. All of the registers of the device are 8-bits with 16-bit addresses. The registers are made up of bits that are either inputs or outputs. Input bits are read-only (RO). Output bits are read/write (R/W). The state of an output may be read back by the processor.

Test Mode:

RAM locations 00H and 100H are reserved for test mode. User access is prohibited.

Serial Mode:

In parallel mode (CONF = 0) the functions of the UART registers are exactly the same as those in 16C450 UART. However in serial mode, (CONF = 1), the UART is turned around and controlled by the internal processor and it becomes a data set UART. The DTR, RTS, and OUT1 in MCR register becomes DSR, CTS, and RLSD outputs. The CTS, DSR in MSR register become RTS, DTR input status from $\overline{RTS}$, $\overline{DTR}$ pins.

Note:

In serial version to echo SIN to SOUT after RESET and then go back to normal operation.

1) Set "SB" in LCR to "1".
2) Sample RDI in UART monitor register.
3) Set CM = $\overline{RDI}$ in the same register.
4) SOUT will be the same state as $\overline{CM}$.
5) Receiver is functioning, ignoring it.
6) After finishing all echoing, reset "SB" in LCR.
7) Update DLL, DLM, and set CM = 1 for normal operation.
8) Do a SET then RESET to RTRST bit to RESET RCV and TMR. Do a READ to LSR to clear LSR.
9) The UART is ready for normal operaton.

Register Address MAP

NAME	ABV	INTERNAL[3]			EXTERNAL[6]	
		INDIRECT ADDRESS[4]	DIRECT ADDRESS[5]	R/W	ADDRESS A [2:0]	R/W
UART Registers:						
Receive Buffer[1]	RBR	80H	180H	R/W	00H	RO
Transmit Holding[1]	THR	8AH	18AH	R/W	00H	WO
Interrupt Enable[1]	IER	81H	181H	R/W	01H	R/W
Interrupt ID	IIR	82H	182H	RO	02H	RO
Line Control	LCR	83H	183H	R/W	03H	R/W
Modem Control	MCR	84H	184H	R/W	04H	R/W
Line Status	LSR	85H	185H	R/W	05H	R/W
Modem Status	MSR	86H	186H	R/W	06H	R/W
Scratch Pad (8 bit)	STR	87H	187H	R/W	07H	R/W
Divisor Latch LSB[2]	DLL	88H	188H	R/W	00H	R/W
Divisor Latch MSB[2]	DLM	89H	189H	R/W	01H	R/W
UART Monitor	UMR	8BH	18BH	R/W		
Internal Registers:						
Switch Port	SWP	8DH	18DH	RO		
General I/O Port						
Direction Register	DIR	8EH	18EH	WO		
Data Register	DAR	8FH	18FH	R/W		
General Control	GCR	90H	190H	R/W		
TIMER	TIM	91H	191H	R/W		
Processor Status Byte	PSB	92H	192H	R/W		
Interrupt Control	ICR	93H	193H	R/W		

[1] DLAB bit (LCR [7]) must be zero for external access.
[2] DLAB bit (LCR [7]) must be one for external access.
[3] Register access through MA bus.
[4] 8-bit addresses for indirect addressing only, with Page bit (GCR [1]) used.
[5] 16-bit addresses for direct addressing only.
[6] UART register access through PC parallel system bus.

ACCESSIBLE REGISTERS

The system programmer may access or control any of the UART registers summarized in Table 1 via the CPU. These registers are used to control UART operations and to transmit and receive data. Their reset functions are summarized in Table 2.

Line Control Register (LCR, location 183H)

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in Table 1 and are described in the following.

Table 1: Summary of Accessible Registers

	Register Address										
	0(DLAB=0)	0(DLAB=0)	(DLAB=0)	2	3	4	5	6	7	(DLAB=1)	(DLAB=1)
Bit No	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Iden. Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Scratch Register	Divisor Latch (LS)	Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	STR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OE)	Delta Data Set Ready (DDSR)	Bit 1	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSi)	0	Parity Enable (PEN)	Out 2 INT0 is High-Z when out2=0	Framing Error (FE)	Delta Data Carrier Detect (DDCD)	Bit 3	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register (THRE)	Data Set Ready (DSR)	Bit 5	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Empty (TEMT)	Ring Indicator (RI)	Bit 6	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Data Carrier Detect (DCD)	Bit 7	Bit 7	Bit 15

*Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted character. If bit 2 is a logic 0, one Stop bit is generated in the transmitted data. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, one and a half Stop bits are generated. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, two Stop bits are generated. The Receiver checks the first Stop-bit only, regardless of the number of Stop bits selected.

Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of logic 1s is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bits 3, 4 and 5 are logic 1 the Parity bit is transmitted and checked by the receiver as a logic 0. If bits 3 and 5 are 1 and bit 4 is a logic 0, then the Parity bit is transmitted as a 1.

Table 2. Summary of Accessible Registers

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0–3) forced and 4–7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low, Bit 3–7 are permanently Low
Line Control Register	Master Reset	All Bits Low
Modem Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	"All Bits Low, Except Bits 5 and 6 are High"
MODEM Status Register	Master Reset	"Bits 0–3 Low, Bits 4–7—Input Signal"
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read BRR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read RBR/MR	Low

Bit 6: This bit is the Break Control bit. When it is set to a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state. The break is disabled by setting bit 6 to a logic 0. The Break Control bit acts only on SOUT and has not effect on the transmitter logic.

Note: This feature enables the CPU to alert a terminal in a computer communications system. If the following sequence is followed, no erroneous or extraneous characters will be transmitted because of the break.

1. Load an all 0s, pad character, in response to THRE.
2. Set break after the next THRE.
3. Wait for the transmitter to be idle, (TEMT=1), and clear break when normal transmission has to be restored.

During the break, the Transmitter can be used as a character timer to accurately establish the break duration.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

Programmable Baud Generator

The UART contains a programmable Baud Generator that takes an internal clock of (3/32)(XTAL1) = 1.8432 MHz and divides it by any divisor from 1 to (2^{16}–1). The output frequency of the Baud Generator is 16 x the Baud [(divisor # = (frequency input) + (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to ensure desired operation of the Baud Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on the initial load.

Table 3 illustrates the used of the

Baud Generator with a crystal frequency of 19.6608 MHz. The accuracy of the desired baud rate is dependent on the crystal accuracy. Communicaiton software writing values to the divisor latches typically expects the input to the UART to be 1.8432 MHz. They will work correctly only if the MAC input clock is maintained at 19.6608 MHz.

Line Status Register (LSR, location 185H)

Desired Baud Rate	Divisor Used to Generate 16 x Clock	Error Between Desired and Actual
50	2304	—
75	1536	—
110	1047	0.026
134.4	857	0.058
150	768	—
300	384	—
600	192	—
1200	96	—
1800	64	—
2000	58	0.69
2400	48	—
3600	32	—
4800	24	—
7200	16	—
9600	12	—
19200	6	—
38400	3	—
57600	2	—

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in Table 1 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 is reset to a logic 0 by reading the data in the Receiver Buffer Register.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits). The BI indicator is reset whenever the CPU reads the contents of the Line Status indicator.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: The bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the ACE is ready to accept a new character for transmission. In addition, this bit causes the UART to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Empty (TEMT) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Holding Register (THR) and the Transmitter Shift Register (TSR) are both empty. It is reset to a logic 0 whenever either the THR or TSR contains a data character.

Bit 7: This bit is permanently set to logic 0.

Note: The Line Status Register is intended for read operations only. Writing to this register is not recommended as this operation is used for factory testing.

Interrupt Identification Register (IIR, location 182H)

The UART has on-chip interrupt capability that allows for flexibility in interfacing popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the UART prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (IIR). When addressed during chip-select time, the IIR freezes the highest priority interrupt pending

and no other interrupts change the IIR, even though they are recorded, until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in Table 1 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in Table 4.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Interrupt Enable Register (IER, location 181H)

The 8-bit register enables the four types of interrupts of the UART to separately activate the chip interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in Table 1 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

Modem Control Register

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in Table 1 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Interrupt Identification Register				Interrupt Set and Reset Functions		
Bit 2	**Bit 1**	**Bit 0**	**Priority Level**	**Interrupt Type**	**Interrupt Source**	**Interrupt Reset Control**
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Receiver Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (If source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Bit 2: Out1. Auxiliary user-designated bit. It is connected to MSR[6] (RI) during local loopback.

Bit 3: Out 2. Auxiliary user-designated bit. It is connect to MSR[7] (DCD) during local loopback. When Out2 = 0, INTO pin is Hi-Z.

Bit 4: This bit provides a local loopback feature for diagnostic testing of the UART. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input: the four MODEM. Status Register bits CTS, DSR, DCD and RI are disconnected internally; and the four MODEM Control Register bits DTR, RTS, OUT1 and OUT2 are internally connected to the four MODEM Status Register inputs, and the MODEM Control output pins $\overline{RLSD}$, $\overline{CTS}$, $\overline{DSR}$ are forced to their inactive state (high). In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit and received-data paths of the UART.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational, but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5–7: These bits are permanently set to logic 0.

Modem Status Register (MSR, location 186H)

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU in addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in Table 1 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Read (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from a low to a high state.

Bit 3: This is the Delta Data Carrier Detect (DDCD) indicator. Bit 3 indicates that the $\overline{DCD}$ input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status Interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent of DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: this bit is the complement of the Data Carrier Detect ($\overline{DCD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

Scratchpad Register (STR, location 187H)

This 8-bit Read/Write Register does not control the ACE in any way. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

REGISTER DESCRIPTION (Cont.)

UART Monitor (UMR, location 18BH):

The UART Monitor register allows the processor to monitor UART operations. A read operation to the UART Monitor register will clear Bit 0 to Bit 4.

BIT	NAME	DESCRIPTION
7	RTRST	Reset receiver and transmitter. When set high both receiver and transmitter will be put into reset state.
6	CM	UART Command/Modem Output. When set HIGH the UART is placed in modem mode. At reset it is low, in command mode. This bit together with SB in LCR are used for bit by bit echoing. In serial version the user can set SB = 1 and CM = $\overline{RDI}$ to echo a bit. When CONF = 1 for normal operation set CM = 1.
5	RDI	Receive Data Input. This bit monitors the RXD input of the UART.
4	DLF	Divisor Latch Flag. This bit indicates if a new baud rate count has been written to the Divisor Latch.
3	LCF	Line Control Flag. This bit indicates if the line control register has been written.
2	TXF	Transmit Buffer Full Flag. This bit indicates if a new character is in the transmit shadow register.
1	RXF	Receive Buffer Empty Flag. This bit indicates if the last character has been read from the receive buffer.
0	MCF	Modem Control Flag. This bit indicates if the modem control register has been written.

Internal Registers:

Switch Port (SWP, location 18DH): for serial version only

The Switch Port is a 7-bit input port used only in the serial version of the MAC. It allows for reading of the external switches of a stand-alone modem. Only S0–S2 are available on the 44 pin SC11020CV.

BIT	NAME	DESCRIPTION
6–0	S 6–0	Switch Input. These bits monitor external switches.

General I/O Port (GIO)

Direction Register (DIR, location 018EH):

BIT	NAME	DESCRIPTION
7	Unused	N/A
6	Unused	N/A
5	Unused	N/A
4	Unused	N/A
3	DIR3	When HIGH, IO3 is an output. When LOW, IO3 is an input.
2	DIR2	When HIGH, IO2 is an output. When LOW, IO2 is an input.
1	DIR1	When HIGH, IO1 is an output. When LOW, IO1 is an input.
0	DIR0	When HIGH, IO0 is an output. When LOW, IO0 is an input.

REGISTER DESCRIPTION

General I/O Port (GIO) (Cont.)

Data Register (DAR, location 018FH):

BIT	NAME	DESCRIPTION
7	Unused	N/A
6	Unused	N/A
5	DAR5	This bit is routed to TDOUT pin when DAR4 is set HIGH.
4	DAR4	When set HIGH, DAR5 is output to TDOUT pin. When set LOW, SOUT or SIN is output to TDOUT pin when GCR bit 7 (CONF) is set LOW or HIGH respectively. See Figure 11.
3–0	DAR3–0	Output to IO3–0.

Timer (TIM, location 191H):

The Timer includes an 11 bit counter and a timer flip-flop. It is used to aid software timing functions. The counter is not readable. It can only be reset by a write. The timer flip-flop can be read to test if it is already set.

The counter and flip-flop will be reset on a write (value is don't care). After that the counter sends out a pulse train at 4.8 kHz rate to set the timer flip-flop. The flip-flop can be cleared on a read. The Timer is constantly counting by the internal clock CP (9.8304 MHz).

BIT	NAME	DESCRIPTION
0	TFF0	Timer flip-flop bit.

General Control Register (GCR, location 0190H):

GCR contains a miscellaneous set of control and status bits.

BIT	NAME	DESCRIPTION
7	CONF	Configuration output. This bit controls the state of the MAC configuration. When HIGH, the MAC is configured with the SERIAL interface. It is configured with the PARALLEL interface after a reset.
6	OH	Off Hook Output. When set HIGH, the phone will be placed off hook.
5	KDV	KDV Output. Data/Voice Relay Control. When high, the modem is in the voice mode.
4	MRDY	Modem ready.
3	AA	Active HIGH AA indicator. When high this bit sets the $\overline{AA}$ pin low.
2	HS	Active HIGH HS indicator. When high this bit sets the $\overline{HS}$ pin low.
1	PAGE	Register Page Bit. This bit selects the active register page. When LOW, the lower 256 registers are accessed during register operations and when HIGH, the upper page is active.
0	EA	Inverted external access enable status from $\overline{EA}$ pin. When on it is high. Low indicates $\overline{EA}$ is off.

COMMAND SUMMARY

Configuration & Async/Sync Commands

General:

COMMAND		DESCRIPTION
B	1	BELL/CCITT Protocol
E	1	Command Echo
L	2	Speaker Volume
M	1	Speaker Control
Qn	0	Quiet Command Reset Code
Sn=		Writing to S-Register
Sn?		Reading S-Registers
V	1	Enable Short-form Result Codes
X	4	Enable Extended Result Code Set
&J[1]		Telephone Jack Sel.*
&M[1]		Async/Sync Mode Sel.

Async/Sync Commands—International:

&G	0	Guard Tone Sel.
&P	0	Make/Break Dial Pulse Ratio Sel.

Async-Only Commands:

Y[1]	0	Enable Long Space Disconnect
&C	0	Data-Carrier-Detect (DCD) Options
&D	0	Data-Terminal-Ready (DTR) Options
&S	0	Data-Set-Ready (DSR) Options

Sync-Only Commands:

&R	0	Clear-to-Send (CTS)/Request-to-Send (RTS)
&X	0	Select Sync Transmit Clock Source

* See Figure 10 for Hardware Implementation.

All commands are compliant with Hayes 1988 AT commands. A detailed command set document is available on request. Check our bulletin board – (408) 263-8294.

[1] Not supported in SC11074,75 Sendfax controllers

COMMAND	DESCRIPTION

Immediate Action Commands:

A	Go OFF-Hook in Answer Mode
A/	Re-Execute Last Command
D	Dial Telephone Number
Hn	Switch Hook Control
O	Return to On-Line
Z[1]	Fetch Configuraton Profile from Nonvolatile Memory
&F	Fetch Factory Configuration Profile
&W[1]	Write Active Configuration Profile to Nonvolatile Memory
&Z[1]	Store Telephone Number

Dial Modifiers:

P	Pulse Dial
T	Touch-Tone Dial
R	Originate Call in Answer Mode
W	Wait for Dial Tone B/4 Continue to Dial
,	Delay a Dial Sequence
@	Wait for Quiet Answer B/4 Continue to Dial
!	Initiate a Flash
;	Return to Command State after Dialing
S=n	Dial A Stored Number (n=0 to 3)

Self Test and Diagnostics:

I/IO	Request Prod Code
I1/I2	ROM Checksum
I3	Manufacturer's I.D.
I4	Configuration Mode (Serial or Parallel)
I5	Fax Chip I.D. (11074,5 only)
&T[1]	Test Modes
I33	Sierra I.D.
RV[1]	Display Profiles & Register Settings

COMMAND SUMMARY (continued)

Sendfax Command Set Summary

COMMAND	DESCRIPTION

Sendfax:

#Bn	Speed Control n = 0 Reserved n = 1 Reserved n = 2 Reserved for V.23 n = 3 Reserved for V.23 n = 4 Fax Transmission Speed of 2400 bps n = 5 Fax Transmission Speed of 4800 bps n = 6 Fax Transmission Speed of 7200 bps n = 7 Fax Transmission Speed of 9600 bps
#En	Received frame Display Format Selection n = 0 Disable Display of Received HLDC Frames n = 1 Display Frame in Binary Format n = 2 Display Frame in 2 Digit ASCII Hex Format
#Fn	Mode Control n = 0 Return to Normal Modem Mode (300 to 2400 bps Data Rate) n = 1 Enter Fax Mode (19,200 bps Data Rate)
#Kn	DTE Flow Control n = 0 Disable Flow Control n = 3 Enable CTS Flow Control n = 4 Enable XON/XOFF Flow Control
#Pn	Number of Pages to Be Transmitted (n = 1 to 255)
#Rn	Resolution Control n = 0 Send Document with Normal Resolution n = 1 Send Document with Fine Resolution

Detailed current documentation on the command set is available from Sierra on request and may be downloaded from our bulletin board at (408) 263-8294,

Extensions to the Hayes AT command set for Sendfax mode operation are outline in this section. In order to accomodate these added commands in the 16K ROM space avilable, we eliminated some of the rarely used Hayes commands as indicated on the previous page.

General

1. All extended Sendfax commands start with the AT# prefix. This provides upward compatibility with future EIA command sets which will use the + symbol.

2. Fax mode assumes XON/XOFF or CTS flow control in data mode. &D2 command must be issued for DTR controlled abort.

3. Once the hardware enters the Fax mode, it will remain in the Fax mode (and accept commands at 19.2 kbps) until one of the following occurs:

a) software issues a #F request to return to command mode

b) a call disconnect frame is received

c) application software issues an abort command by dropping DTR

During the Fax session the hardware will report the status of the call with result codes. An action by the software may or may not be necessary depending on the response. All the normal Hayes result codes will also be reported.

Verbose	Digit	Usage
CED	a	Answertone detected
CFR	g	Remote machine confirmation to receive
CONNECT2400/FAX	w	Connection speed 2400 bps
CONNECT4800/FAX	x	Connection speed 4800 bps
CONNECT7200/FAX	y	Connection speed 7200 bps
CONNECT9600/FAX	z	Connection speed 9600 bps
CRC ERROR	e	Error in received frame
CRP	c	Repeat request
CSI	-	Remote machine identification
DCN	d	Disconnect
DIS	b	Remote machine capabilities frame
FTT	f	Failure to train
INVALID FRAME	i	Received frame is invalid
MCF	m	Message received OK
RTN	h	Message not received OK
RTP	j	Retrain positive

SC11019/SC11020/SC11021 SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS:

V_{CC} Supply Voltage	+6 V
Input Voltage	–0.6 V to V_{CC} +0.6 V
Storage Temperature Range	–65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature Range	0 to 70°C

DC ELECTRICAL CHARACTERISTICS: (T_A = 0 TO 70°C, V_{CC} = +5 V +10%)

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNITS
V_{CC}	Positive Supply Voltage	4.5	5.0	5.5	V
I_{CC}	Nominal Operating Current @ V_{CC} = 5.5 V		40	75	mA
I_{CCPD}	Power Down Current @ V_{CC} = 5.5 V		8	15	mA
V_{IH}	High Level Input Voltage for TTL input pins for CMOS input pins	 2 0.8 V_{CC}			 V V
V_{IL}	Low Level Input Voltage for TTL input pins for CMOS input pins			 0.8 0.2 V_{CC}	 V V
VT+	Positive Hysteresis Threshold for RESET & /RI input pins		2.5		V
VT–	Negative Hysteresis Threshold for RESET & /RI input pins		1.8		V
V_{OH}	High Level Output Voltage for D7–D0, into @ I_{OH} = 8 mA for RDY—open collector for other output @ I_{OH} = 2 mA	 0.7 V_{CC} +0.5			 V
V_{OL}	Low Level Output Voltage for D7–D0, into pins @ I_{OL} = 8 mA for RDY @ I_{OL} = 8 mA for other output pins @ I_{OL} = 2 mA			 0.3 V_{CC} –0.5	 V
I_1	Leakage Current		±1	±20	µA
F_{CLK}	Crystal Clock Frequency		19.6608		MHz

TIMING DIAGRAMS

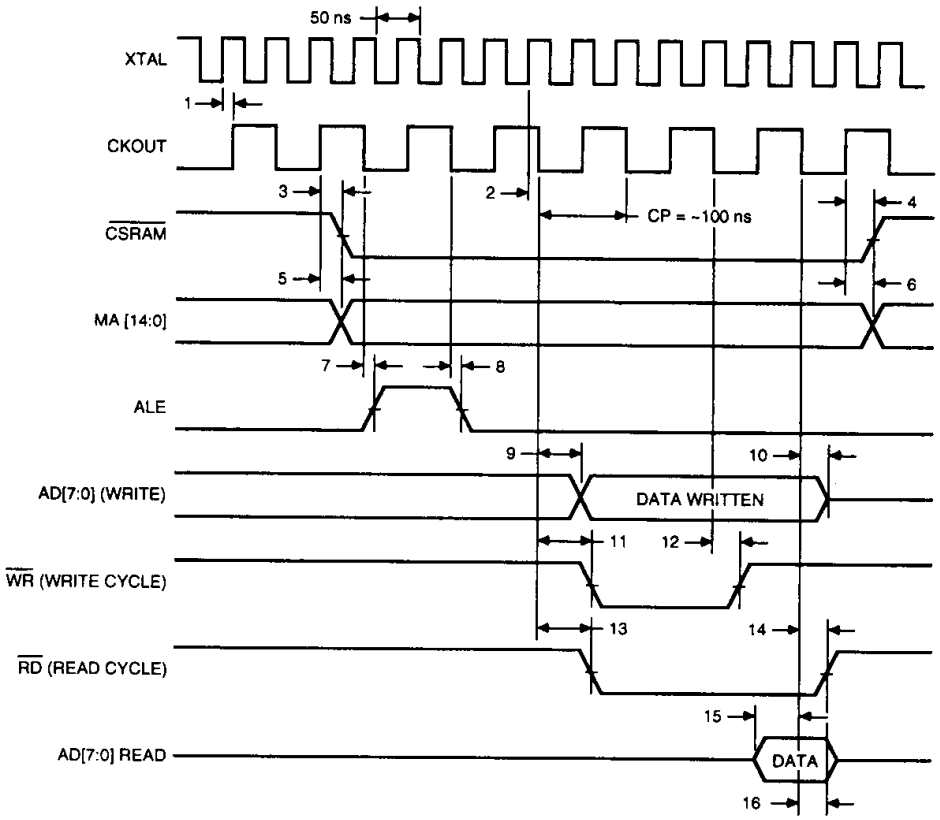


Figure 4. RAM Read or Write Cycle

RAM Read or Write Cycle Timing Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TXTHCH	XTAL high to CKOUT high				45	ns
2	TXTHCL	XTAL high to CKOUT low				45	ns
3	TCHCSL	CKOUT high to $\overline{\text{CSRAM}}$ low				25	ns
4	TCHCSH	CKOUT high to $\overline{\text{CSRAM}}$ high				25	ns
5	TCHMAV	CKOUT high to MA valid				25	ns
6	TCHMAI	CKOUT high to MA invalid				25	ns
7	TCLALH	CKOUT low to ALE high				15	ns
8	TCLALL	CKOUT low to ALE low				15	ns
9	TCLADV	CKOUT low to AD valid				35	ns
10	TCLADI	CKOUT low to AD invalid		5			ns
11	TCLWRL	CKOUT low to $\overline{\text{WR}}$ low				25	ns
12	TCLWRH	CKOUT low to $\overline{\text{WR}}$ high				25	ns
13	TCLRDL	CKOUT low to $\overline{\text{RD}}$ low				15	ns
14	TCLRDH	CKOUT low to $\overline{\text{RD}}$ high				15	ns
15	TADVCL	AD valid to CKOUT low (Read Set-up Time)		50			ns
16	TCLADI	CKOUT low to AD invalid (Read Hold Time)		0			ns

TIMING DIAGRAMS (Cont.)

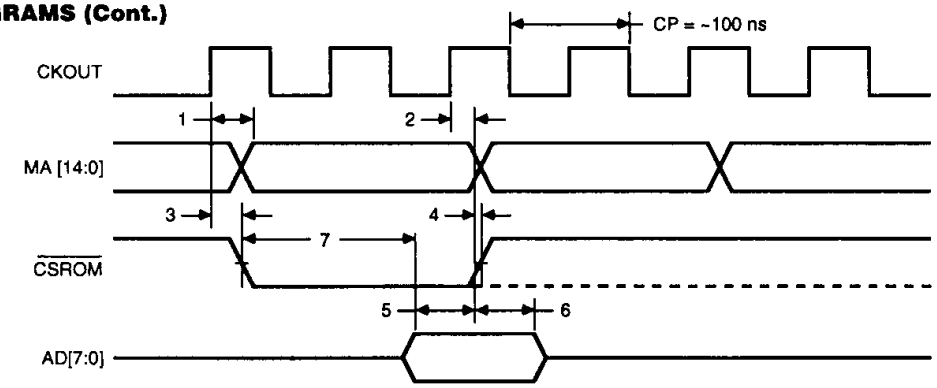


Figure 5. External Program Storage Read Bus Cycle

External Program Storage Read Bus Cycle Table

NO.	SYMBOL	PARAMETER	TEST COMMENTS	MIN	TYP	MAX	UNITS
1	TCHMAV	CKOUT high to MA valid				15	ns
2	TCHMAI	CKOUT high to MA invalid				15	ns
3	TCHCSL	CKOUT high to $\overline{\text{CSROM}}$ low	$\overline{\text{CSROM}}$ may already be low			15	ns
4	TCHCSH	CKOUT high to $\overline{\text{CSROM}}$ high	$\overline{\text{CSROM}}$ may not go high			15	ns
5	TADVCH	AD valid to CKOUT high		35			ns
6	TCHADZ	CKOUT high to AD high-Z		0			ns
7	TADRDA	$\overline{\text{RD}}$ valid to data valid				170	ns

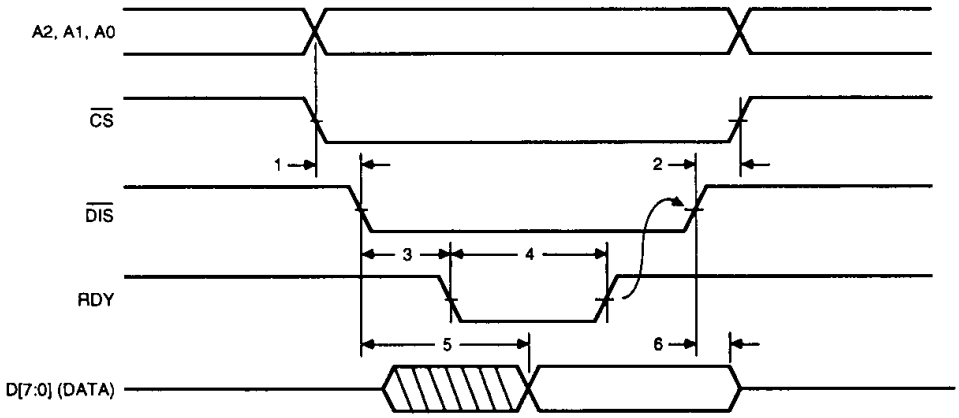


Figure 6. Read Cycle (PC Bus Read From UART Register)

Read Cycle (PC Bus Read From UART Register) Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDIL	$\overline{\text{CS}}$ low to $\overline{\text{DIS}}$ low				0	ns
2	TDIHCSH	$\overline{\text{DIS}}$ high to $\overline{\text{CS}}$ high				0	ns
3	TDILRDL	$\overline{\text{DIS}}$ low to RDY low				30	ns
4	TRDL	RDY low time (~5–6CP)		500		600	ns
5	TDILDV	$\overline{\text{DIS}}$ low to D valid				250	ns
6	TDIHDZ	$\overline{\text{DIS}}$ high to D high-Z				15	ns

TIMING DIAGRAMS (Cont.)

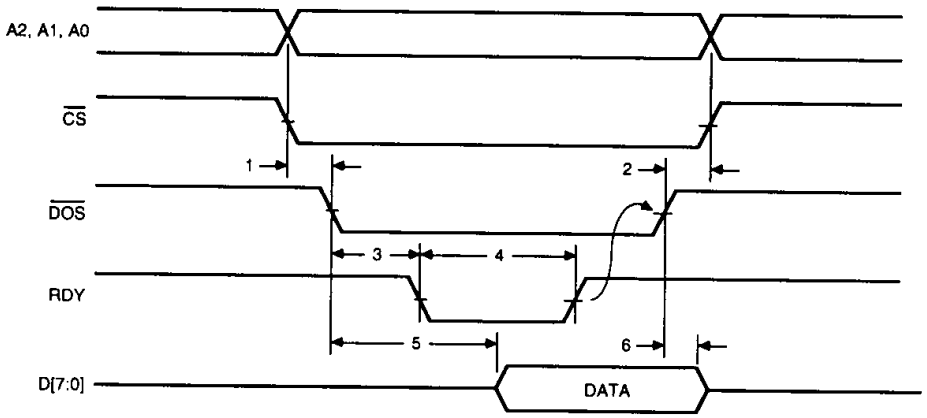


Figure 7. Write Cycle (PC Bus Write Into UART Register)

Write Cycle (PC Bus Write Into UART Register) Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TCSLDOL	$\overline{CS}$ low to $\overline{DOS}$ low				0	ns
2	TDOHCSH	$\overline{DOS}$ high to $\overline{CS}$ high				0	ns
3	TDOLRDL	$\overline{DOS}$ low to RDY low				30	ns
4	TRDL	RDY low time (~5–6CP)		500		600	ns
5	TDOLDV	$\overline{DOS}$ low to D valid				260	ns
6	TDOHDZ	$\overline{DOS}$ high to D high-Z		0			ns

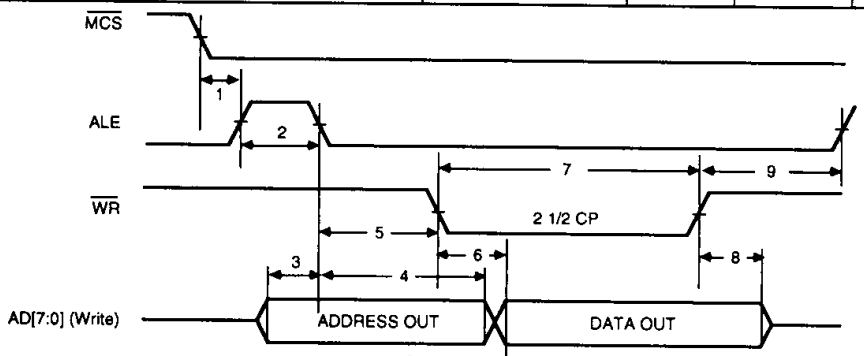


Figure 8. MAP and E^2 RAM Interface Write Cycle

MAP and E^2 RAM Interface Write Cycle Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TMCAL	$\overline{MCS}$ low to ALE high		10		20	ns
2	TALE	ALE pulse width		45			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		48			ns
5	TALRD	Delay from ALE low to $\overline{WR}$ low		45			ns
6	TDVRL	Data valid after $\overline{WR}$ low				25	ns
7	TWR	Write pulse width		230			ns
8	TDHWR	Data hold after $\overline{WR}$ high		30			ns
9	TWHLH	End of $\overline{WR}$ to next ALE		200			ns

When the SC11011 is reading or writing to the MAP, the address is valid at least 30 ns before ALE goes low and stays valid 48 ns or more beyond the trailing edge of ALE. When writing, data id valid within 25 sn afte WRn goes true and stays valid i=until at least 30 ns after WRn goes false

TIMING DIAGRAMS (Cont.)

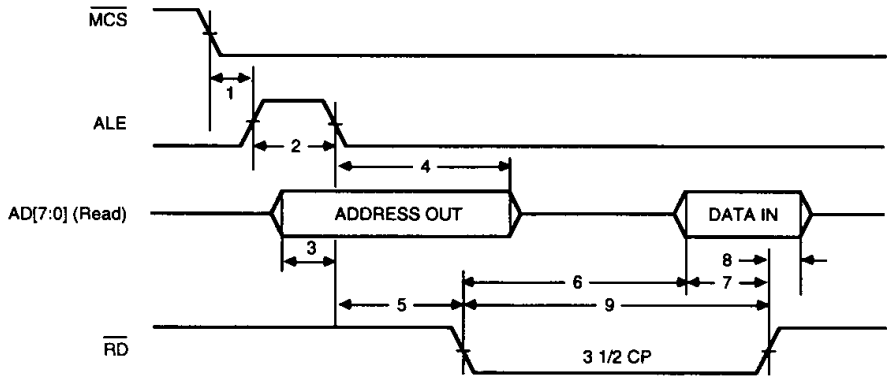


Figure 9. MAP and E²RAM Interface Read Cycle

MAP and E²RAM Interface Read Cycle Table

NO.	SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNITS
1	TMCAL	$\overline{MCS}$ low to ALE high		10		20	ns
2	TALE	ALE pulse width		45			ns
3	TAVLE	Address valid to ALE low		30			ns
4	THAD	Hold address after ALE low		48			ns
5	TALRD	Delay from ALE low to $\overline{RD}/\overline{WR}$ low		45			ns
6	TDVRL	Data valid after RD low				300	ns
7	TDVRH	Data valid setup to $\overline{RD}$ high		15			ns
8	TDH	Data hold after $\overline{RD}$ high		0			ns
9	TRD	Read pulse width		330		370	ns

When reading from the MAP, data must be valid a maximum of 300ns after $\overline{RD}$ goes true and stays valid at least until 0ns after $\overline{RD}$ goes false.

CIRCUIT DIAGRAMS

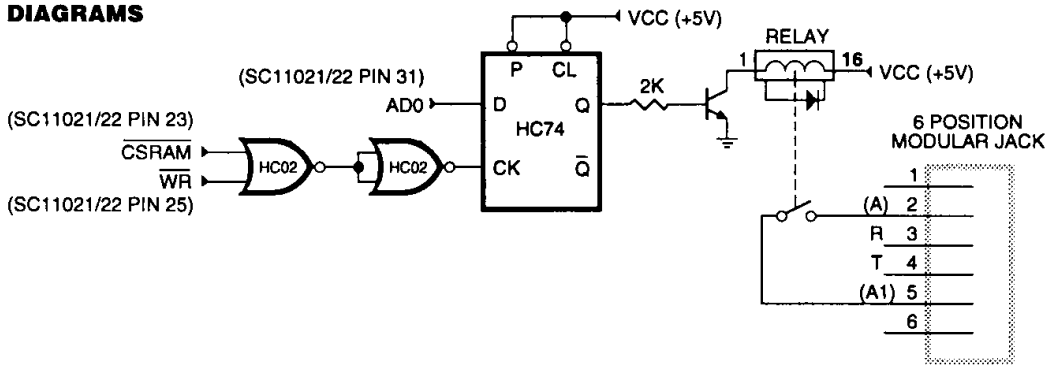


Figure 10. Circuit for Implementing & J1 Command

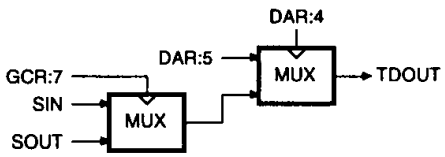


Figure 11. TDOUT Function

THE MAC AND INTEL 8096 SPEED COMPARISON

The attached is an instruction execution time comparison for the MAC and Intel 8096. The biggest improvement over 8096 is the 16 bit multiplication, it is 3.3 µs versus 6.5 µs. The jump instructions are twice as fast. The shift instructions are also about twice faster. The other arithmetic and logic instructions are about the same speed. Indirect addressing instructions in the MAC is about 20% slower than in the 8096.

The following comparison is for the 8096 with 12 MHz crystal and the MAC with 19.6608 MHz. The time unit is "µs". The instructions and operands are all from internal storage. Both the MAC and Intel 8096 will run slower for external storage access.

INSTRUCTION	OPERANDS	DIRECT MAC	DIRECT 8096	IMMEDIATE MAC	IMMEDIATE 8096	INDIRECT MAC	INDIRECT 8096
ADD	2	1.02	1.00	1.22	1.25	1.94	1.50
ADD	3	1.02	1.25	1.22	1.50	1.94	1.75
ADDB	2	1.02	1.00	1.02	1.00	1.94	1.50
ADDB	3	1.02	1.25	1.02	1.25	1.94	1.75
AND	2	1.02	0.75	1.22	1.25	1.94	1.50
AND	3	1.02	1.00	1.22	1.50	1.94	1.75
ANDB	2	1.02	1.00	1.02	1.00	1.94	1.50
ANDB	3	1.02	1.25	1.02	1.25	1.94	1.75
CMP	2	1.02	1.00	1.22	1.25	1.94	1.50
CMPB	2	1.02	1.00	1.02	1.00	1.94	1.50
DJNZ		0.92/1.25	1.25/2.25	(NO JUMP/JUMP)			
EXTB		0.71	1.00				
JBC		1.02/1.32	1.25/2.25				
JBS		1.02/1.32	1.25/2.25				
JC		0.51/0.82	1.00/2.00				
JE		0.51/0.82	1.00/2.00				
JGE		0.51/0.82	1.00/2.00				
JGT		0.51/0.82	1.00/2.00				
JH		0.51/0.82	1.00/2.00				
JLE		0.51/0.82	1.00/2.00				
JLT		0.51/0.82	1.00/2.00				
JNC		0.51/0.82	1.00/2.00				
JNE		0.51/0.82	1.00/2.00				
JNH		0.51/0.82	1.00/2.00				
JNV		0.51/0.82	1.00/2.00				
JV		0.51/0.82	1.00/2.00				
LCALL		1.12	3.25				
LD	2	1.02	1.00	1.22	1.25	1.94	1.50
LDB	2	1.02	1.00	1.02	1.00	1.94	1.50
LJMP	1	0.92	2.00	1.02	1.00	1.94	1.50
MUL	3	3.36	6.50	(BIGGEST IMPROVEMENT)			
NOP		0.24	1.00				
OR	2	1.02	1.00	1.22	1.25	1.94	1.50
ORB	2	1.02	1.00	1.02	1.00	1.94	1.50
PUSHF		0.51	2.00				
POPF		0.51	2.25				
RET		1.02	3.00				
SHL		1.12+0.10N	1.75+0.25N	(N = SHIFT COUNT)			
SHLB		1.12+0.10N	1.75+0.25N				
SHLL		1.53+0.10N	1.75+0.25N				
SHR		1.12+0.10N	1.75+0.25N				
SHRB		1.12+0.10N	1.75+0.25N				
SHRL		1.53+0.10N	1.75+0.25N				
SHRA		1.02+0.10N	1.75+0.25N				
SHRAL		1.53+0.10N	1.75+0.25N				
SJMP		0.71	2.00				
ST		1.32	1.75				
STB		1.32	1.75				
SUB	2	1.02	1.00	1.22	1.25	1.94	1.50
SUBB	2	1.02	1.00	1.02	1.00	1.94	1.50
SUB	3	1.02	1.25	1.22	1.50	1.94	1.75
SUBB	3	1.02	1.25	1.02	1.25	1.94	1.75
XOR	2	1.02	1.00	1.22	1.25	1.94	1.50
XORB	2	1.02	1.00	1.02	1.00	1.94	1.50

APPLICATIONS

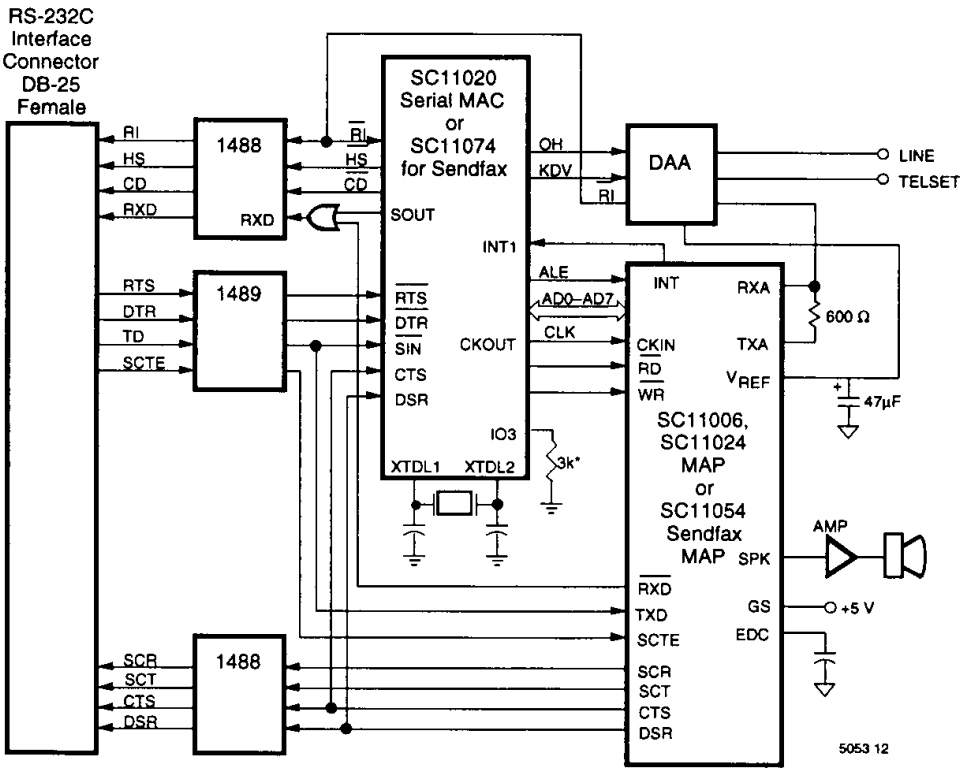


Figure 12. V22 bis Standalone Intelligent Modem with Internal ROM.

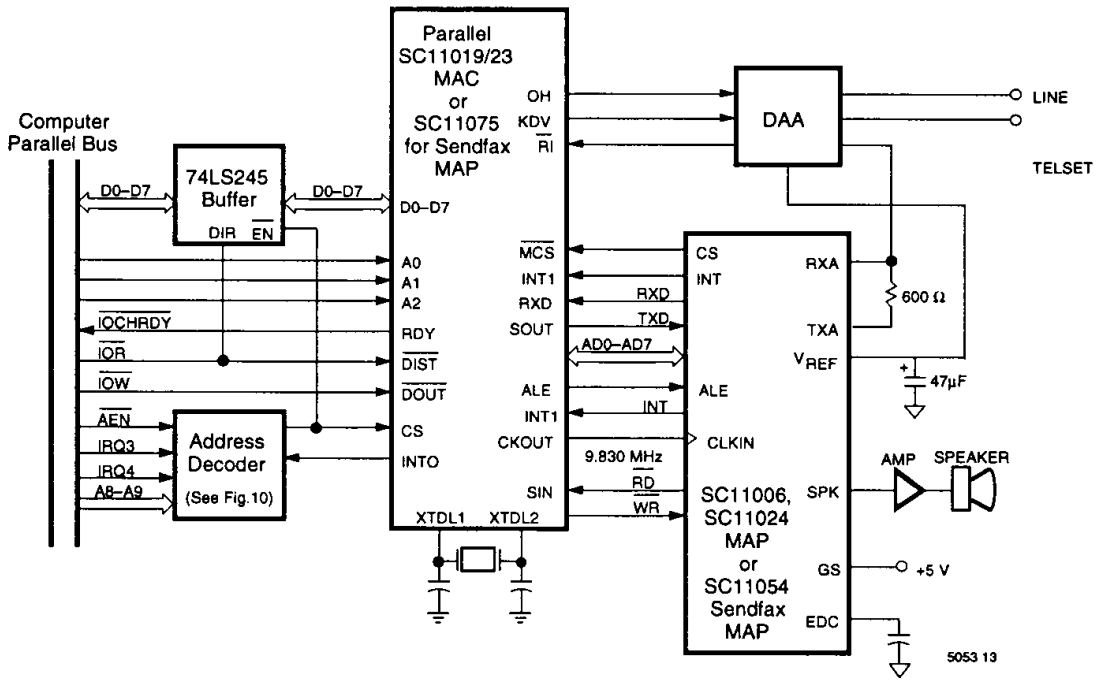


Figure 13. Internal Smart Modem for PC Bus Applications with Internal ROM.

For additional application information, consult the MAP data sheets (SC11006, SC11024, SC11026, SC11046, SC11054 etc.).

Detailed firmware and schematic information is available through your local Sierra sales office and our BBS – (408) 263-8294.