# Features

- Enhanced DisplayPort® (DP) receiver
  - DP 1.1a compliant
  - Embedded DisplayPort (eDP) compliant
  - 1, 2, or 4 lanes
- Higher bandwidth "Turbo mode" (3.24 Gbps per lane), supports:
  - 1920 x 1080 (FHD) 120 Hz/10-bit color video standard timings and 7.1 Ch audio
  - 2560 x 1600 (WQXGA), 2560 x 2048 (QSXGA) 60 Hz/10-bit color graphics and 7.1 Ch audio
- Interface compatibility with wide range of display controller ICs
  - LVTTL (60 wide) and LVDS (quad bus) video interface
  - 8-Ch I2S and SPDIF audio interface
- Robust AUX channel
  - Link service, maintenance
  - I2C-over-AUX (MCCS, DDC)
  - IR, full duplex UART protocol
- Configurable through I2C host interface
- Supports HDCP 1.3 with on-chip keys

- HDCP repeater capability
  - Acts as upstream receiver
- AUX to I2C bridge for EDID, MCCS pass through
- Spread spectrum on DisplayPort, LVDS, and TTL interfaces for EMI reduction
- Supports deep color and color format conversion
  - RGB/YUV (4:4:4) – 10-bit color
  - YUV (4:2:2/4:2:0) – 12-bit color
  - RGB (4:4:4) to YUV (4:4:4) conversion and vice-versa
- Supports HBR/"Turbo" speed over HBR/RBR-rated long cables (15 m and more)
- Package
  - 164 LFBGA (12 x 12 mm / 0.8 mm)
- Power supply voltages
  - 3.3 V I/O; 1.2 V core

Applications

- Digital TV, LCD monitor, mobile display, projector, etc
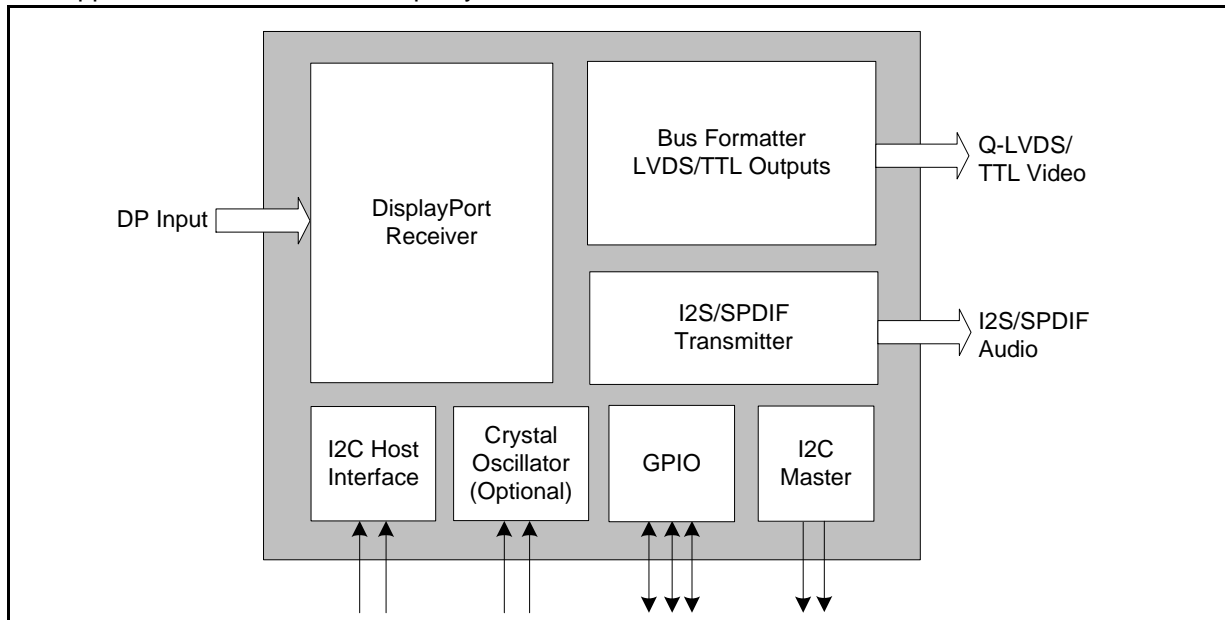
1. Description

The STDP4020 is a DisplayPort receiver IC for the reception of secure, high-bandwidth uncompressed digital audio-video signals targeted for applications such as DTV, LCD monitor, projector, and other types of display systems. STDP4020 is a VESA DP 1.1a and eDP compliant device, implementing a single link DisplayPort input port comprising four main lanes, auxiliary channel, and HPD. In addition to the standard HBR (2.7 Gbps) and RBR (1.62 Gbps) speeds, this device supports turbo speed of 3.24 Gbps per lane with a total link bandwidth of 12.96 Gbps. The higher bandwidth provides unique benefits to users over other commercial DP receivers for embedded applications by offering additional margin to support higher color depth, resolution, and refresh rate. For example, STDP4020 supports FHD non-reduced blanking video (1080p 30-bit color per pixel) at 120 Hz, plus 7.1 Ch audio for two-box TV applications.The advanced equalizer built in this device offers guaranteed performance over long reach cables. The auxiliary channel in STDP4020 acts as a bidirectional communication link, supporting application-specific protocols such as MCCS, DDC, UART, IR, as well as the dedicated DisplayPort link training and device management functions.

The STDP4020 supports RGB and YUV video color formats with color depth of 12 (YUV 4:2:2 only), 10, and 8 bits. This device offers LVDS and LVTTL output interfaces configurable to map a wide range of display controller products. The Quad LVDS interface supports video signals up to 400 MHz pixel rate with flexible channel and lane swapping options. The 60-bit LVTTL output ports can be mapped to transfer video data either in two pixels per clock or single pixel per clock up to 330 MHz pixel rate, which opens up possibilities for 3D applications. The STDP4020 also supports both compressed and uncompressed audio formats. The extracted audio signal is transferred on a digital audio output bus. This device comprises four I2S audio output, supporting up to 8 channel LPCM audio and a single wire S/PDIF output for encoded audio. The STDP4020 features the HDCP 1.3 content protection scheme with an embedded key option for secure reception of digital audio-video content. In addition, it also supports the HDCP repeater function and, thus acts as an upstream receiver suitable for two-box TV and HDMI/DVI converter applications.

The STDP4020 is configurable from an external host controller through I2C host interface. This IC also includes general-purpose inputs/outputs for controlling system components. The STDP4020 features a color space converter (RGB to YUV and YUV to RGB) for flexible interface with external video processing devices.

2.   Application overview

The STDP4020 is designed as a DisplayPort front-end capture device for display applications. Typical display design has a display controller (scaler) that acts as system master (host). The host controller configures STDP4020 through a 2-wire host interface. The host and STDP4020 also use interrupt mechanism whenever the slave needs attention. The STDP4020 may require an external SPI Flash to store firmware for supporting custom specific applications. The audio and video output from STDP4020 can directly interface to the host display controller for further processing. The AUX I2C bypass channel handles the I2C traffic between STDP4020 and host controller, as shown in the figure below.

Figure 1. System interface block diagram
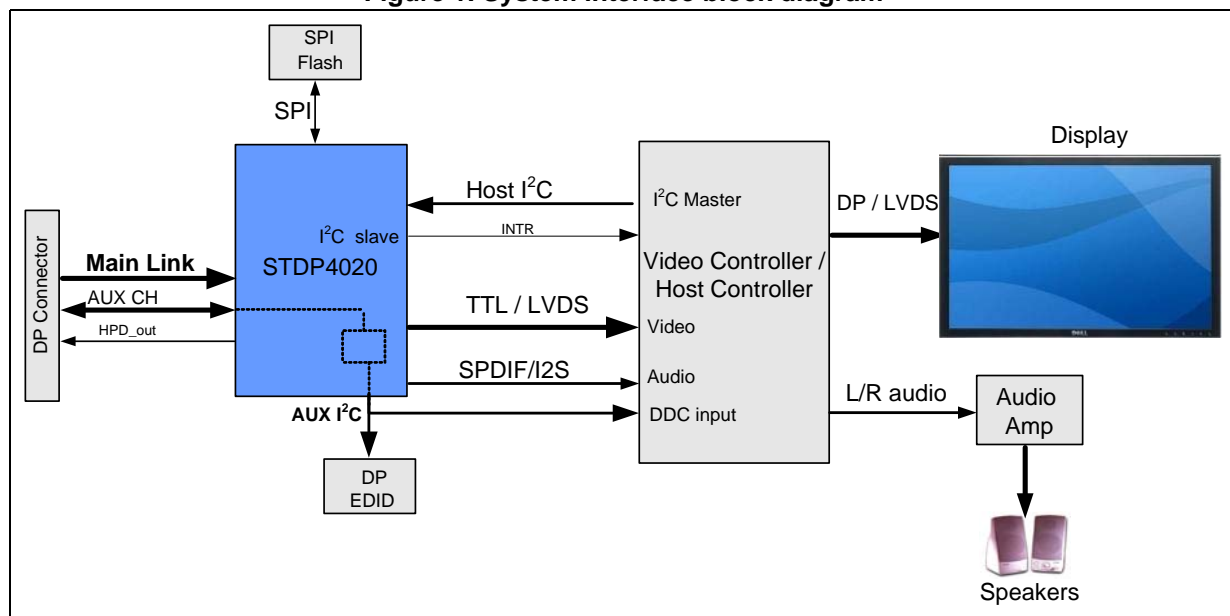
3. Feature attributes

- Enhanced DisplayPort (DP) receiver compliant with DP1.1a and embedded (eDP) specification

- Supports higher bandwidth mode called "Turbo mode" (3.24 Gbps per lane) for embedded applications. For example, supports FHD 120 Hz-10/12-bit video or QSXGA (2560 x 2048) 60 Hz/10-bit color graphics and 7.1 Ch audio

- Interface compatibility with wide range of display products. Supports LVTTL (60 wide) and quad LVDS video interface

- Supports I2S 8 Ch and SPDIF audio output interface compliant with IEC60958 and IEC61937 audio formats.

- Robust AUX channel for Link service, maintenance and supports I2C over AUX, MCCS, DDC, IR and full duplex UART protocol

- Supports HDCP 1.3 with on-chip key storage

- Acts HDCP repeater for an upstream receiver

- Supports AUX to I2C bridge for EDID, MCCS pass through

- Spread spectrum on DisplayPort, LVDS and TTL interfaces for EMI reduction

- Supports deep color and color format conversion: RGB (4:4:4) to YUV (4:4:4) and vice-versa

- Supports TTL up to 330 MHz pixel clock, which allows 3D video applications

- Supports HBR/"Turbo" speed over HBR/RBR rated long cables (15 m and more)

- Configurable through I2C host interface

- Package: 164 LFBGA (12 x 12 mm / 0.8 mm)

- Power supply voltages: 3.3 V I/O; 1.2 V core

4.   Ordering information

Table 1. Order codes

Part number	Description
STDP4020-AD	164 LFBGA (12 x 12 mm)
STDP4010-AD	164 LFBGA (12 x 12 mm)

5.　Revision history

Table 2. Document revision history

Date	Revision	Changes
10-Sep-2009	1	Initial release.
28-May-2014	2	Updated to comply with MegaChips documentation style/formatting.
15-Sep-2014	3	Updated footers and added copyright information to last page.

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