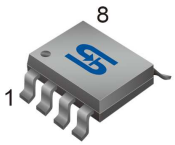
TSM4953D

30V Dual P-Channel MOSFET

SOP-8



Pin Definition:

1. Source 1	8. Drain 1
2. Gate 1	7. Drain 1
3. Source 2	6. Drain 2
4. Gate 2	5. Drain 2

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$(mΩ)	I_D (A)
-30	60 @ V_{GS} = 10V	-4.9
	90 @ V_{GS} = 4.5V	-3.7

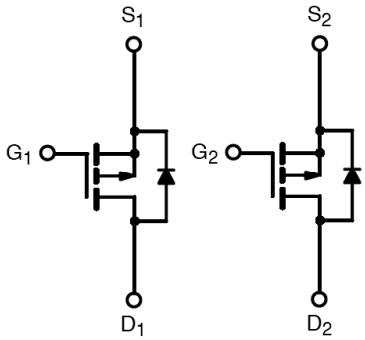
Features

- Advance Trench Process Technology
- High Density Cell Design for Ultra Low On-resistance

Application

- Load Switch
- PA Switch

Block Diagram



Dual P-Channel MOSFET

Ordering Information

Part No.	Package	Packing
TSM4953DCS RL	SOP-8	2.5Kpcs / 13” Reel
TSM4953DCS RLG	SOP-8	2.5Kpcs / 13” Reel

Note: “G” denotes Halogen Free Product.

Absolute Maximum Rating (Ta = 25°C unless otherwise noted)

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current, V_{GS} @4.5V.		I_D	-4.9	A
Pulsed Drain Current, V_{GS} @4.5V		I_{DM}	-20	A
Continuous Source Current (Diode Conduction)[a,b]		I_S	-2.6	A
Maximum Power Dissipation	Ta = 25°C	P_D	2.5	W
	Ta = 70°C		1.3	
Operating Junction Temperature		T_J	+150	°C
Operating Junction and Storage Temperature Range		T_J, T_{STG}	- 55 to +150	°C

Thermal Performance

Parameter	Symbol	Limit	Unit
Junction to Case Thermal Resistance	$R\Theta_{JC}$	40	°C/W
Junction to Ambient Thermal Resistance (PCB mounted)	$R\Theta_{JA}$	62.5	°C/W

Notes:

a. Pulse width limited by the Maximum junction temperature

b. Surface Mounted on FR4 Board, t ≤ 5 sec.

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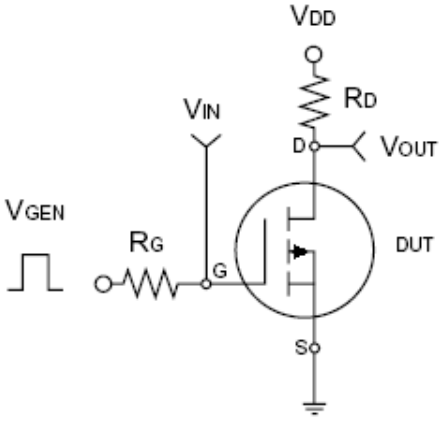
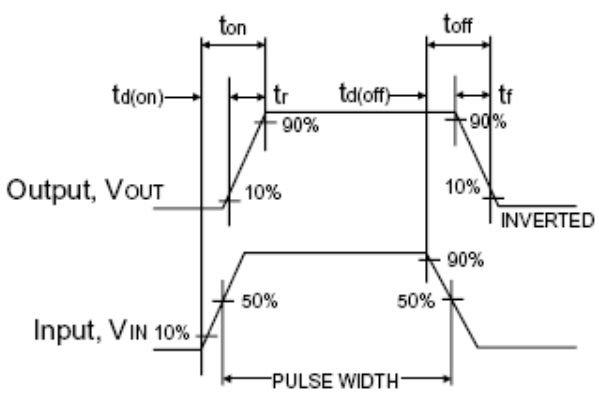
Electrical Specifications (Ta = 25°C unless otherwise noted)

Parameter	Conditions	Symbol	Min	Typ	Max	Unit
Static						
Drain-Source Breakdown Voltage	V_{GS} = 0V, I_D = -250uA	BV_{DSS}	-30	--	--	V
Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250μA	$V_{GS(TH)}$	-1.0	-1.5	-3.0	V
Gate Body Leakage	V_{GS} = ±20V, V_{DS} = 0V	I_{GSS}	--	--	±100	nA
Zero Gate Voltage Drain Current	V_{DS} = -24V, V_{GS} = 0V	I_{DSS}	--	--	-1.0	μA
On-State Drain Current[a]	V_{DS} =-5V, V_{GS} = -10V	$I_{D(ON)}$	-6	--	--	A
Drain-Source On-State Resistance[a]	V_{GS} = -10V, I_D = -4.9A	$R_{DS(ON)}$	--	50	60	mΩ
	V_{GS} = -4.5V, I_D = -3.7A		--	75	90	
Forward Transconductance[a]	V_{DS} = -15V, I_D = -4.9A	g_{fs}	--	10	--	S
Diode Forward Voltage	I_S = -1.9A, V_{GS} = 0V	V_{SD}	--	--	-1.3	V
Dynamic						
Total Gate Charge	V_{DS} = -15V, I_D = -4.9A, V_{GS} = -10V	Q_g	--	28	--	nC
Gate-Source Charge		Q_{gs}	--	3	--	
Gate-Drain Charge		Q_{gd}	--	7	--	
Input Capacitance	V_{DS} = -15V, V_{GS} = 0V, f = 1.0MHz	C_{iss}	--	745	--	pF
Output Capacitance		C_{oss}	--	440	--	
Reverse Transfer Capacitance		C_{rss}	--	120	--	
Switching						
Turn-On Delay Time	V_{DD} = -15V, R_L = 15Ω, I_D = -1A, V_{GEN} = -10V, R_G = 6Ω	$t_{d(on)}$	--	9	--	nS
Turn-On Rise Time		t_r	--	15	--	
Turn-Off Delay Time		$t_{d(off)}$	--	75	--	
Turn-Off Fall Time		t_f	--	40	--	

Notes:
1. pulse test: PW ≤300μS, duty cycle ≤2%
2. For DESIGN AID ONLY, not subject to production testing.
3. Switching time is essentially independent of operating temperature.



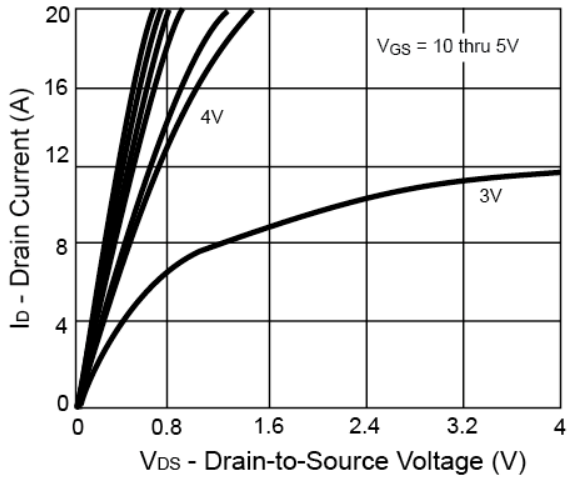
Switching Test Circuit



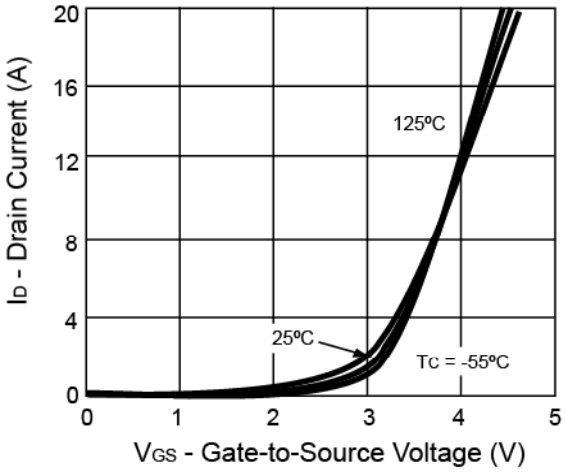
Switchin Waveforms

Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

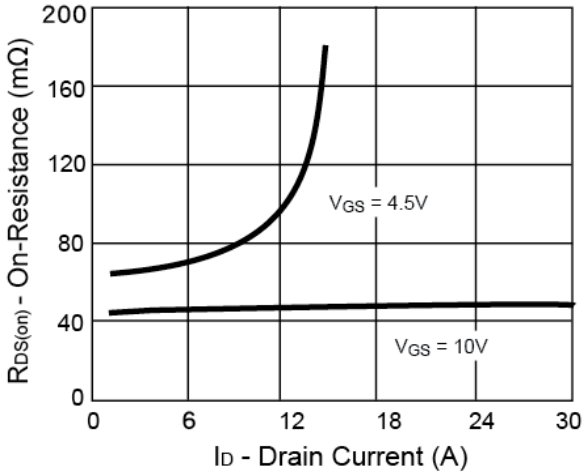
Output Characteristics



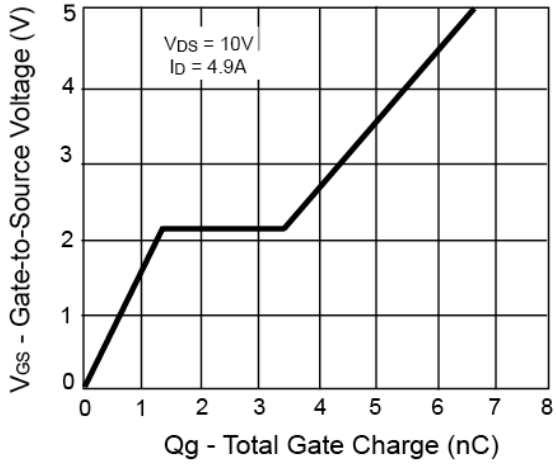
Transfer Characteristics



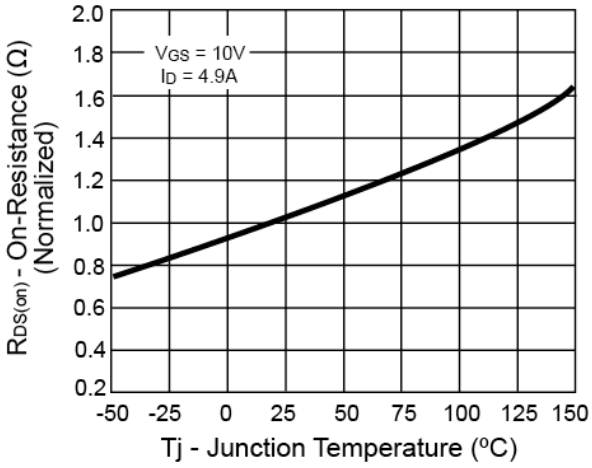
On-Resistance vs. Drain Current



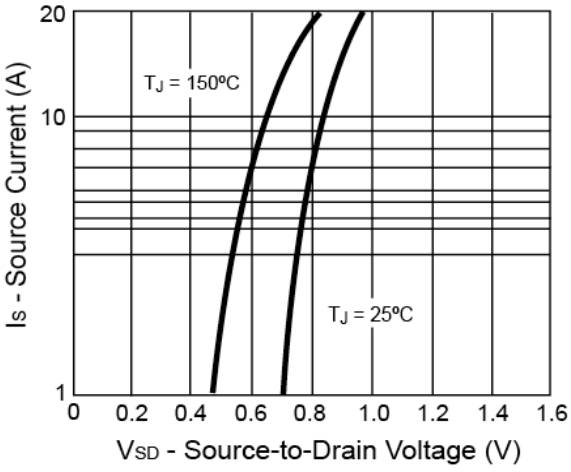
Gate Charge



On-Resistance vs. Junction Temperature

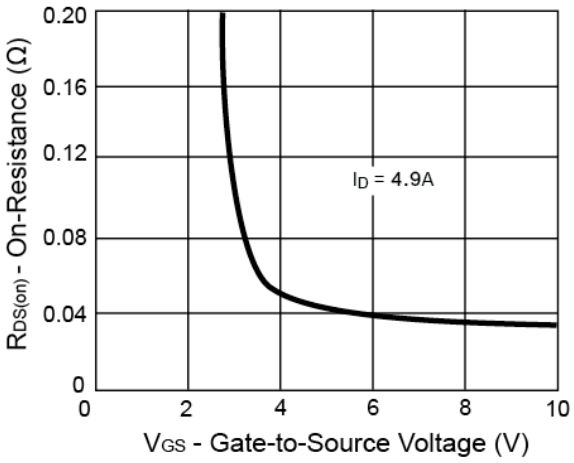


Source-Drain Diode Forward Voltage

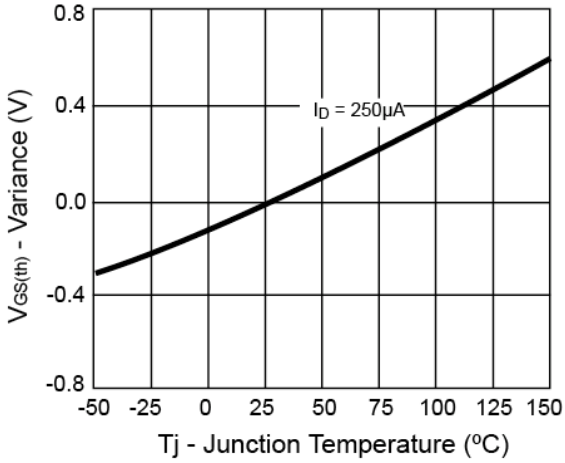


Electrical Characteristics Curve (Ta = 25°C, unless otherwise noted)

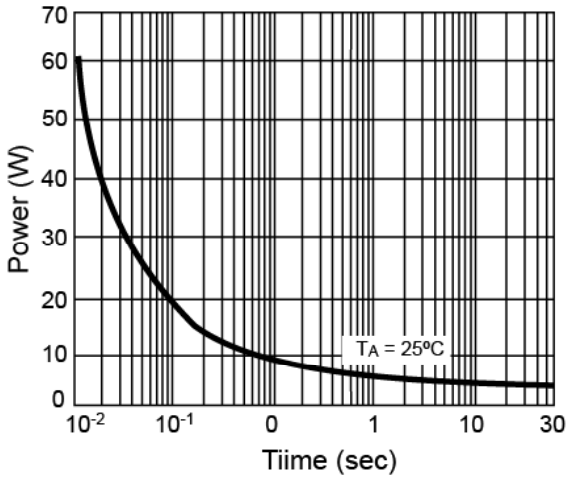
On-Resistance vs. Gate-Source Voltage



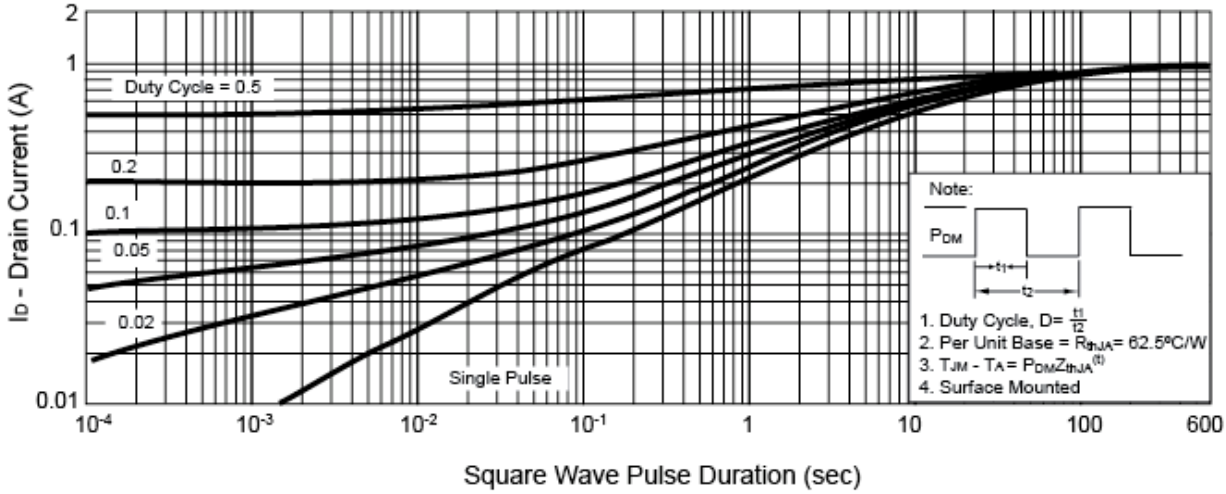
Threshold Voltage



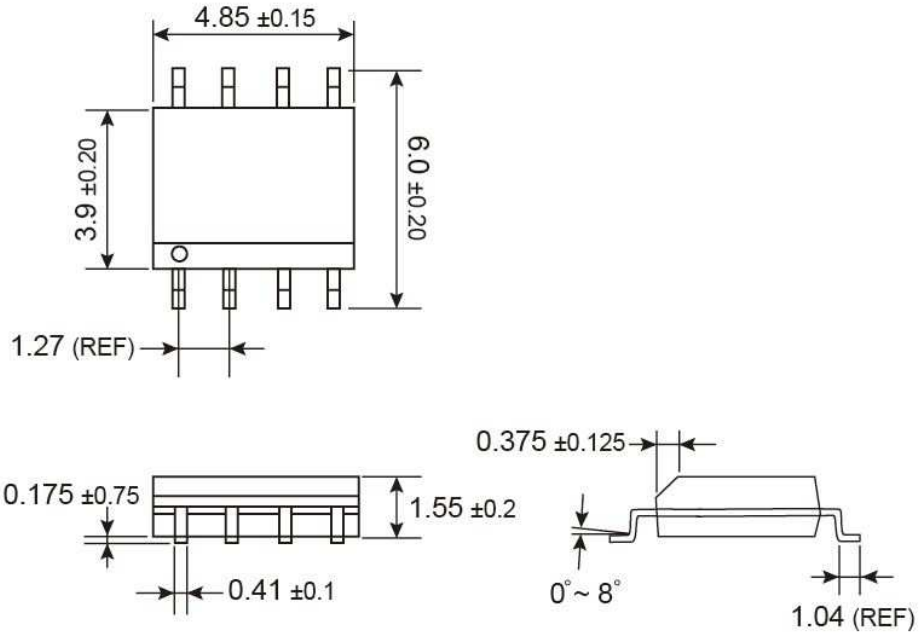
Single Pulse Power



Normalized Thermal Transient Impedance, Junction-to-Ambient

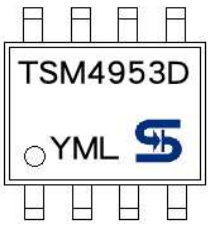


SOP-8 Mechanical Drawing



Unit: Millimeters

Marking Diagram



Y = Year Code
M = Month Code
(**A**=Jan, **B**=Feb, **C**=Mar, **D**=Apl, **E**=May, **F**=Jun, **G**=Jul, **H**=Aug, **I**=Sep, **J**=Oct, **K**=Nov, **L**=Dec)
= Month Code for Halogen Free Product
(**O**=Jan, **P**=Feb, **Q**=Mar, **R**=Apl, **S**=May, **T**=Jun, **U**=Jul, **V**=Aug, **W**=Sep, **X**=Oct, **Y**=Nov, **Z**=Dec)
L = Lot Code

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