FAIRCHILD SEMICONDUCTOR®

April 2013

FDP8N50NZU / FDPF8N50NZU

N-Channel UniFET™ II Ultra FRFET™ MOSFET

500 V, 6.5 A, 1.2 Ω

Features

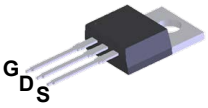
- $R_{DS(on)}$ = 1.0 Ω (Typ.) @ V_{GS} = 10 V, I_D = 3.25 A
- Low Gate Charge (Typ. 14 nC)
- Low C_{rss} (Typ. 5 pF)
- 100% Avalanche Tested
- Improve dv/dt Capability
- ESD Improved Capability
- RoHS Compliant

Application

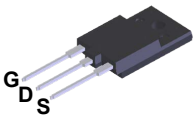
- LCD/LED TV
- Lighting
- Uninterruptible Power Supply
- AC-DC Power Supply

Description

UniFET™ II MOSFET is Fairchild Semiconductor®'s high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2kV HBM surge stress. UniFET II Ultra FRFET™ MOSFET has much superior body diode reverse recovery performance. Its t_{rr} is less than 50nsec and the reverse dv/dt immunity is 20V/nsec while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore UniFET II Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



TO-220



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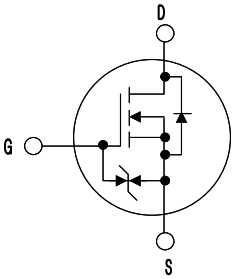


MOSFET Maximum Ratings T_C = 25°C unless otherwise noted

Symbol	Parameter		FDP8N50NZU	FDPF8N50NZU	Unit
V_{DSS}	Drain to Source Voltage		500		V
V_{GSS}	Gate to Source Voltage		±25		V
I_D	Drain Current	-Continuous (T_C = 25°C)	6.5	6.5*	A
		-Continuous (T_C = 100°C)	3.9	3.9*	
I_{DM}	Drain Current	- Pulsed (Note 1)	26	26*	A
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	80		mJ
I_{AR}	Avalanche Current	(Note 1)	6.5		A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	13		mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20		V/ns
P_D	Power Dissipation	(T_C = 25°C)	130	40	W
		- Derate above 25°C	1	0.32	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150		°C
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds		300		°C

*Drain current limited by maximum junction temperature

Thermal Characteristics

Symbol	Parameter	FDP8N50NZU	FDPF8N50NZU	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.96	3.1	°C/W
$R_{\theta CS}$	Thermal Resistance, Case to Sink, Typ.	0.5	-	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	62.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDP8N50NZU	FDP8N50NZU	TO-220	-	-	50
FDPF8N50NZU	FDPF8N50NZU	TO-220F	-	-	50

Electrical Characteristics $T_C = 25^oC$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250μA, V_{GS} = 0V, T_C = 25°C	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250μA, Referenced to 25°C	-	0.5	-	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 500V, V_{GS} = 0V	-	-	25	μA
		V_{DS} = 400V, T_C = 125°C	-	-	250	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±25V, V_{DS} = 0V	-	-	±10	μA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250μA	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10V, I_D = 4A	-	1.0	1.2	Ω
g_{FS}	Forward Transconductance	V_{DS} = 20V, I_D = 4A	-	6.3	-	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 25V, V_{GS} = 0V, f = 1MHz	-	565	735	pF
C_{oss}	Output Capacitance		-	80	105	pF
C_{rss}	Reverse Transfer Capacitance		-	5	8	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	V_{DS} = 400V, I_D = 6.5A, V_{GS} = 10V (Note 4, 5)	-	14	18	nC
Q_{gs}	Gate to Source Gate Charge		-	4	-	nC
Q_{gd}	Gate to Drain “Miller” Charge		-	6	-	nC
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = 250V, I_D = 6.5A, R_G = 25Ω, V_{GS} = 10V (Note 4, 5)	-	17	45	ns
t_r	Turn-On Rise Time		-	34	80	ns
$t_{d(off)}$	Turn-Off Delay Time		-	43	95	ns
t_f	Turn-Off Fall Time		-	27	60	ns
Drain-Source Diode Characteristics						
I_S	Maximum Continuous Drain to Source Diode Forward Current		-	-	6.5	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		-	-	26	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0V, I_{SD} = 6.5A	-	-	1.6	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0V, I_{SD} = 6.5A, dI_F/dt = 100A/μs	-	50	-	ns
Q_{rr}	Reverse Recovery Charge		-	0.05	-	μC

Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. L = 3.8mH, I_{AS} = 6.5A, V_{DD} = 50V, R_G = 25Ω, Starting T_J = 25°C
3. $I_{SD} \le$ 6.5A, di/dt ≤ 200A/μs, $V_{DD} \le BV_{DSS}$, Starting T_J = 25°C
4. Pulse Test: Pulse width ≤ 300μs, Duty Cycle ≤ 2%
5. Essentially Independent of Operating Temperature Typical Characteristics

Typical Performance Characteristics

Figure 1. On-Region Characteristics

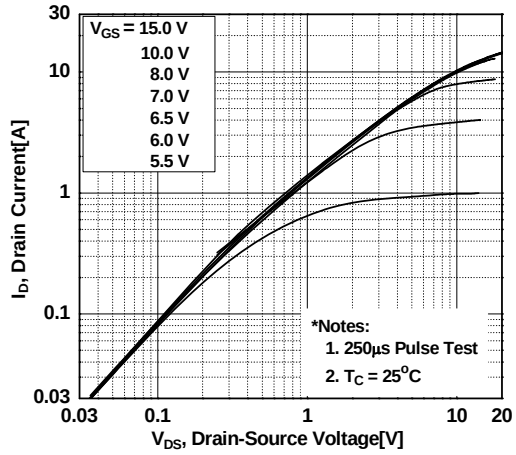


Figure 2. Transfer Characteristics

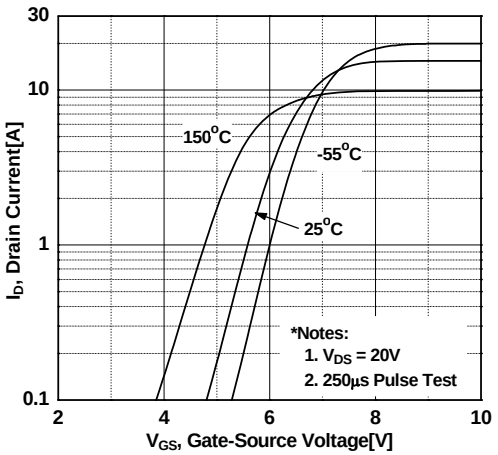


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

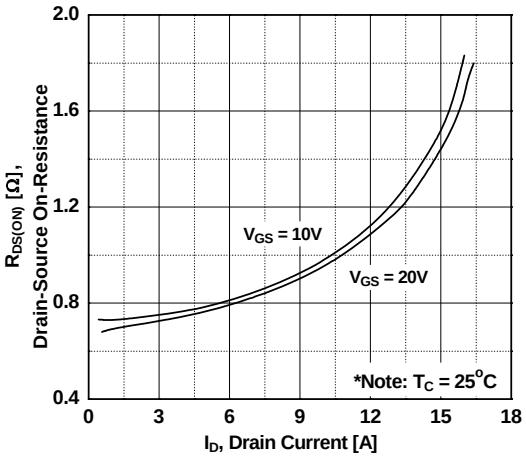


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

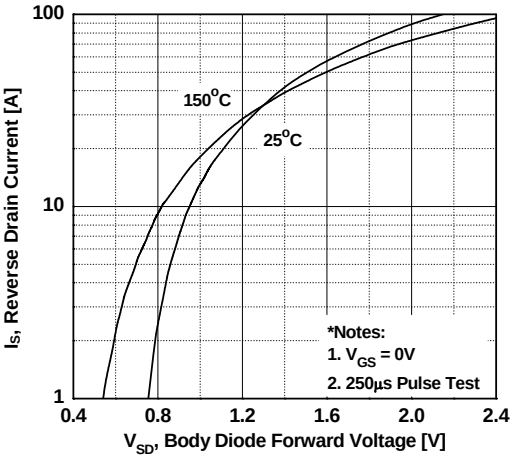


Figure 5. Capacitance Characteristics

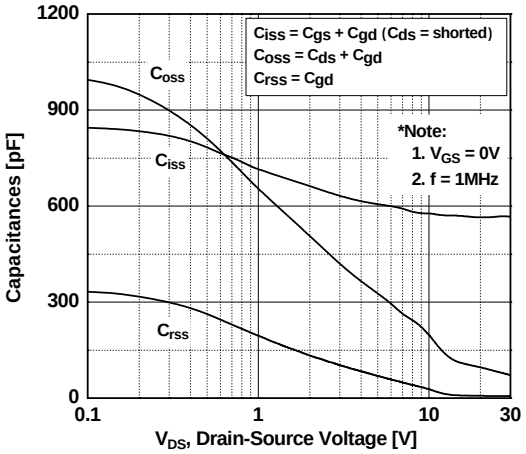
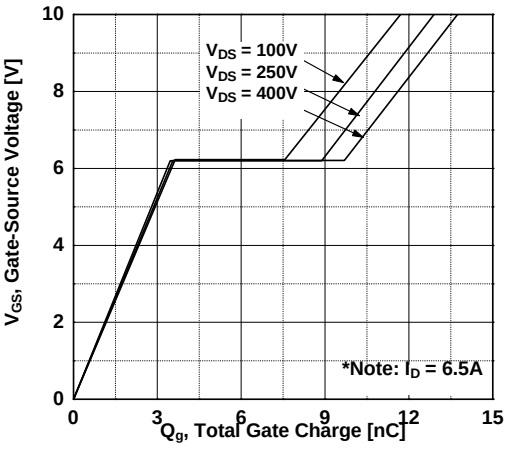


Figure 6. Gate Charge Characteristics



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

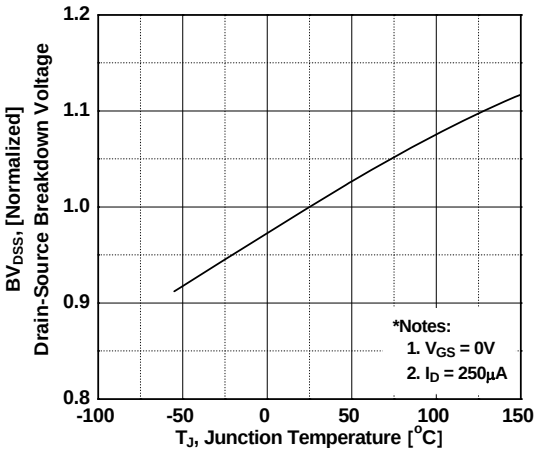


Figure 8. Maximum Safe Operating Area - FDPF8N50NZU

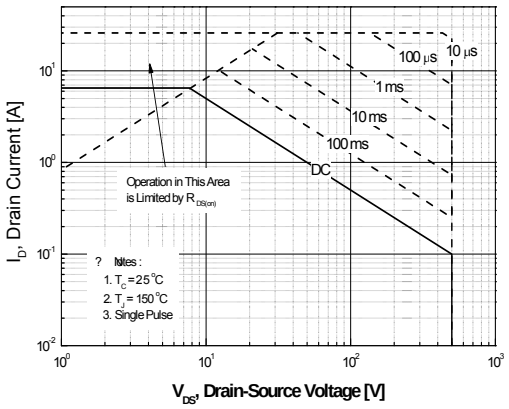


Figure 9. Maximum Drain Current vs. Case Temperature

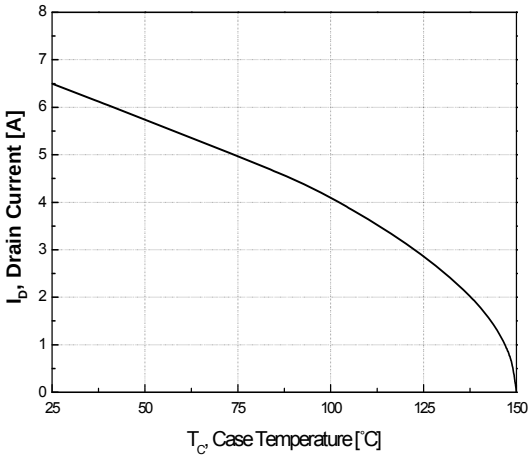
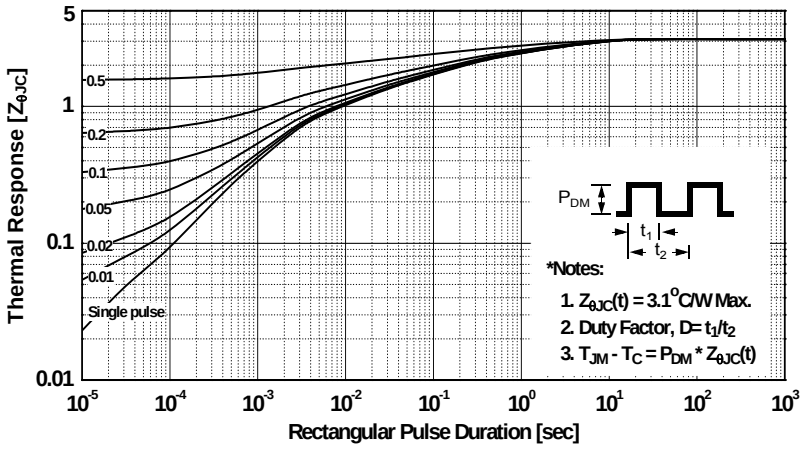
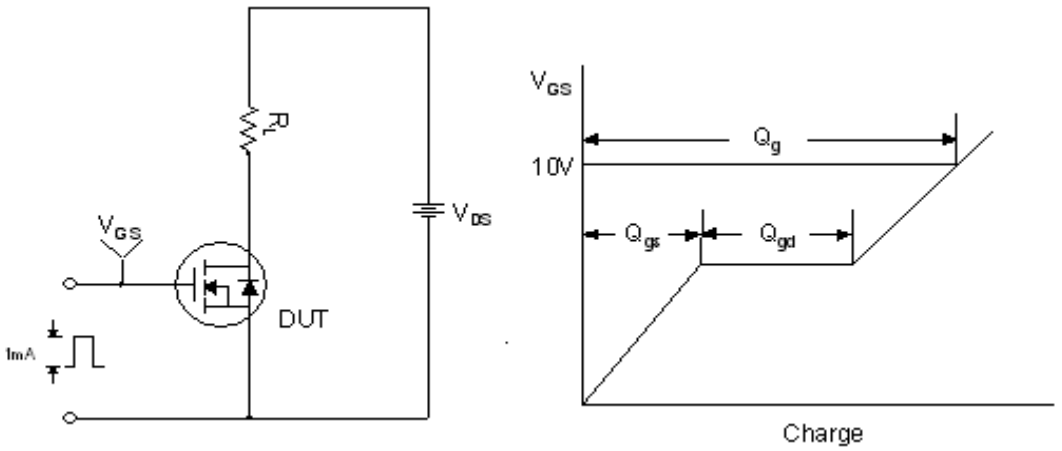


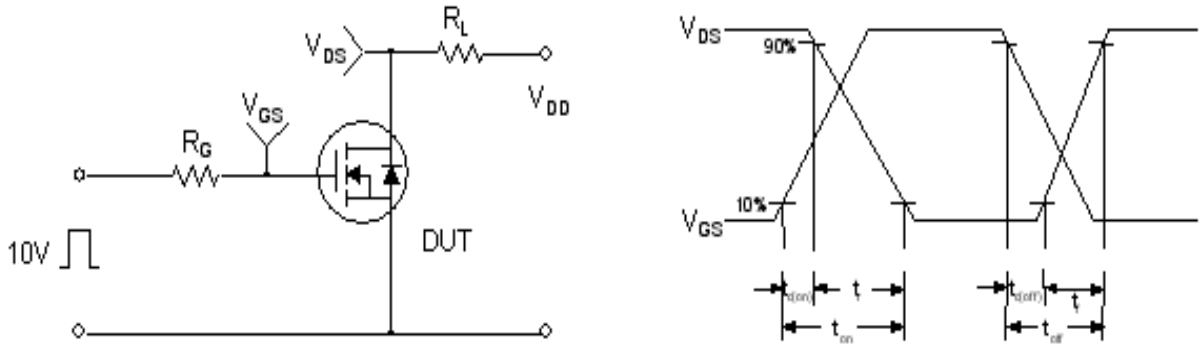
Figure 11. Transient Thermal Response Curve-FDPF8N50NZU



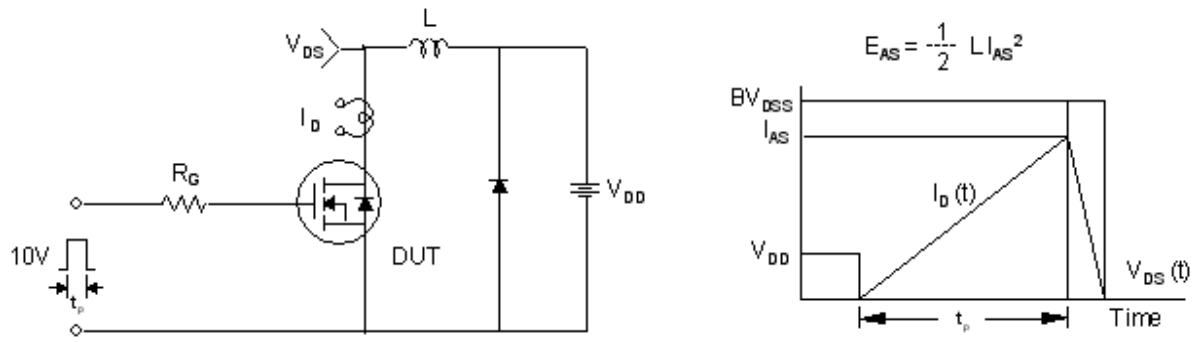
Gate Charge Test Circuit & Waveform



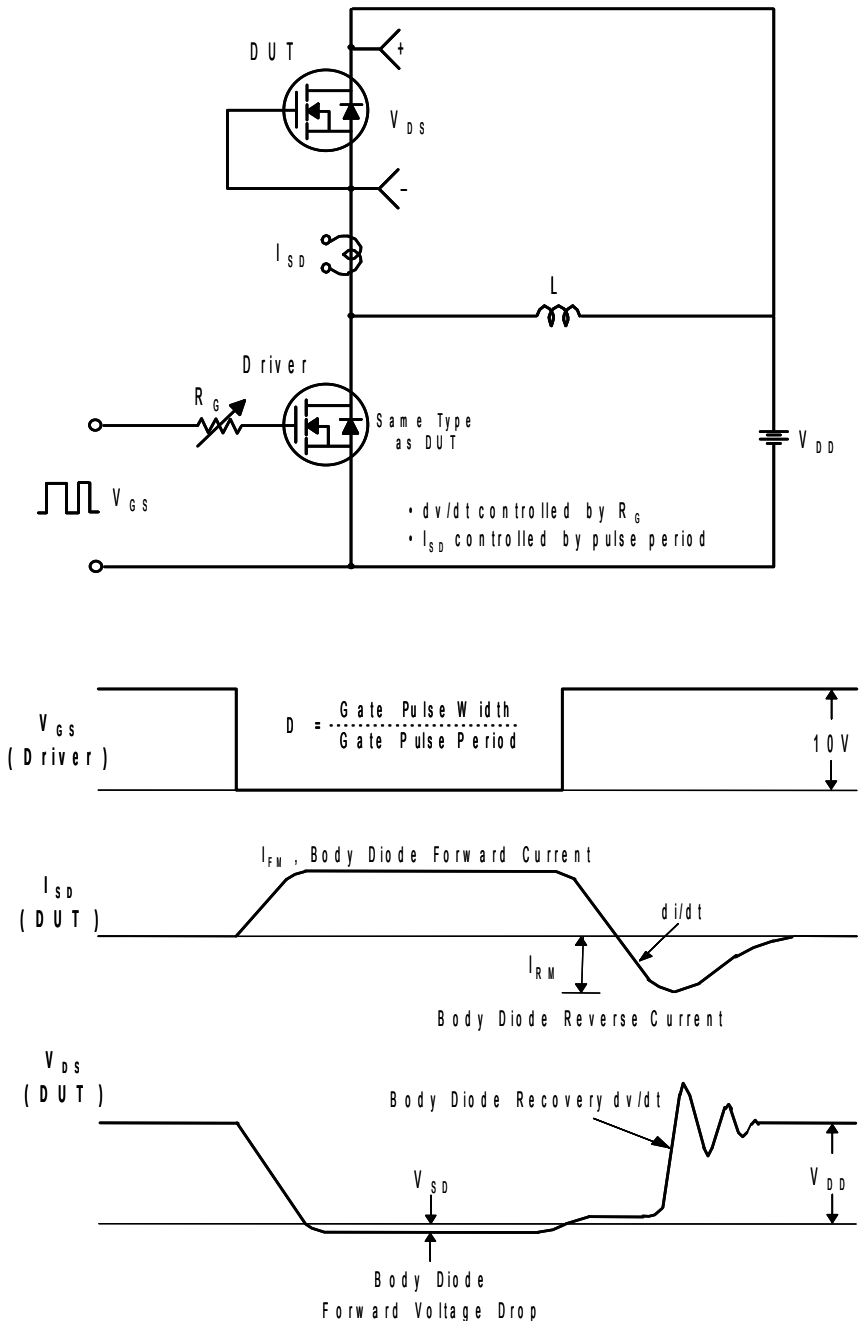
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching Test Circuit & Waveforms

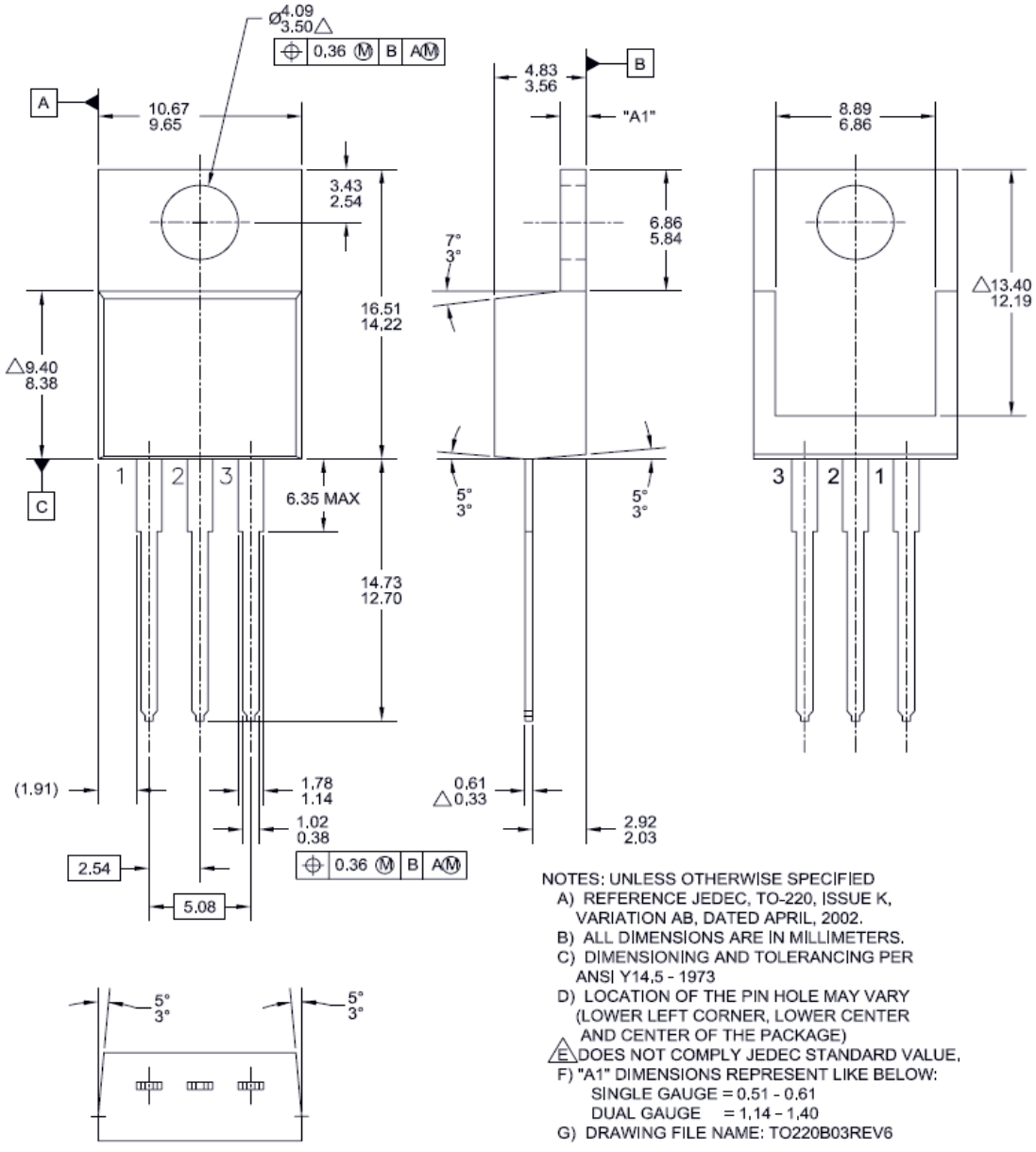


Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions

TO-220B03

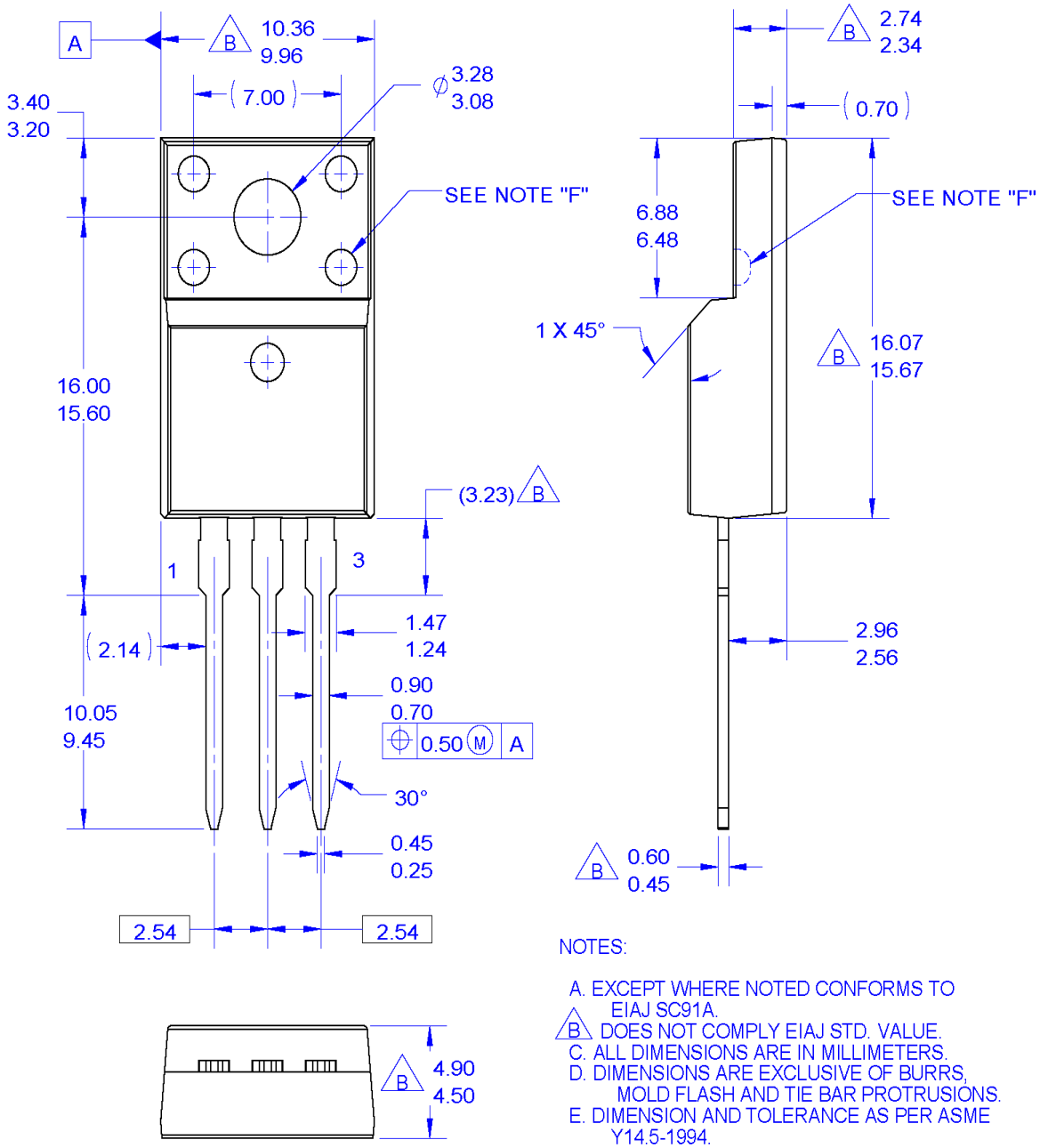


NOTES: UNLESS OTHERWISE SPECIFIED
A) REFERENCE JEDEC, TO-220, ISSUE K, VARIATION AB, DATED APRIL, 2002.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONING AND TOLERANCING PER ANSI Y14.5 - 1973
D) LOCATION OF THE PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF THE PACKAGE)
△E DOES NOT COMPLY JEDEC STANDARD VALUE,
F) "A1" DIMENSIONS REPRESENT LIKE BELOW:
SINGLE GAUGE = 0.51 - 0.61
DUAL GAUGE = 1,14 – 1,40
G) DRAWING FILE NAME: TO220B03REV6

Dimensions in Millimeters

Mechanical Dimensions

TO-220M03



NOTES:

A. EXCEPT WHERE NOTED CONFORMS TO EIAJ SC91A.
B DOES NOT COMPLY EIAJ STD. VALUE.
C. ALL DIMENSIONS ARE IN MILLIMETERS.
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.
E. DIMENSION AND TOLERANCE AS PER ASME Y14.5-1994.
F. OPTION 1 - WITH SUPPORT PIN HOLE.
OPTION 2 - NO SUPPORT PIN HOLE.
G. DRAWING FILE NAME: TO220M03REV3

Dimensions in Millimeters

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No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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