NTMFS5C612NL

Power MOSFET
60 V, 1.5 mΩ, 226 A, Single N–Channel

Features
- Small Footprint (5x6 mm) for Compact Design
- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- These Devices are Pb–Free and are RoHS Compliant

ON Semiconductor®

http://onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)}$ MAX	I_D MAX
60 V	1.5 mΩ @ 10 V	226 A
	2.3 mΩ @ 4.5 V	

N–CHANNEL MOSFET

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain–to–Source Voltage			V_{DSS}	60	V
Gate–to–Source Voltage			V_{GS}	±20	V
Continuous Drain Current $R_{θJC}$ (Notes 1, 3)	Steady State	$T_C = 25°C$	I_D	226	A
		$T_C = 100°C$		143	
Power Dissipation $R_{θJC}$ (Note 1)		$T_C = 25°C$	P_D	139	W
		$T_C = 100°C$		56	
Continuous Drain Current $R_{θJA}$ (Notes 1, 2, 3)	Steady State	$T_A = 25°C$	I_D	34	A
		$T_A = 100°C$		22	
Power Dissipation $R_{θJA}$ (Notes 1 & 2)		$T_A = 25°C$	P_D	3.2	W
		$T_A = 100°C$		1.3	
Pulsed Drain Current	$T_A = 25°C$, $t_p = 10$ μs		I_{DM}	900	A
Operating Junction and Storage Temperature			T_J, T_{stg}	−55 to +150	°C
Source Current (Body Diode)			I_S	158	A
Single Pulse Drain–to–Source Avalanche Energy ($I_{L(pk)} = 17$ A)			E_{AS}	451	mJ
Lead Temperature for Soldering Purposes (1/8″ from case for 10 s)			T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

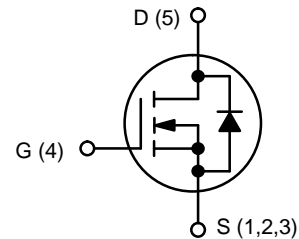| Parameter	Symbol	Value	Unit
Junction–to–Case – Steady State	$R_{θJC}$	0.9	°C/W
Junction–to–Ambient – Steady State (Note 2)	$R_{θJA}$	39	

1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface–mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.
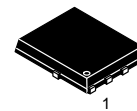

**DFN5
(SO–8FL)
CASE 488AA
STYLE 1**

MARKING DIAGRAM

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5C612L
AYWZZ
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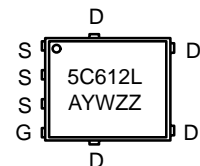
5C612L = Specific Device Code
A   = Assembly Location
Y   = Year
W   = Work Week
ZZ   = Lot Traceability

Publication Order Number:
NTMFS5C612NL/D

NTMFS5C612NL

ELECTRICAL CHARACTERISTICS ($T_J = 25°C$ unless otherwise specified)

Parameter	Symbol	Test Condition		Min	Typ	Max	Unit
OFF CHARACTERISTICS							
Drain–to–Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0$ V, $I_D = 250$ μA		60			V
Drain–to–Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$				12.7		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0$ V, $V_{DS} = 60$ V	$T_J = 25$ °C			1.0	μA
			$T_J = 125°C$			250	
Gate–to–Source Leakage Current	I_{GSS}	$V_{DS} = 0$ V, $V_{GS} = 20$ V				100	nA
ON CHARACTERISTICS (Note 4)							
Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}$, $I_D = 250$ μA		1.2		2.0	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$				–5.76		mV/°C
Drain–to–Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10$ V	$I_D = 50$ A		1.2	1.5	mΩ
		$V_{GS} = 4.5$ V	$I_D = 50$ A		1.65	2.3	
Forward Transconductance	g_{FS}	$V_{DS} = 15$ V, $I_D = 50$ A			151		S
CHARGES, CAPACITANCES & GATE RESISTANCE							
Input Capacitance	C_{ISS}	$V_{GS} = 0$ V, f = 1 MHz, $V_{DS} = 25$ V			6660		pF
Output Capacitance	C_{OSS}				2953		
Reverse Transfer Capacitance	C_{RSS}				45		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5$ V, $V_{DS} = 30$ V; $I_D = 50$ A			41		nC
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10$ V, $V_{DS} = 30$ V; $I_D = 50$ A			91		
Threshold Gate Charge	$Q_{G(TH)}$	$V_{GS} = 4.5$ V, $V_{DS} = 30$ V; $I_D = 50$ A			5		
Gate–to–Source Charge	Q_{GS}				17.1		
Gate–to–Drain Charge	Q_{GD}				10.9		
Plateau Voltage	V_{GP}				2.9		V
SWITCHING CHARACTERISTICS (Note 5)							
Turn–On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5$ V, $V_{DS} = 30$ V, $I_D = 50$ A, $R_G = 1.0$ Ω			19		ns
Rise Time	t_r				51		
Turn–Off Delay Time	$t_{d(OFF)}$				47		
Fall Time	t_f				18		
DRAIN–SOURCE DIODE CHARACTERISTICS							
Forward Diode Voltage	V_{SD}	$V_{GS} = 0$ V, $I_S = 50$ A	$T_J = 25°C$		0.78	1.2	V
			$T_J = 125°C$		0.66		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0$ V, dIS/dt = 100 A/μs, $I_S = 50$ A			78		ns
Charge Time	t_a				36		
Discharge Time	t_b				42		
Reverse Recovery Charge	Q_{RR}				105		nC

4. Pulse Test: pulse width ≤ 300 μs, duty cycle $\leq 2\%$.
5. Switching characteristics are independent of operating junction temperatures.

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
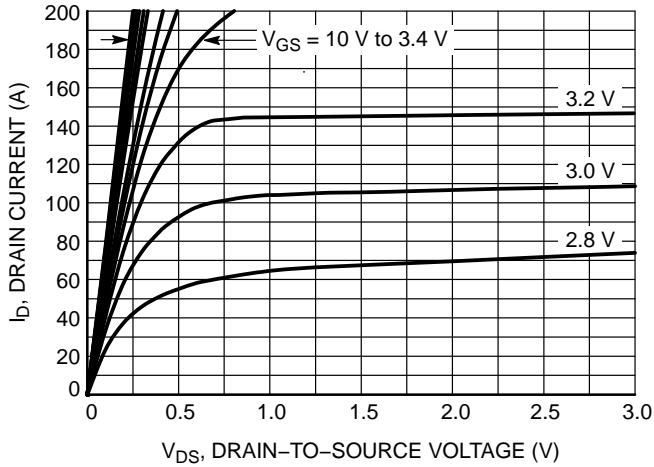
NTMFS5C612NL

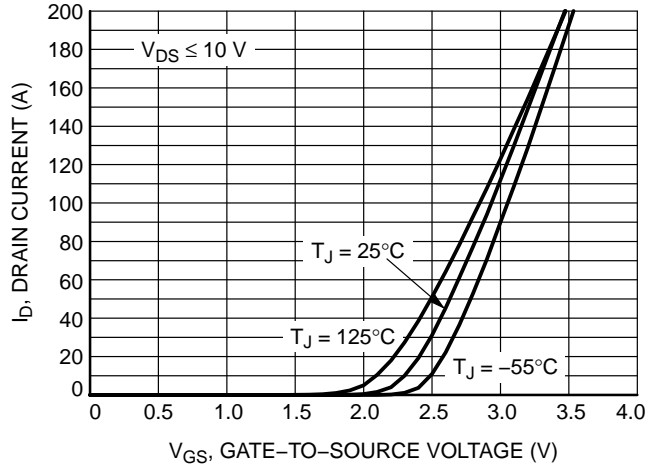## TYPICAL CHARACTERISTICS

Figure 1. On–Region Characteristics

V_{GS} = 10 V to 3.4 V

3.2 V
3.0 V
2.8 V

Figure 2. Transfer Characteristics

$V_{DS} \leq$ 10 V

T_J = 25°C
T_J = 125°C
T_J = –55°C
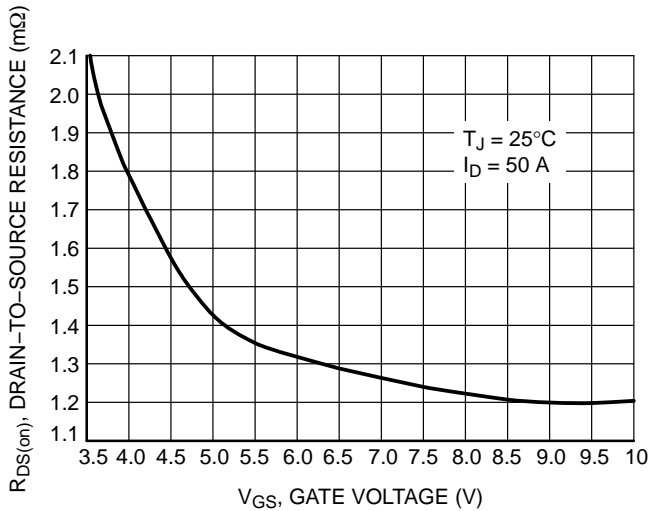
Figure 3. On–Resistance vs. Gate–to–Source Voltage

T_J = 25°C
I_D = 50 A
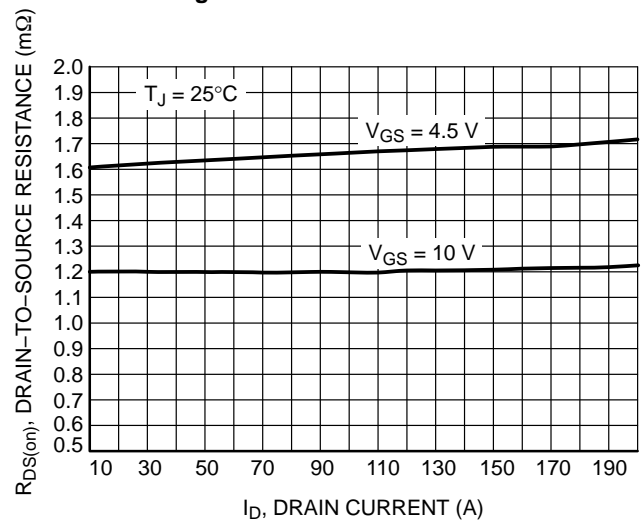
Figure 4. On–Resistance vs. Drain Current and Gate Voltage

T_J = 25°C
V_{GS} = 4.5 V
V_{GS} = 10 V
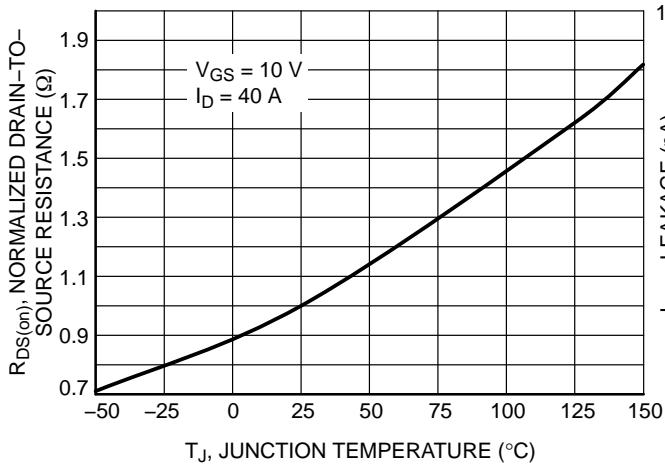
Figure 5. On–Resistance Variation with Temperature

V_{GS} = 10 V
I_D = 40 A
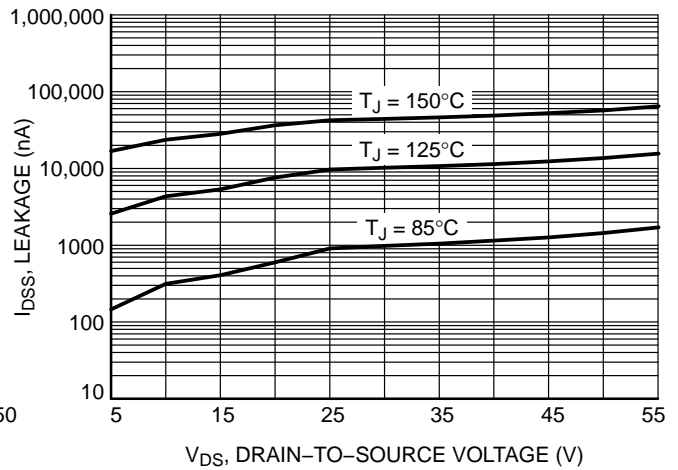
Figure 6. Drain–to–Source Leakage Current vs. Voltage

T_J = 150°C
T_J = 125°C
T_J = 85°C

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TYPICAL CHARACTERISTICS
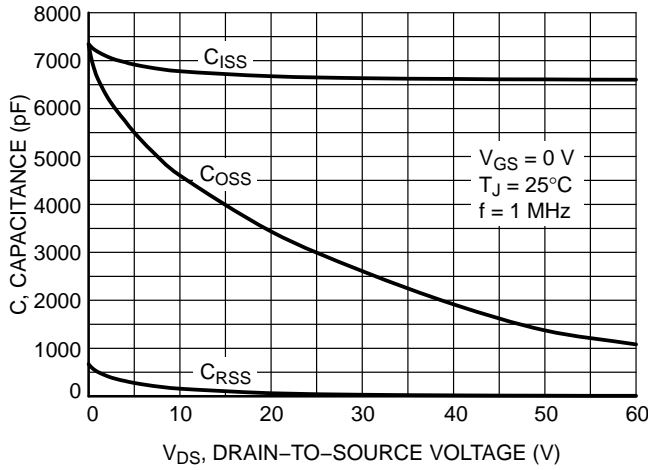
Figure 7. Capacitance Variation

$V_{GS} = 0$ V
$T_J = 25°C$
f = 1 MHz
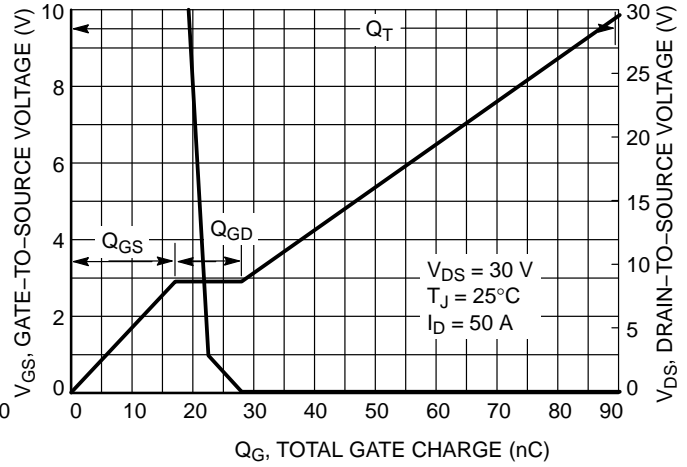
Figure 8. Gate–to–Source and Drain–to–Source Voltage vs. Total Charge

$V_{DS} = 30$ V
$T_J = 25°C$
$I_D = 50$ A

$V_{GS} = 4.5$ V
$V_{DD} = 30$ V
$I_D = 50$ A
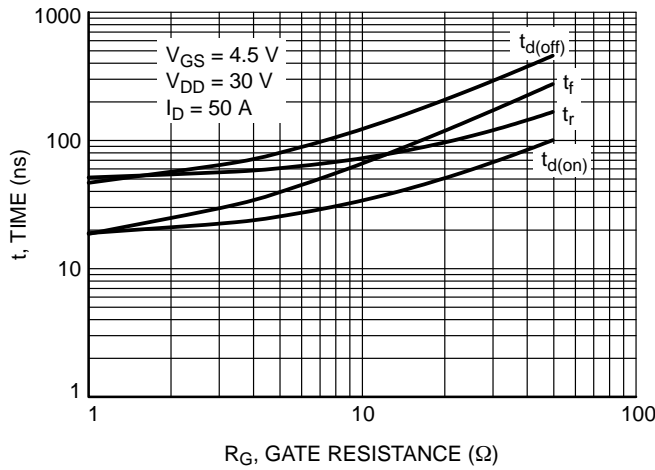
Figure 9. Resistive Switching Time Variation vs. Gate Resistance

$T_J = 125°C$
$T_J = 25°C$
$T_J = -55°C$
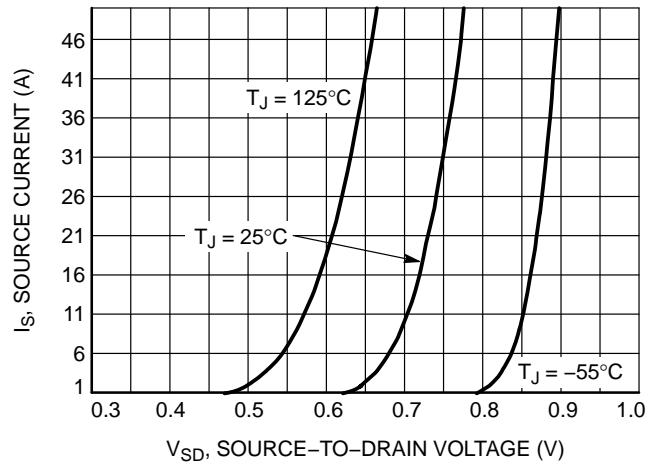
Figure 10. Diode Forward Voltage vs. Current

$T_C = 25°C$
$V_{GS} \leq 10$ V

0.01 ms
0.1 ms
1 ms
dc
10 ms

– – – $R_{DS(on)}$ Limit
——— Thermal Limit
—·—·— Package Limit
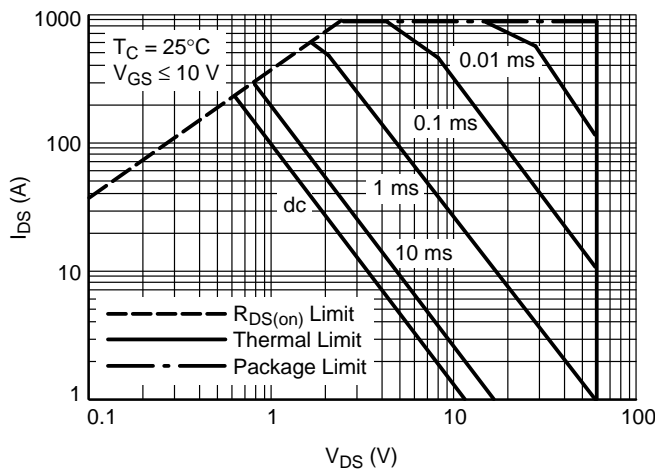
Figure 11. Safe Operating Area

$T_{J(initial)} = 25°C$
$T_{J(initial)} = 100°C$
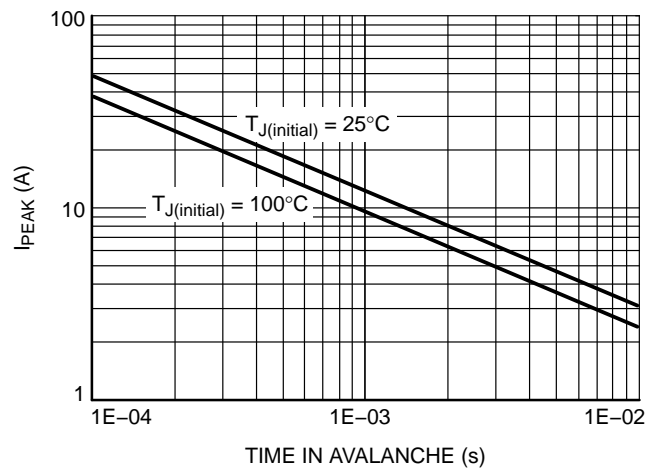
Figure 12. I_{PEAK} vs. Time in Avalanche

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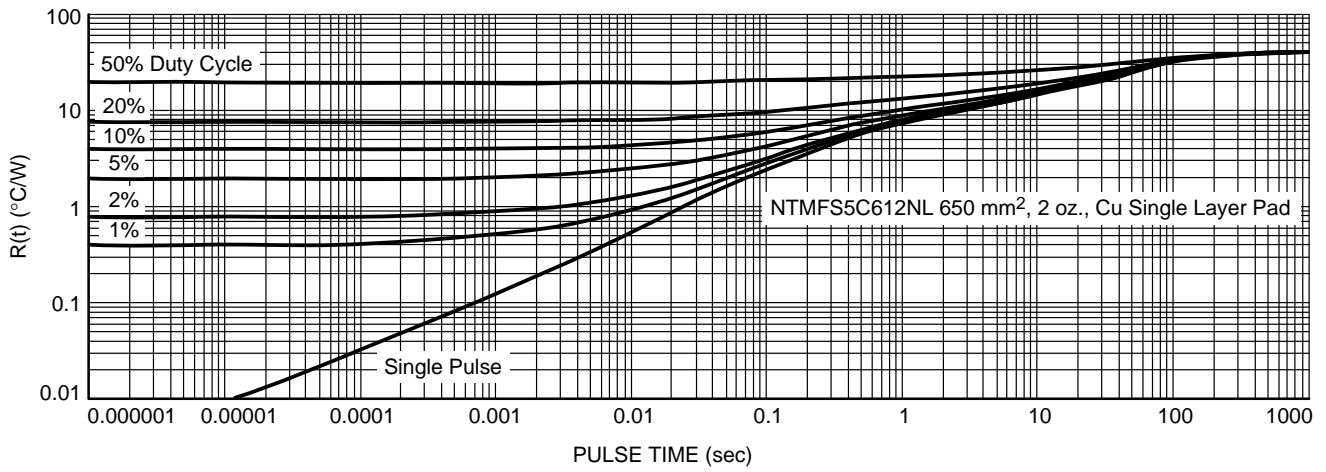
Figure 13. Thermal Characteristics

DEVICE ORDERING INFORMATION

Device	Marking	Package	Shipping†
NTMFS5C612NLT1G	5C612L	DFN5 (Pb–Free)	1500 / Tape & Reel
NTMFS5C612NLT3G	5C612L	DFN5 (Pb–Free)	5000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTMFS5C612NL

PACKAGE DIMENSIONS

DFN5 5x6, 1.27P
(SO–8FL)
CASE 488AA
ISSUE H

TOP VIEW

SIDE VIEW

DETAIL A

BOTTOM VIEW

DETAIL A

SOLDERING FOOTPRINT*

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS		
	MIN	**NOM**	**MAX**
A	0.90	1.00	1.10
A1	0.00	———	0.05
b	0.33	0.41	0.51
c	0.23	0.28	0.33
D	5.15 BSC		
D1	4.70	4.90	5.10
D2	3.80	4.00	4.20
E	6.15 BSC		
E1	5.70	5.90	6.10
E2	3.45	3.65	3.85
e	1.27 BSC		
G	0.51	0.61	0.71
K	1.20	1.35	1.50
L	0.51	0.61	0.71
L1	0.05	0.17	0.20
M	3.00	3.40	3.80
θ	0 °	———	12 °
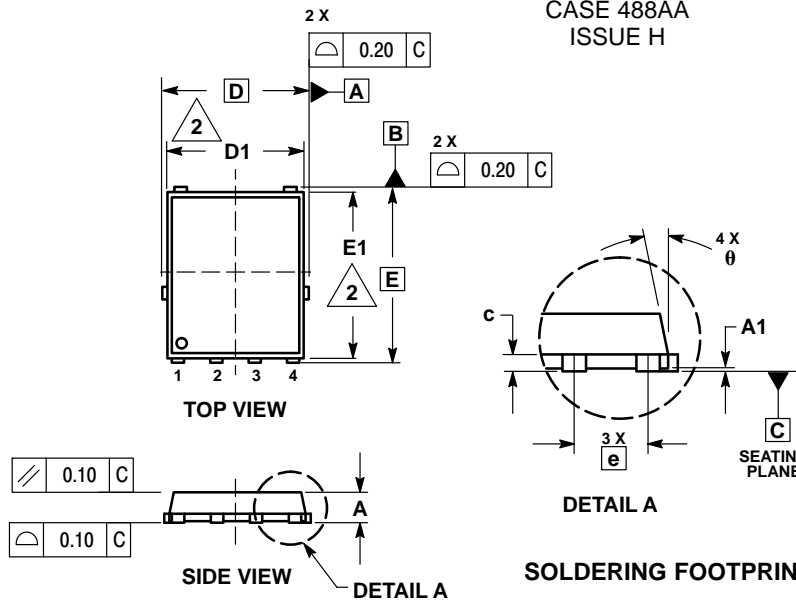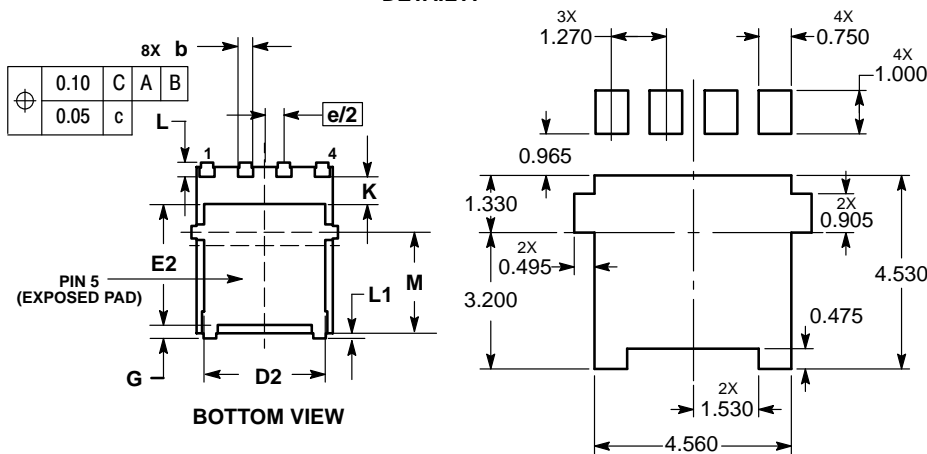
STYLE 1:
PIN 1. SOURCE
2. SOURCE
3. SOURCE
4. GATE
5. DRAIN

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NTMFS5C612NL/D