SILIKRON **SSF7504**

Feathers:

- Advanced trench process technology
- Special designed for Convertors and power controls
- High density cell design for ultra low Rdson
- Fully characterized Avalanche voltage and current
- Avalanche Energy 100% test

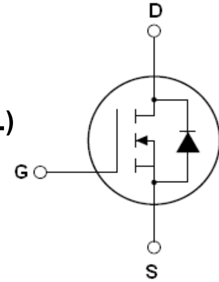
Description:

The SSF7504 is a new generation of middle voltage and high current N–Channel enhancement mode trench power MOSFET. This new technology increases the cell density and reduces the on-resistance; its typical Rdson can reduce to 2.7mohm.

Application:

- Power switching application

ID=220A
BV=75V
Rdson=2.7mΩ(typ.)



SSF7504 TOP View (TO220)

Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D@T_c=25^\circ C$	Continuous drain current,VGS@10V	220	A
$I_D@T_c=100^\circ C$	Continuous drain current,VGS@10V	170	
I_{DM}	Pulsed drain current ①	880	
$P_D@T_C=25^\circ C$	Power dissipation	370	W
	Linear derating factor	2.0	W/°C
V_{GS}	Gate-to-Source voltage	±20	V
dv/dt	Peak diode recovery voltage	20	v/ns
E_{AS}	Single pulse avalanche energy ②	960	mJ
E_{AR}	Repetitive avalanche energy	TBD	
T_J T_{STG}	Operating Junction and Storage Temperature Range	–55 to +175	°C

Thermal Resistance

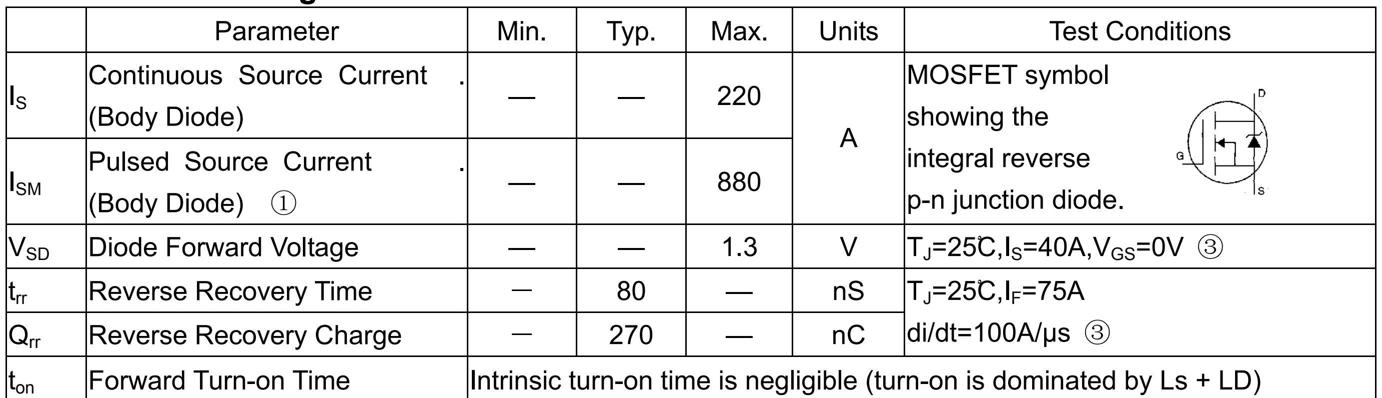
	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-case	—	0.41	—	°C/W
$R_{\theta JA}$	Junction-to-ambient	—	—	62	

Electrical Characteristics @TJ=25°C(unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Test Conditions
BV_{DSS}	Drain-to-Source breakdown voltage	75	—	—	V	$V_{GS}=0V,I_D=250\mu A$
$R_{DS(on)}$	Static Drain-to-Source on-resistance	—	2.7	4	mΩ	$V_{GS}=10V,I_D=40A$
$V_{GS(th)}$	Gate threshold voltage	2.0	3.1	4.0	V	$V_{DS}=V_{GS},I_D=250\mu A$
g_{fs}	Forward transconductance	—	65	—	S	$V_{DS}=5V,I_D=30A$
I_{DSS}	Drain-to-Source leakage current	—	—	10	μA	$V_{DS}=80V,V_{GS}=0V$
		—	—	50		$V_{DS}=80V$, $V_{GS}=0V,T_J=150^\circ C$

I_{GSS}	Gate-to-Source forward leakage	—	—	100	nA	V_{GS}=20V
	Gate-to-Source reverse leakage	—	—	-100		V_{GS}=-20V
Qg	Total gate charge	—	140	—	nC	I_D=30A
Qgs	Gate-to-Source charge	—	30	—		V_{DD}=30V
Qgd	Gate-to-Drain("Miller") charge	—	36	—		V_{GS}=10V
td(on)	Turn-on delay time	—	22	—	nS	V_{DD}=30V
tr	Rise time	—	35	—		I_D=2A ,R_L=15Ω
td(off)	Turn-Off delay time	—	77.8	—		R_G=2.5Ω
tf	Fall time	—	19.8	—		V_{GS}=10V
Ciss	Input capacitance	—	7005	—	pF	V_{GS}=0V
Coss	Output capacitance	—	600	—		V_{DS}=25V
Crss	Reverse transfer capacitance	—	280	—		f=1.0MHZ

Source-Drain Ratings and Characteristics



	Parameter	Min.	Typ.	Max.	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	220	A	MOSFET symbol showing the integral reverse p-n junction diode.
I_{SM}	Pulsed Source Current (Body Diode) ①	—	—	880		
V_{SD}	Diode Forward Voltage	—	—	1.3	V	T_J=25℃,I_S=40A,V_{GS}=0V ③
t_{rr}	Reverse Recovery Time	—	80	—	nS	T_J=25℃,I_F=75A di/dt=100A/μs ③
Q_{rr}	Reverse Recovery Charge	—	270	—	nC	
t_{on}	Forward Turn-on Time	Intrinsic turn-on time is negligible (turn-on is dominated by Ls + LD)				

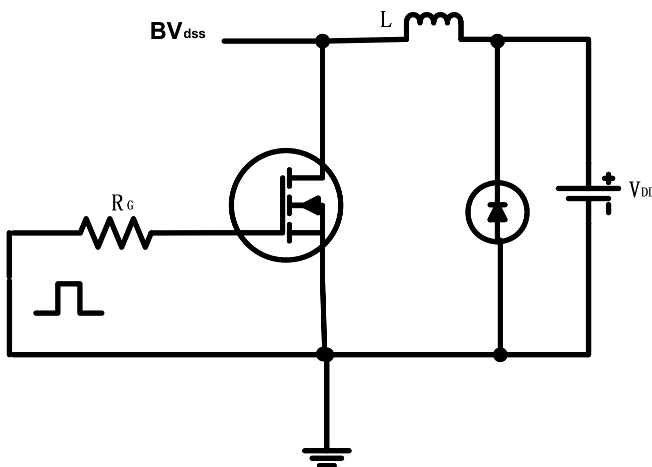
Notes:

① Repetitive rating; pulse width limited by max junction temperature.

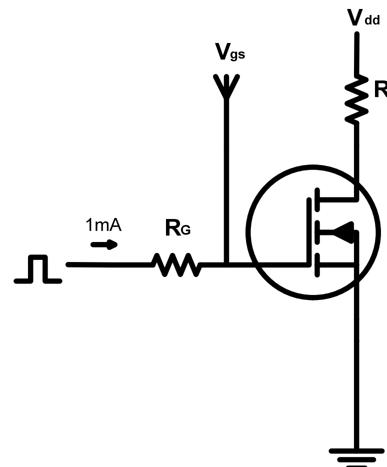
② Test condition: L =0.3mH, ID = 80A, VDD = 37.5V

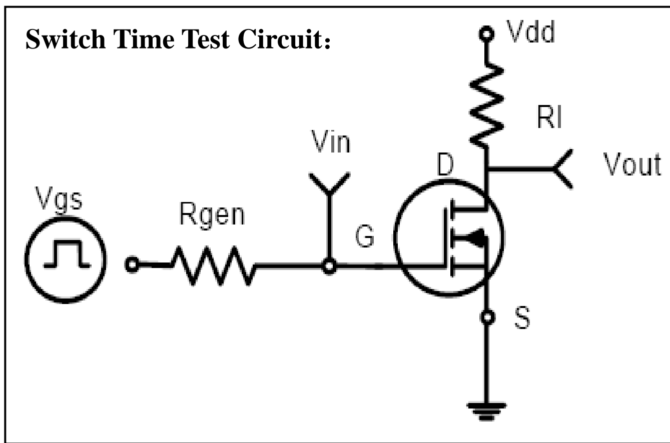
③ Pulse width≤300μS; duty cycle≤1.5% RG = 25ΩStarting TJ = 25°C

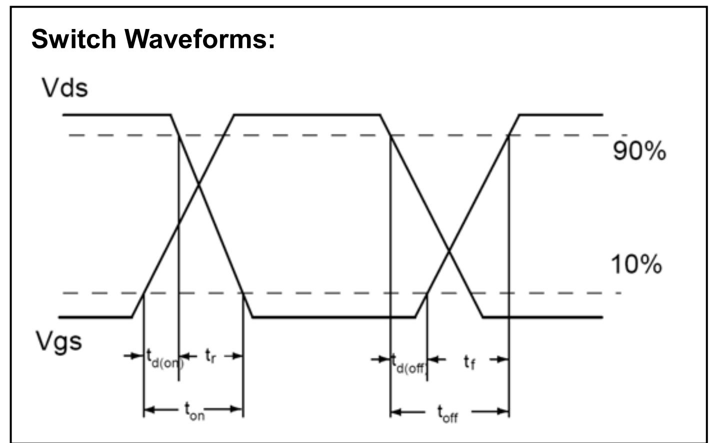
EAS test circuits:



Gate charge test circuit:







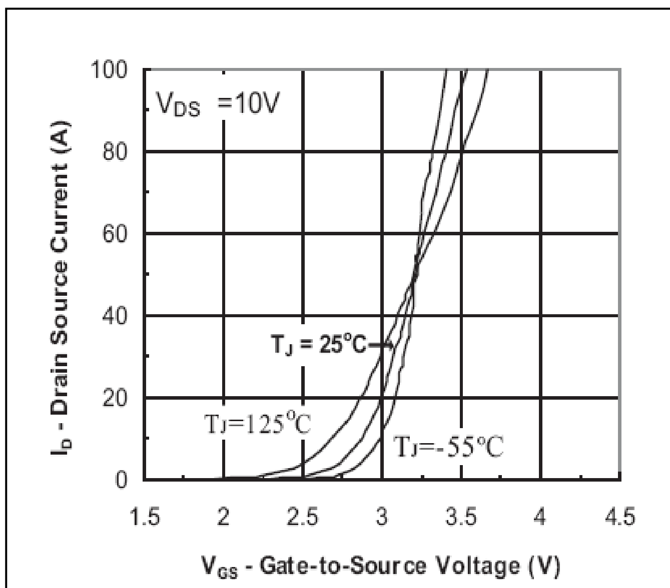


Figure1:Transfer Characteristic

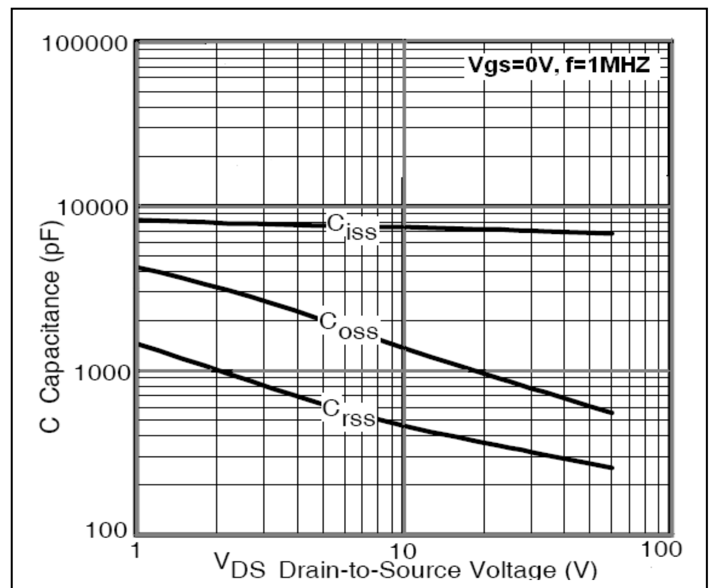


Figure2:Capacitance

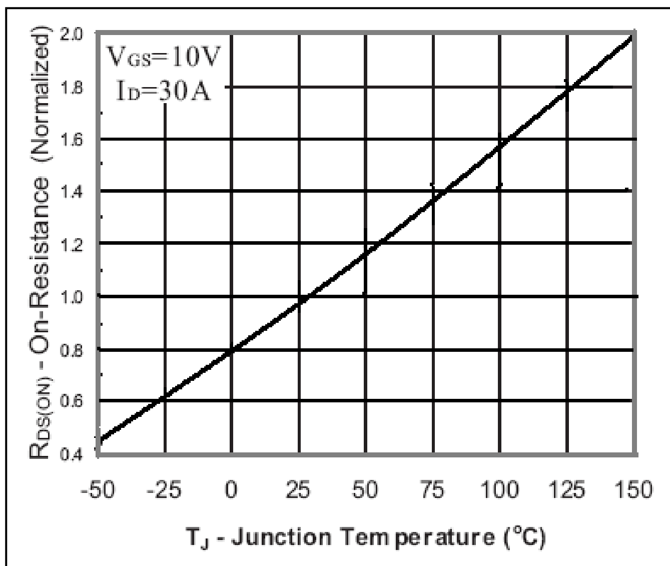


Figure3:On Resistance vs Junction Temperature

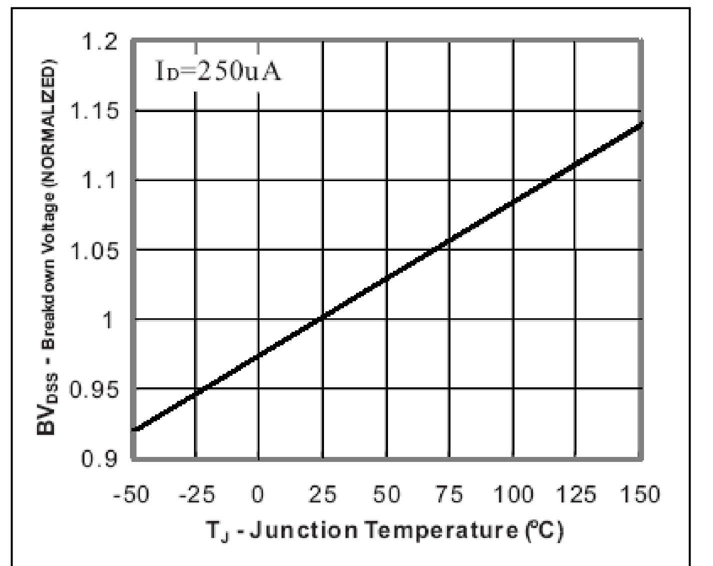


Figure4:Breakdown Voltage vs Junction Temperature

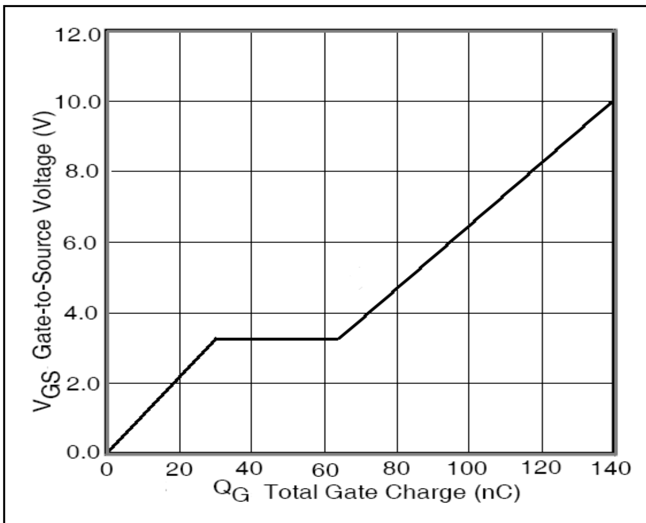


Figure5:Gate Charge

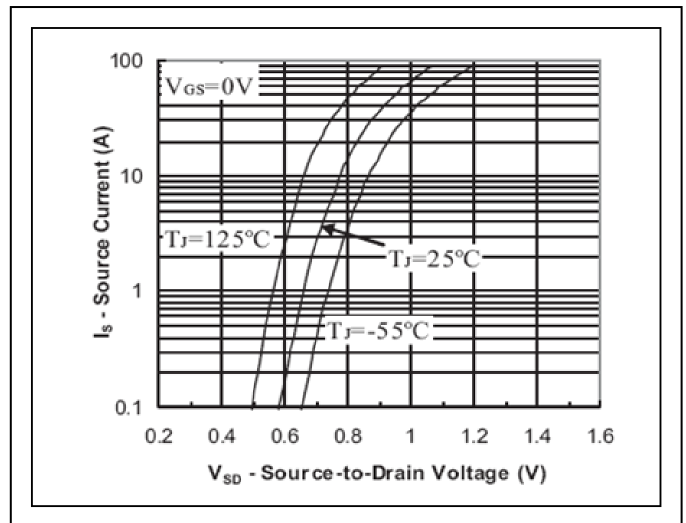


Figure6:Source-Drain Diode Forward Voltage

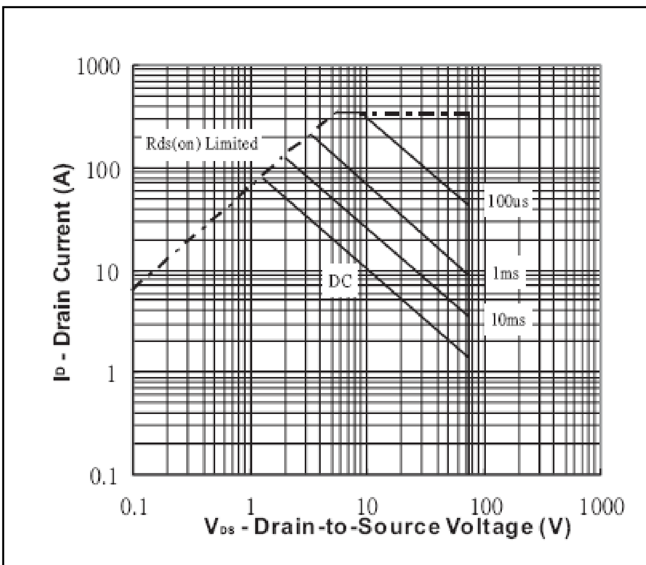


Figure7:Safe Operation Area

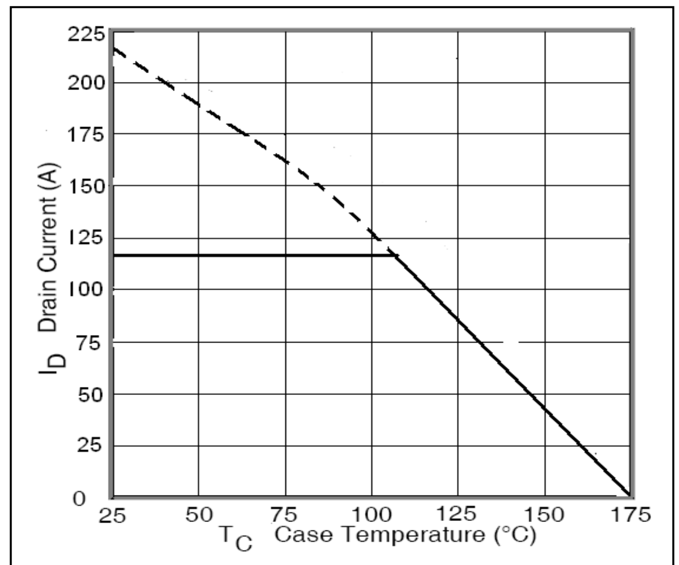


Figure8:Max Drain Current vs Junction Temperature

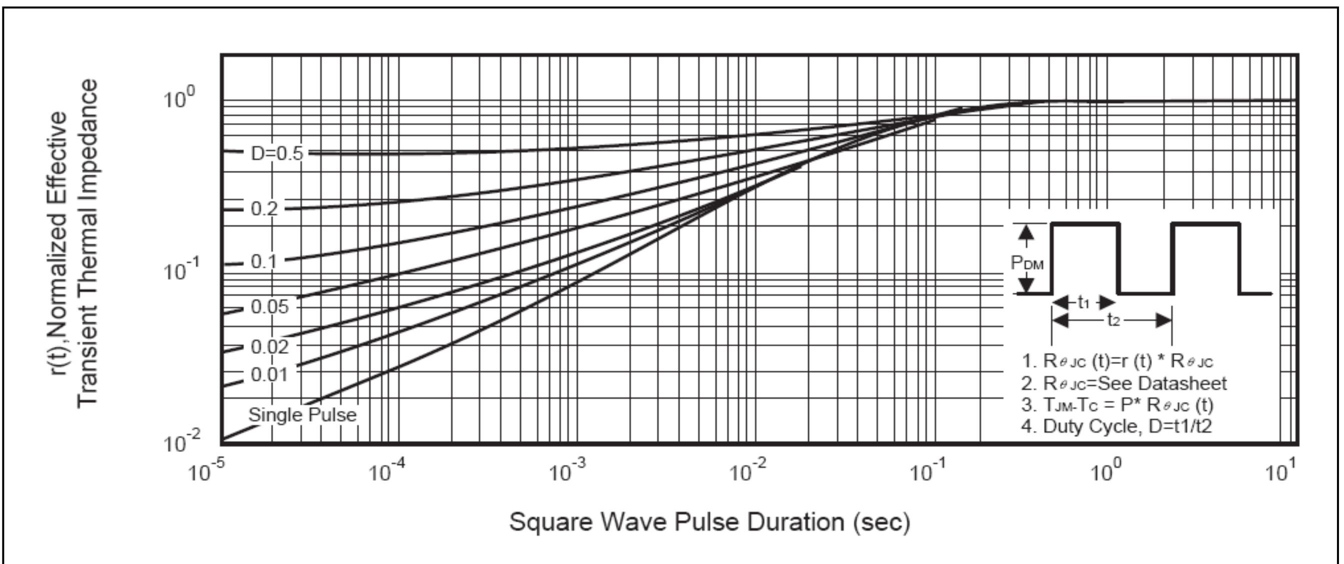


Figure9:Transient Thermal Impedance Curve

TO220 MECHANICAL DATA: