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Highly–Integrated, Fully–Featured 12–port DS3/E3/STS–1 Jitter–Attenuator and STS–1 to DS3/E3 Desynchronizer

M28320 Digital Jitter–Attenuator (DJAT)

Mindspeed Technologies™ offers its first 12–port DS3/E3/STS–1 Jitter–Attenuator and desynchronizer based on DJAT technology

Mindspeed's DJAT technology performs critical jitter-attenuation and signal desynchronization functions to improve performance and reliability in both telecommunciations and data communications equipment surrounding the edge of the optical network.

This high density, low power solution is designed for transmission applications including add/drop multiplexers, routers, ATM multi-service switches, digital cross connects, and DS3 to STS-1 mappers. The M28320 12-port DJAT device can be combined with Line Interface Units (LIUs) and mapper devices in addressing traffic-aggregation equipment needs in converting high-speed Synchronous Transport Signal-1 (STS-1) streams to asynchronous lower-speed DS3/E3 data rates for systems used in data centers and points of presence (POPs).

The 12-port M28320 DJAT leverages Mindspeed's advance digital signal processing techniques along, with extensive knowledge of analog mixed signal design, that provide the first solution of its kind to adapt and fully smooth a STS-1 clock (with overhead gaps) to a network compliant DS3 or E3 line clock.

The M28320 12-port DJAT complies with Telcordia GR-253 and GR-499, ETSI TBR-24, ANSI T1.105.03b, as well as ITU G.751, G.755, G.783, and G.823 standards. For Category I interfaces, the M28320 12-port DJAT device smooths the inherent jitter due to demapping, bit stuffing and pointer adjustments in DS3 or E3 payloads extracted from STS-1

KEY FEATURES

- High density: up to 12 independent jitter-attenuators and desynchronizers for DS3/E3, and STS-1 in one package
- Low power: <350 mW maximum power consumption
- Programmable FIFO depth optimal for SONET/SDH
- Crystal-less jitter-attenuation
- Programmable clocking of both inputs and outputs on either edge
- Two PRBS generator/detector per channel
- One second timer for event latching
- Ability to dejitter AMI or NRZ input data
- Ability to independently bypass the JAT for each channel
- Power-down control for each channel
- Small 15 mm BGA package
- Single 3.3 V supply

frames, generating a network compliant clock. The M28320 12-port DJAT seamlessly interfaces with Mindspeed's DS3/E3/STS-1 LIU devices — M28331/2/3 (1/2/3-port), M28335 (12-port), and CX28365 (12-port DS3/E3 framer with ATM TC) — providing a complete solution for high density DS3/E3 line cards.

Jitter Definition

Jitter is defined as the short-term variations of the significant instants of any signal from their ideal position in time. The short-term variations are phase oscillations of the digital signal. Clock jitter can lead to incorrect data bit sampling, resulting in bit errors.

Jitter can be caused by any or all of the following:

- Interference
- Oscillator phase noise
- Signal distortion
- Stuffing jitter
- Demapping jitter
- Pointer jitter

Jitter–Attenuator and Desynchronizer

Jitter-attenuator (JAT) smooths the phase differences of clock signals due to phase variations between STRATUM clocks, bit stuffing, pointer adjustments due to frequency differences, and demapping of STS-1 payloads. There are two modes of operation for the M28320 12-port DJAT. The first involves attenuating jitter from a clock signal of E3, DS3, or STS-1 data rates. This is typically referred to as a Category II interface. Clock jitter on this interface is also referred to as line timing jitter. The second mode of operation, for a Category I interface, involves extracting an E3 or DS3 payload from a STS-1 frame. Clock jitter on this interface is also referred to as demapping jitter.

Microprocessor Interface

In hardware mode, the M28320 12-port device requires little or no control and may be statically configured. The M28320 12-port device also supports a 4 signal serial and a parallel 8-bit micro-processor interface that allows access to extended features such as the PRBS generators and bit error rate (BER) counters. Control and status registers are memory mapped.
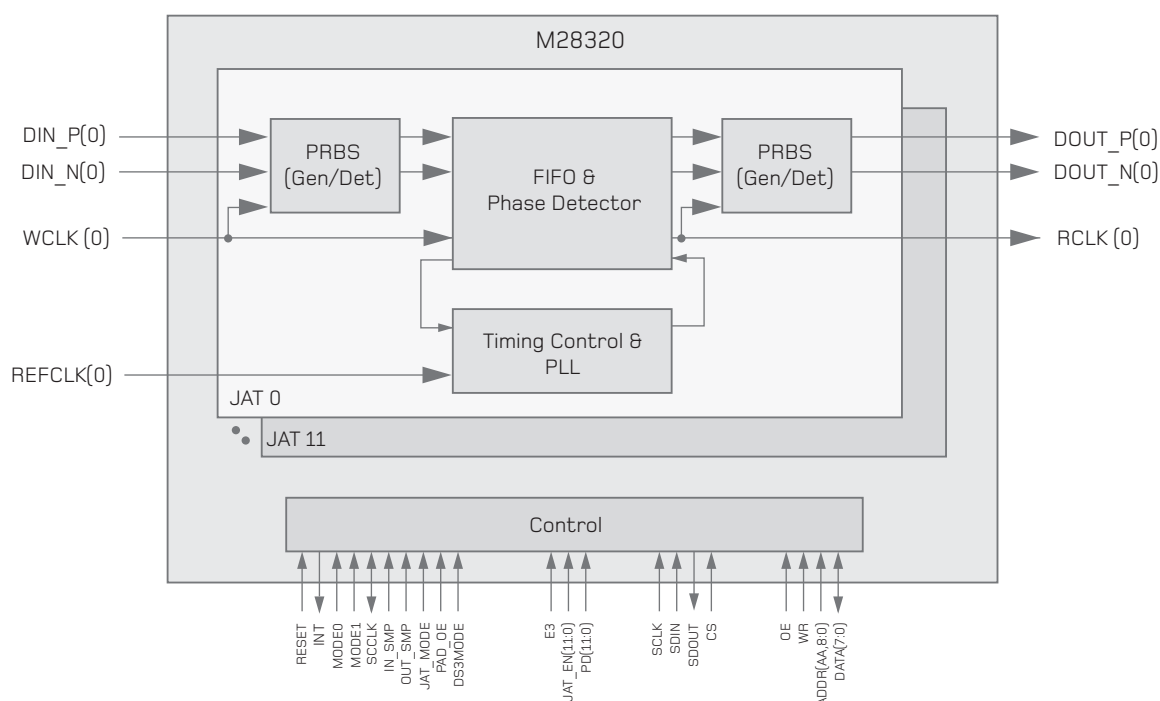
Functional Block Diagram

Product Features

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Applications

- **Digital Cross-connect systems**
- **Multi-service ATM switches**
- **Routers**
- **Add/drop Multiplexers**