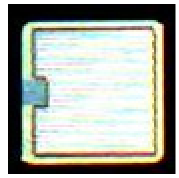
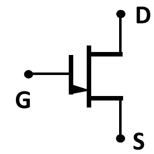
Normally – OFF Silicon Carbide Junction Transistor

V_{DS}	=	600 V
$R_{DS(ON)}$	=	120 mΩ
I_D (Tc = 25°C)	=	25 A
$h_{FE(Tc = 25°C)}$	=	120

Features

- 250°C maximum operating temperature
- Gate Oxide Free SiC switch
- Exceptional Safe Operating Area
- Excellent Gain Linearity
- Temperature Independent Switching Performance
- Low Output Capacitance
- Positive Temperature Co-efficient of $R_{DS,ON}$
- Suitable for connecting an anti-parallel diode





Advantages

- Compatible with Si MOSFET/IGBT gate-drivers
- > 20 µs Short-Withstand Capability
- Lowest-in-class Conduction Losses
- High Circuit Efficiency
- Minimal Input Signal Distortion
- High Amplifier Bandwidth

Applications

- Down Hole Oil Drilling, Geothermal Instrumentation
- Hybrid Electric Vehicles (HEV)
- Solar Inverters
- Switched-Mode Power Supply (SMPS)
- Power Factor Correction (PFC)
- Induction Heating
- Uninterruptible Power Supply (UPS)
- Motor Drives

Absolute Maximum Ratings

Parameter	Symbol	Conditions	Value	Unit	Notes
Drain – Source Voltage	V_{DS}	V_{GS} = 0 V	600	V	
Continuous Drain Current	I_D	T_C = 25°C	25	A	
Continuous Gate Current	I_{GM}		3	A	
Turn-Off Safe Operating Area	RBSOA	T_{VJ} = 250 °C, I_G = 1 A, Clamped Inductive Load	$I_{D,max}$ = 10 @ $V_{DS} \leq V_{DSmax}$	A	
Short Circuit Safe Operating Area	SCSOA	T_{VJ} = 225 °C, I_G = 2.5 A, V_{DS} = 400 V, Non Repetitive	> 20	µs	
Reverse Gate – Source Voltage	V_{SG}		30	V	
Reverse Drain – Source Voltage	V_{SD}		25	V	
Storage Temperature	T_{stg}		-55 to 250	°C	

Electrical Characteristics

Parameter	Symbol	Conditions	Value Min.	Value Typical	Value Max.	Unit	Notes
On State Characteristics							
Drain – Source On Resistance	$R_{DS(ON)}$	I_D = 10 A, T_j = 25 °C I_D = 10 A, T_j = 125 °C I_D = 10 A, T_j = 175 °C I_D = 10 A, T_j = 225 °C		120 180 240 320		mΩ	Fig. 5
Gate Forward Voltage	$V_{GS(FWD)}$	I_G = 500 mA, T_j = 25 °C I_G = 500 mA, T_j = 225 °C		2.95 2.63		V	Fig. 4
DC Current Gain	β	V_{DS} = 5 V, I_D = 10 A, T_j = 25 °C V_{DS} = 5 V, I_D = 10 A, T_j = 125 °C V_{DS} = 5 V, I_D = 10 A, T_j = 175 °C V_{DS} = 10 V, I_D = 10 A, T_j = 225 °C		123 87 80 76		–	Fig. 5
Off State Characteristics							
Drain Leakage Current	I_{DSS}	V_R = 600 V, V_{GS} = 0 V, T_j = 25 °C V_R = 600 V, V_{GS} = 0 V, T_j = 125 °C V_R = 600 V, V_{GS} = 0 V, T_j = 225 °C		10 50 100		µA	Fig. 6
Gate Leakage Current	I_{SG}	V_{SG} = 20 V, T_j = 25 °C		20		nA	

Figures

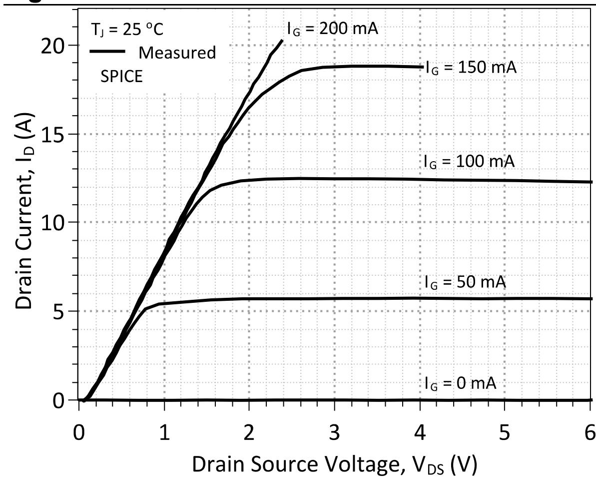


Figure 1: Typical Output Characteristics at 25 °C

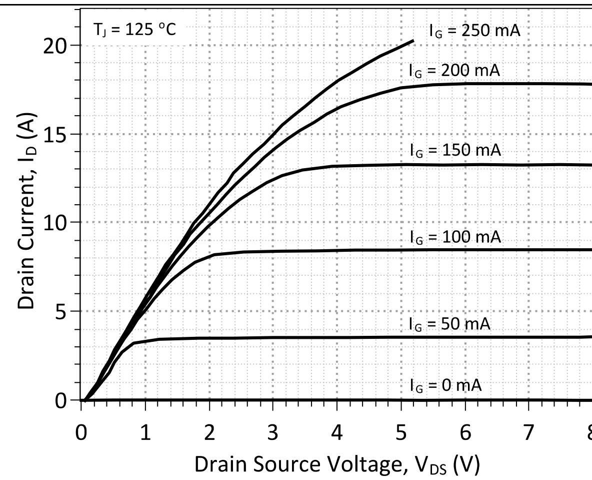


Figure 2: Typical Output Characteristics at 125 °C

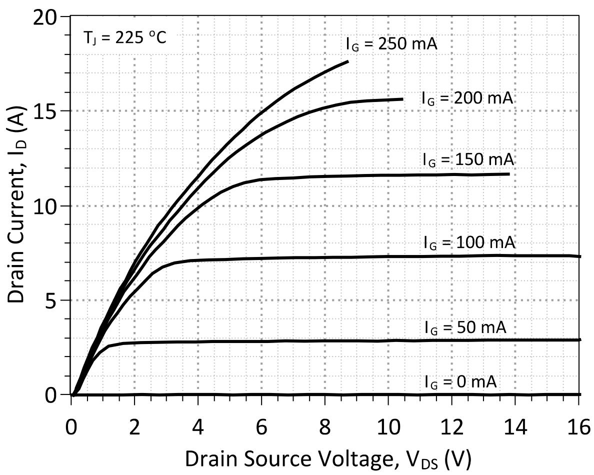


Figure 3: Typical Output Characteristics at 225 °C

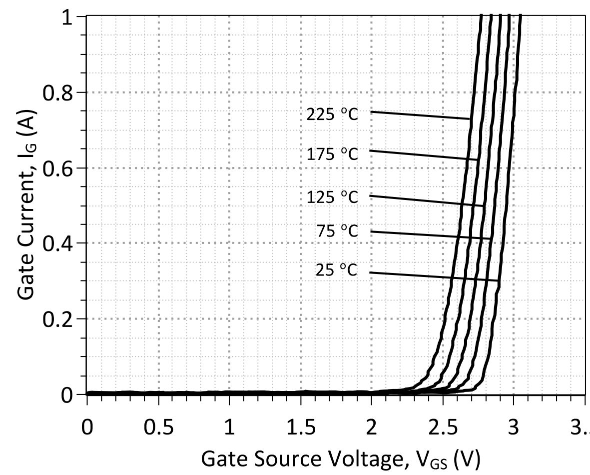


Figure 4: Typical Gate Source I-V Characteristics vs. Temperature

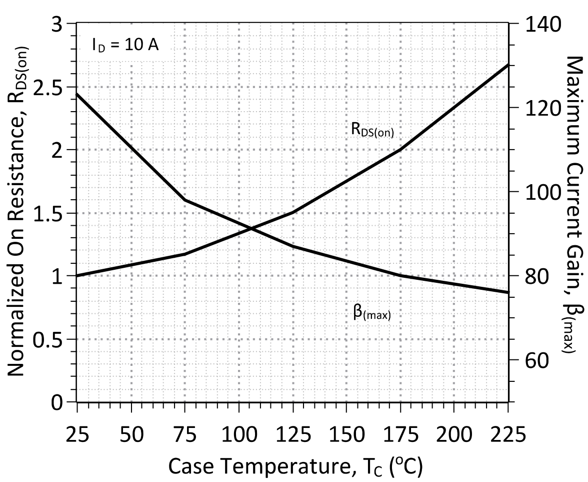


Figure 5: Normalized On-Resistance and Current Gain vs. Temperature

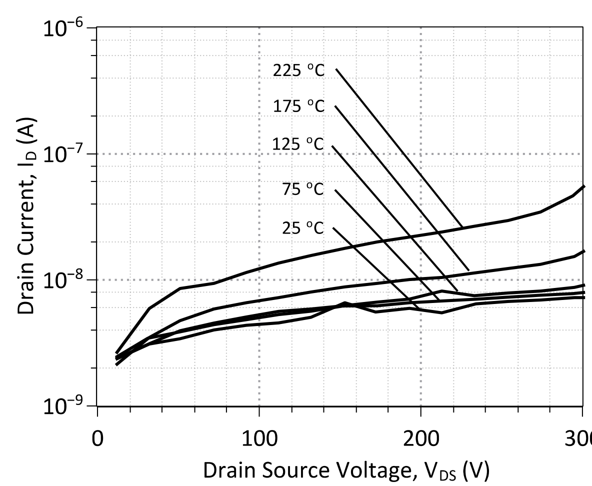


Figure 6: Typical Blocking Characteristics

Gate Drive Theory of Operation

The SJT transistor is a current controlled transistor which requires a positive gate current for turn-on as well as to remain in on-state. An ideal gate current waveform for ultra-fast switching of the SJT, while maintaining low gate drive losses, is shown in Figure 9.

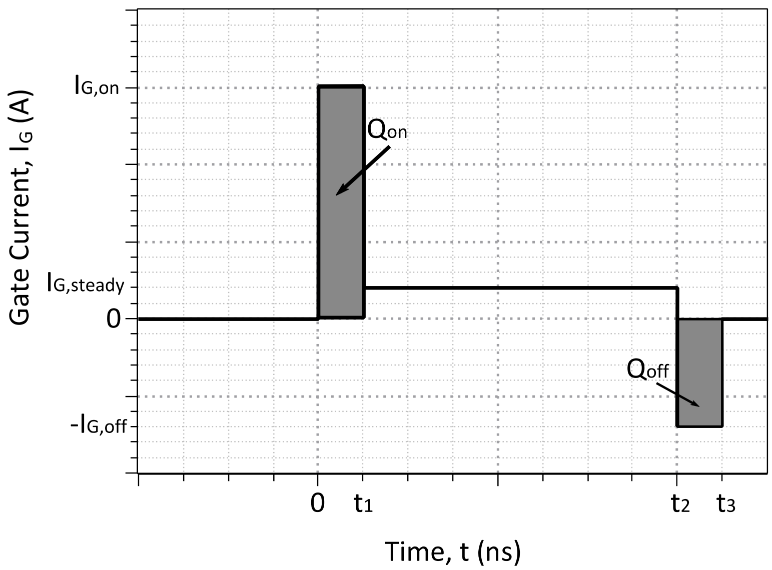


Figure 9: Idealized Gate Current Waveform

Gate Currents, $I_{G,pk}$/-$I_{G,pk}$ and Voltages during Turn-On and Turn-Off

An SJT is rapidly switched from its blocking state to on-state, when the necessary gate charge, Q_G, for turn-on is supplied by a burst of high gate current, $I_{G,on}$, until the gate-source capacitance, C_{GS}, and gate-drain capacitance, C_{GD}, are fully charged.

$$I_{G,on} * t_1 \geq Q_{gs} + Q_{gd}$$

The $I_{G,pon}$ pulse should ideally terminate, when the drain voltage falls to its on-state value, in order to avoid unnecessary drive losses during the steady on-state. In practice, the rise time of the $I_{G,on}$ pulse is affected by the parasitic inductances, L_{par} in the package and drive circuit. A voltage developed across the parasitic inductance in the source path, L_s, can de-bias the gate-source junction, when high drain currents begin to flow through the device. The applied gate voltage should be maintained high enough, above the $V_{GS,ON}$ level to counter these effects.

A high negative peak current, -$I_{G,off}$ is recommended at the start of the turn-off transition, in order to rapidly sweep out the injected carriers from the gate, and achieve rapid turn-off. While satisfactory turn off can be achieved with V_{GS} = 0 V, a negative gate voltage V_{GS} may be used in order to speed up the turn-off transition.

Steady On-State

After the device is turned on, I_G may be advantageously lowered to $I_{G,steady}$ for reducing unnecessary gate drive losses. The $I_{G,steady}$ is determined by noting the DC current gain, h_{FE}, of the device

The desired $I_{G,steady}$ is determined by the peak device junction temperature T_J during operation, drain current I_D, DC current gain h_{FE}, and a 50 % safety margin to ensure operating the device in the saturation region with low on-state voltage drop by the equation:

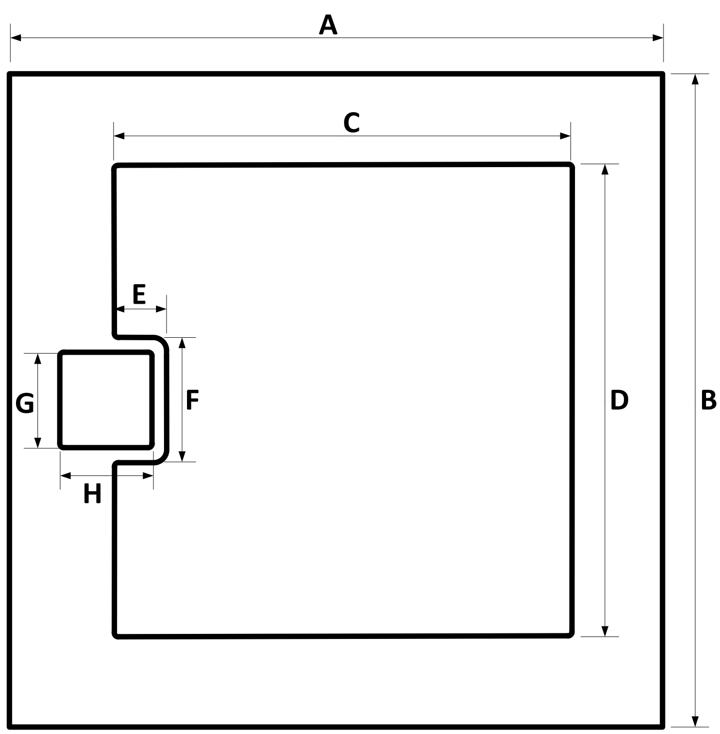
$$I_{G,steady} \approx \frac{I_D}{h_{FE}(T, I_D)} * 1.5$$

Mechanical Specifications

Mechanical Parameters

Raster Size	2.10 x 2.10	mm^2	83 x 83	mil^2
Area total / active	4.41/3.31	mm^2	6836/5134	mil^2
Thickness	360	µm	14	mil
Wafer Size	100	mm	3937	mil
Flat Position	0	deg	0	deg
Passivation frontside	Polyimide			
Pad Metal (Anode)	4000 nm Al			
Backside Metal (Cathode)	400 nm Ni + 200 nm Au -system			
Die Bond	Electrically conductive glue or solder			
Wire Bond	Al ≤ 10 mil (Source) Al ≤ 3 mil (Gate)			
Reject ink dot size	Φ ≥ 0.3 mm			
Recommended storage environment	Store in original container, in dry nitrogen, < 6 months at an ambient temperature of 23 °C			

Chip Dimensions:



		mm	mil
DIE	A	2.10	83
	B	2.10	83
SOURCE WIREBONDABLE	C	1.47	58
	D	1.52	60
	E	0.17	7
	F	0.40	16
GATE WIREBONDABLE	G	0.30	12
	H	0.30	12

Revision History			
Date	Revision	Comments	Supersedes
2014/08/26	1	Initial Release	

Published by
GeneSiC Semiconductor, Inc.
43670 Trade Center Place Suite 155
Dulles, VA 20166

SPICE Model Parameters

This is a secure document. Please copy this code from the SPICE model PDF file on our website (http://www.genesicsemi.com/images/hit_sic/baredie/sjt/GA10JT06-CAL_SPICE.pdf) into LTSPICE (version 4) software for simulation of the GA10JT06-CAL.

```
*     MODEL OF GeneSiC Semiconductor Inc.
*
*     $Revision:   2.0           $
*     $Date:   26-AUG-2014       $
*
*     GeneSiC Semiconductor Inc.
*     43670 Trade Center Place Ste. 155
*     Dulles, VA 20166
*
*     COPYRIGHT (C) 2014 GeneSiC Semiconductor Inc.
*     ALL RIGHTS RESERVED
*
* These models are provided "AS IS, WHERE IS, AND WITH NO WARRANTY
* OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUT NOT LIMITED
* TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A
* PARTICULAR PURPOSE."
* Models accurate up to 2 times rated drain current.
*
.model GA10JT06 NPN
+ IS        4.4E-48
+ ISE       1.858E-28
+ EG        3.23
+ BF        125
+ BR        0.55
+ IKF       400
+ NF        1
+ NE        2
+ RB        7.0
+ RE        0.005
+ RC        0.105
+ CJC       3.96E-10
+ VJC       3.189
+ MJC       0.469
+ CJE       8.083E-10
+ VJE       3.1441
+ MJE       0.4308
+ XTI       3
+ XTB       -0.9
+ TRC1      1.0E-2
+ VCEO      600
+ ICRATING  10
+ MFG       GeneSiC_Semiconductor
*
* End of GA10JT06 SPICE Model
```