# IRLR3915
# IRLU3915

**KERSEMI ELECTRONIC CO.,LTD.**

## Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax

## Description

Specifically designed for Automotive applications, thi Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this product are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in Automotive applications and a wide variety of other applications.

D-Pak
IRLR3915

I-Pak
IRLU3915
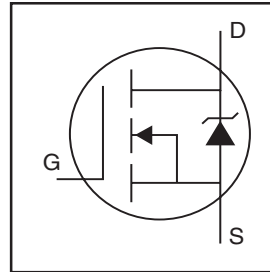
$V_{DSS} = 55V$
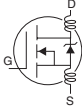
$R_{DS(on)} = 14m\Omega$

$I_D = 30A$

## Absolute Maximum Ratings

| | Parameter | Max. | Units |
|---|---|---|---|
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Silicon limited) | 61 | A |
| $I_D$ @ $T_C$ = 100°C | Continuous Drain Current, $V_{GS}$ @ 10V (See Fig.9) | 43 | |
| $I_D$ @ $T_C$ = 25°C | Continuous Drain Current, $V_{GS}$ @ 10V (Package limited) | 30 | |
| $I_{DM}$ | Pulsed Drain Current ① | 240 | |
| $P_D$ @$T_C$ = 25°C | Power Dissipation | 120 | W |
| | Linear Derating Factor | 0.77 | W/°C |
| $V_{GS}$ | Gate-to-Source Voltage | ± 16 | V |
| $E_{AS}$ | Single Pulse Avalanche Energy② | 200 | mJ |
| $E_{AS}$ (6 sigma) | Single Pulse Avalanche Energy Tested Value⑦ | 600 | |
| $I_{AR}$ | Avalanche Current① | See Fig.12a, 12b, 15, 16 | A |
| $E_{AR}$ | Repetitive Avalanche Energy⑥ | | mJ |
| $T_J$ | Operating Junction and | -55 to + 175 | |
| $T_{STG}$ | Storage Temperature Range | | °C |
| | Soldering Temperature, for 10 seconds | 300 (1.6mm from case ) | |
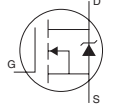
## Thermal Resistance

| | Parameter | Typ. | Max. | Units |
|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case | —— | 1.3 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient (PCB mount)⑧ | —— | 50 | |
| $R_{\theta JA}$ | Junction-to-Ambient—— | 110 | | |

# IRLR/U3915

## Electrical Characteristics @ $T_J$ = 25°C (unless otherwise specified)

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $V_{(BR)DSS}$ | Drain-to-Source Breakdown Voltage | 55 | —— | —— | V | $V_{GS}$ = 0V, $I_D$ = 250μA |
| $\Delta V_{(BR)DSS}/\Delta T_J$ | Breakdown Voltage Temp. Coefficient | —— | 0.057 | —— | V/°C | Reference to 25°C, $I_D$ = 1mA |
| $R_{DS(on)}$ | Static Drain-to-Source On-Resistance | —— | 12 | 14 | mΩ | $V_{GS}$ = 10V, $I_D$ = 30A ④ |
| | | —— | 14 | 17 | | $V_{GS}$ = 5.0V, $I_D$ = 26A ④ |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1.0 | —— | 3.0 | V | $V_{DS}$ = 10V, $I_D$ = 250μA |
| $g_{fs}$ | Forward Transconductance | 42 | —— | —— | S | $V_{DS}$ = 25V, $I_D$ = 30A |
| $I_{DSS}$ | Drain-to-Source Leakage Current | —— | —— | 20 | μA | $V_{DS}$ = 55V, $V_{GS}$ = 0V |
| | | —— | —— | 250 | | $V_{DS}$ = 55V, $V_{GS}$ = 0V, $T_J$ = 125°C |
| $I_{GSS}$ | Gate-to-Source Forward Leakage | —— | —— | 200 | nA | $V_{GS}$ = 16V |
| | Gate-to-Source Reverse Leakage | —— | —— | -200 | | $V_{GS}$ = -16V |
| $Q_g$ | Total Gate Charge | —— | 61 | 92 | | $I_D$ = 30A |
| $Q_{gs}$ | Gate-to-Source Charge | —— | 9.0 | 14 | nC | $V_{DS}$ = 44V |
| $Q_{gd}$ | Gate-to-Drain ("Miller") Charge | —— | 17 | 25 | | $V_{GS}$ = 10V④ |
| $t_{d(on)}$ | Turn-On Delay Time | —— | 7.4 | —— | ns | $V_{DD}$ = 28V |
| $t_r$ | Rise Time | —— | 51 | —— | | $I_D$ = 30A |
| $t_{d(off)}$ | Turn-Off Delay Time | —— | 83 | —— | | $R_G$ = 8.5Ω |
| $t_f$ | Fall Time | —— | 100 | —— | | $V_{GS}$ = 10V ④ |
| $L_D$ | Internal Drain Inductance | —— | 4.5 | —— | nH | Between lead, 6mm (0.25in.) from package and center of die contact |
| $L_S$ | Internal Source Inductance | —— | 7.5 | —— | | |
| $C_{iss}$ | Input Capacitance | —— | 1870 | —— | | $V_{GS}$ = 0V |
| $C_{oss}$ | Output Capacitance | —— | 390 | —— | | $V_{DS}$ = 25V |
| $C_{rss}$ | Reverse Transfer Capacitance | —— | 74 | —— | pF | $f$ = 1.0MHz, See Fig. 5 |
| $C_{oss}$ | Output Capacitance | —— | 2380 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 1.0V, $f$ = 1.0MHz |
| $C_{oss}$ | Output Capacitance | —— | 290 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 44V, $f$ = 1.0MHz |
| $C_{oss}$ eff. | Effective Output Capacitance ⑤ | —— | 540 | —— | | $V_{GS}$ = 0V, $V_{DS}$ = 0V to 44V |

## Source-Drain Ratings and Characteristics

| | Parameter | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| $I_S$ | Continuous Source Current (Body Diode) | —— | —— | 61 | A | MOSFET symbol showing the integral reverse p-n junction diode. |
| $I_{SM}$ | Pulsed Source Current (Body Diode) ① | —— | —— | 240 | | |
| $V_{SD}$ | Diode Forward Voltage | —— | —— | 1.3 | V | $T_J$ = 25°C, $I_S$ = 30A, $V_{GS}$ = 0V ④ |
| $t_{rr}$ | Reverse Recovery Time | —— | 62 | 93 | ns | $T_J$ = 25°C, $I_F$ = 30A, $V_{DD}$ = 25xjkl V |
| $Q_{rr}$ | Reverse Recovery Charge | —— | 110 | 170 | nC | di/dt = 100A/μs ④ |
| $t_{on}$ | Forward Turn-On Time | | | | | Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$) |
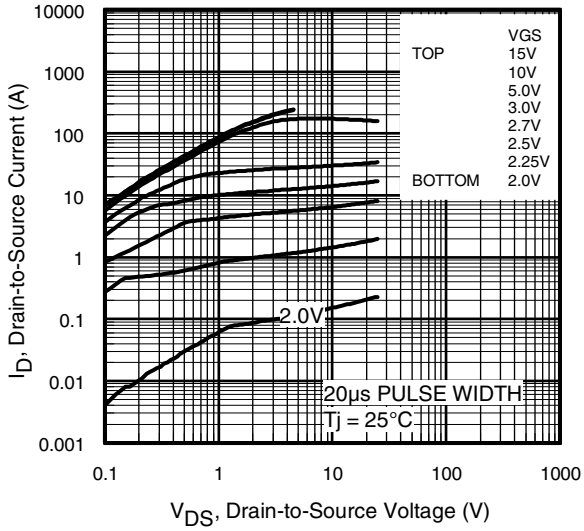
**Fig 1.** Typical Output Characteristics
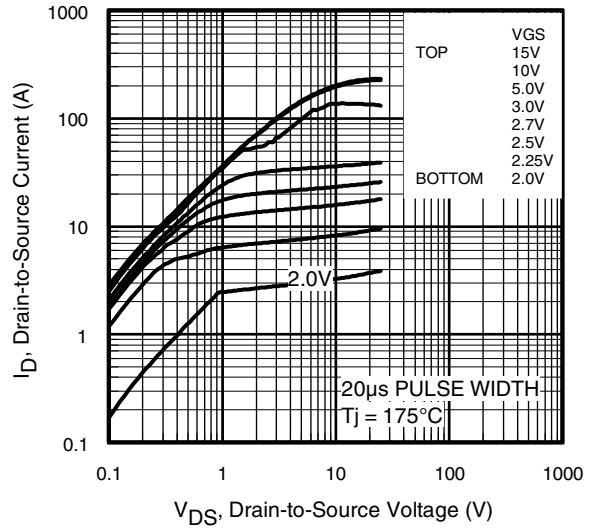


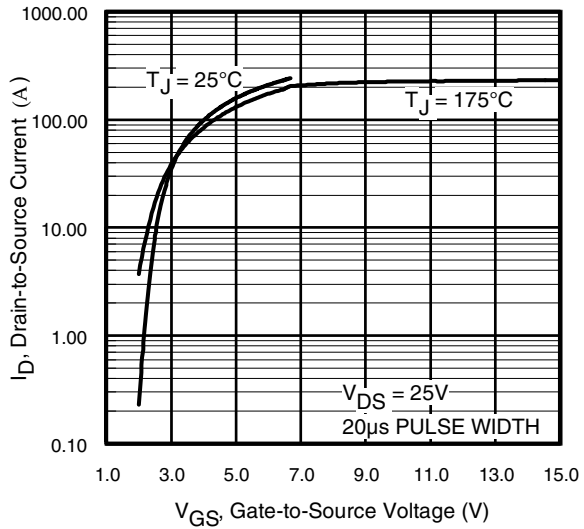**Fig 2.** Typical Output Characteristics



**Fig 3.** Typical Transfer Characteristics
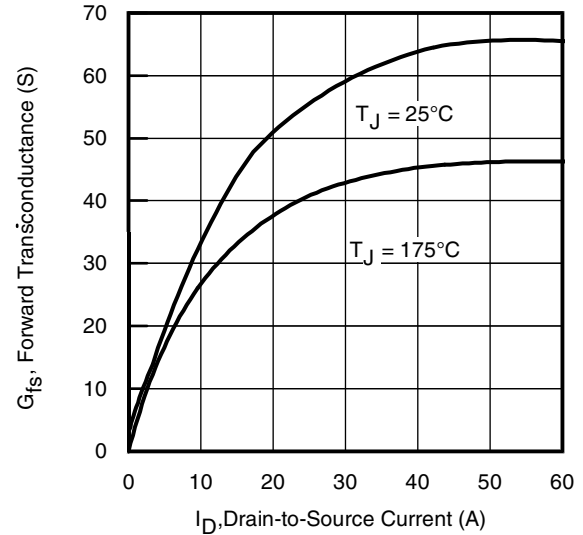


**Fig 4.** Typical Forward Transconductance vs. Drain Current
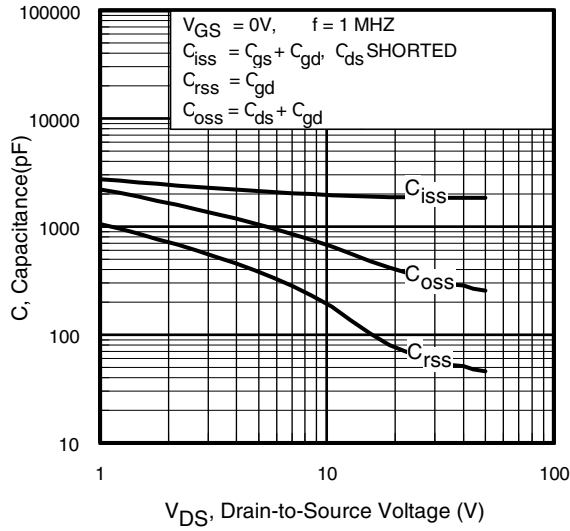
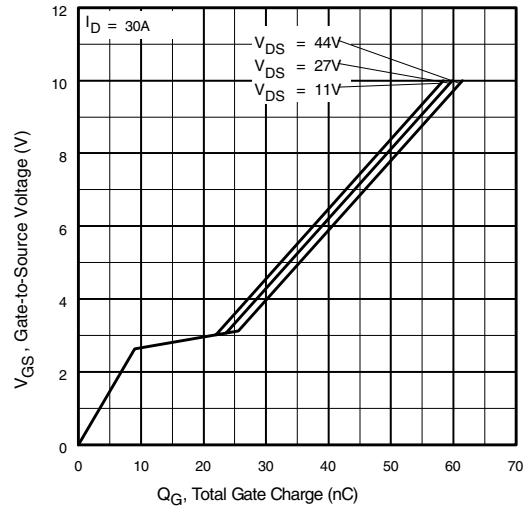**Fig 5.** Typical Capacitance vs.
Drain-to-Source Voltage



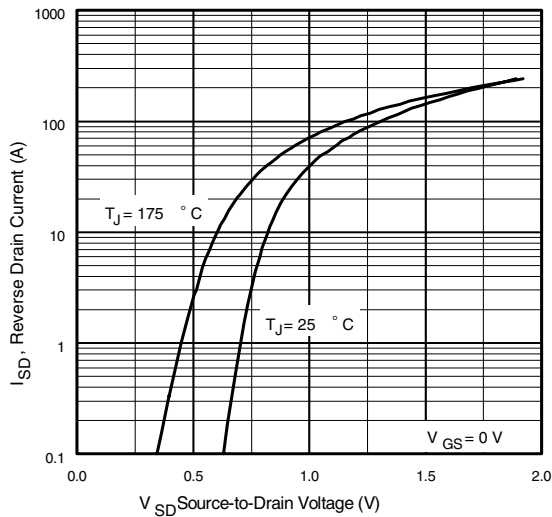**Fig 6.** Typical Gate Charge vs.
Gate-to-Source Voltage

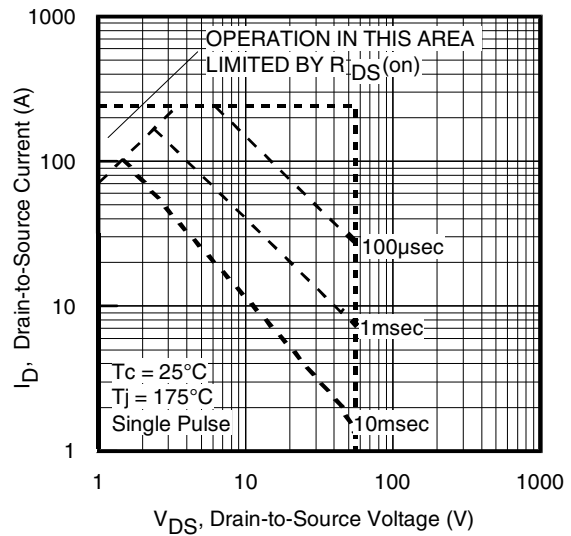

**Fig 7.** Typical Source-Drain Diode
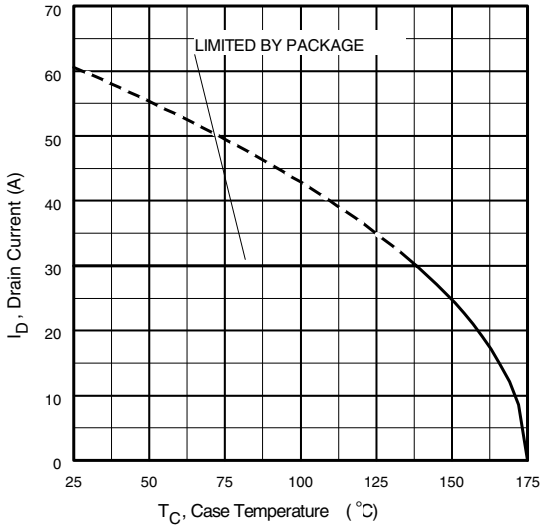Forward Voltage



**Fig 8.** Maximum Safe Operating Area

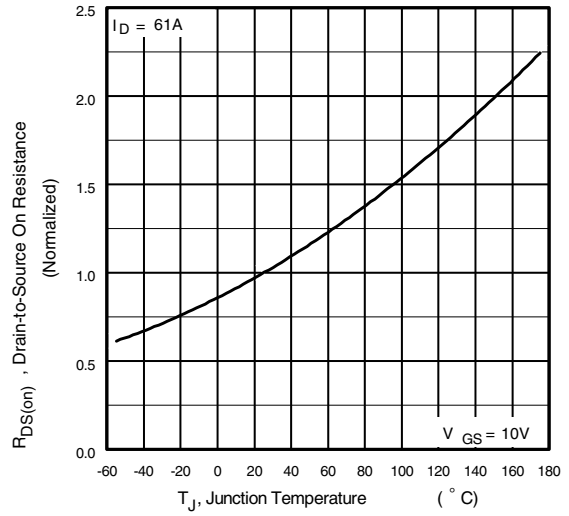**Fig 9.** Maximum Drain Current vs. Case Temperature



**Fig 10.** Normalized On-Resistance vs. Temperature



Notes:
1. Duty factor D = $t_1 / t_2$
2. Peak $T_J$ = $P_{DM}$ x $Z_{thJC}$ + $T_C$
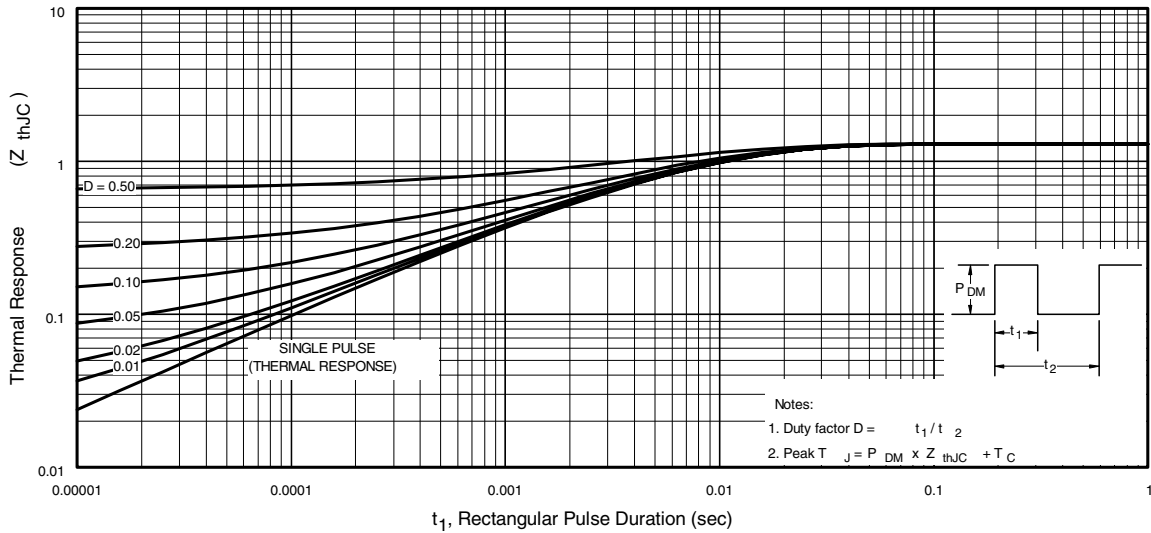
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case
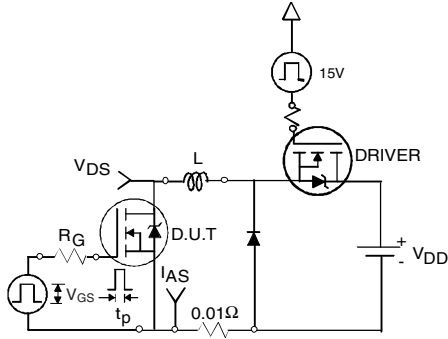
**Fig 12a.** Unclamped Inductive Test Circuit
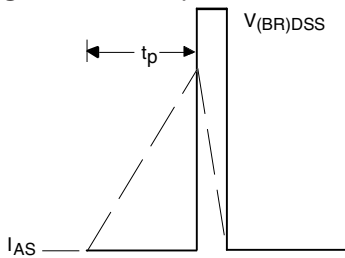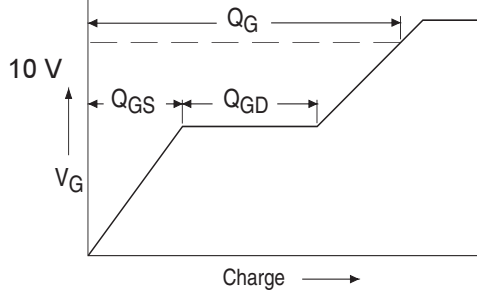


**Fig 12b.** Unclamped Inductive Waveforms



**Fig 13a.** Basic Gate Charge Waveform
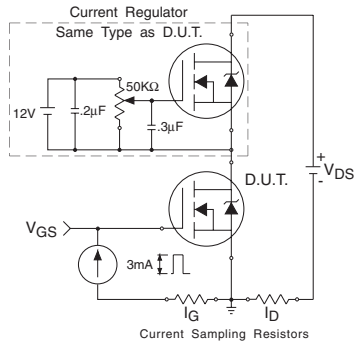


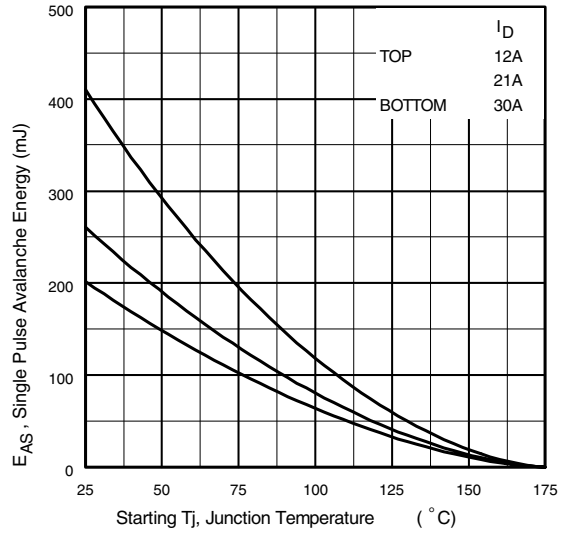**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy vs. Drain Current



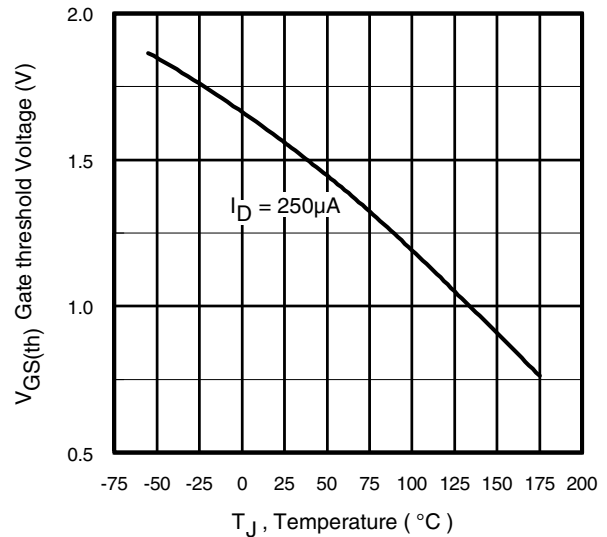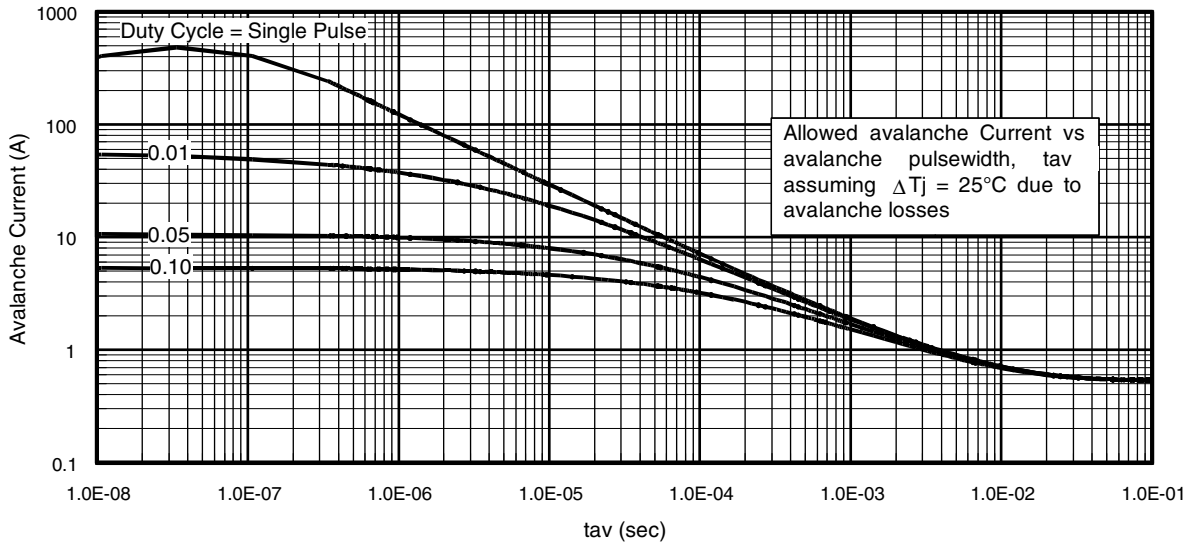**Fig 14.** Threshold Voltage vs. Temperature

**Fig 15.** Typical Avalanche Current vs.Pulsewidth

The graph shows "Duty Cycle = Single Pulse" with curves labeled 0.01, 0.05, 0.10. Text box reads: "Allowed avalanche Current vs avalanche pulsewidth, tav assuming $\Delta$Tj = 25°C due to avalanche losses"



TOP      Single Pulse
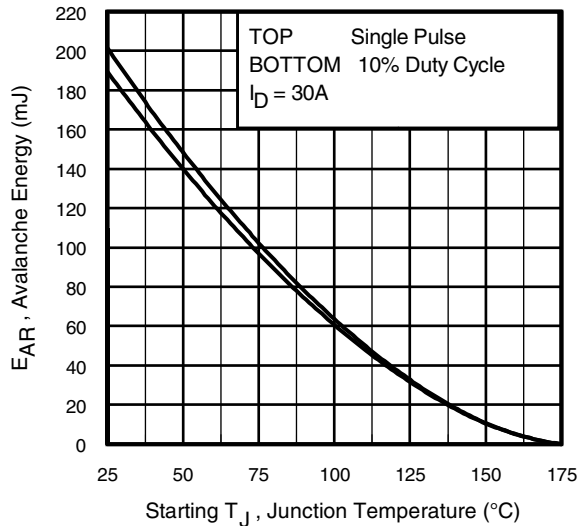BOTTOM   10% Duty Cycle
$I_D$ = 30A

**Fig 16.** Maximum Avalanche Energy vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16:**
**(For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption:
   Purely a thermal phenomenon and failure occurs at a temperature far in excess of $T_{jmax}$. This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as $T_{jmax}$ is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4. $P_{D (ave)}$ = Average power dissipation per single avalanche pulse.
5. BV = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6. $I_{av}$ = Allowable avalanche current.
7. $\Delta T$ = Allowable rise in junction temperature, not to exceed $T_{jmax}$ (assumed as 25°C in Figure 15, 16).
   $t_{av}$ = Average time in avalanche.
   D = Duty cycle in avalanche = $t_{av} \cdot f$
   $Z_{thJC}$(D, $t_{av}$) = Transient thermal resistance, see figure 11)

$$P_{D (ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av}) = \Delta T / Z_{thJC}$$
$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$
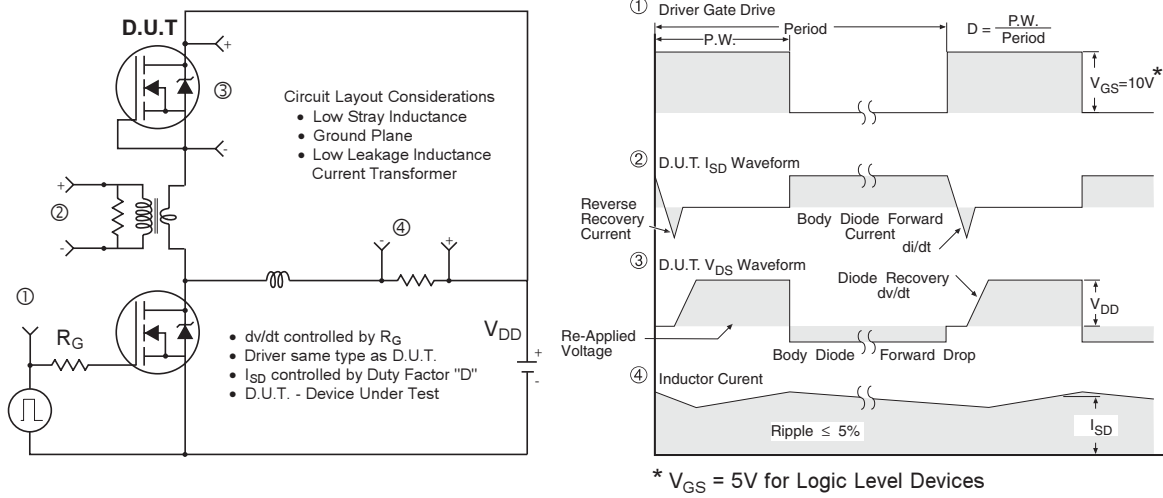$$E_{AS (AR)} = P_{D (ave)} \cdot t_{av}$$

Fig 17. Peak Diode Recovery dv/dt Test Circuit for N-Channel
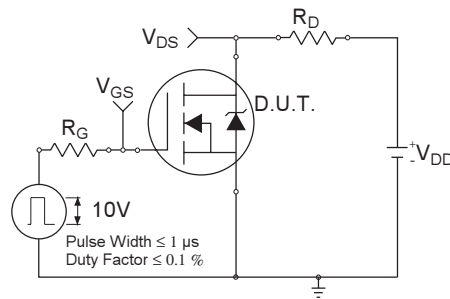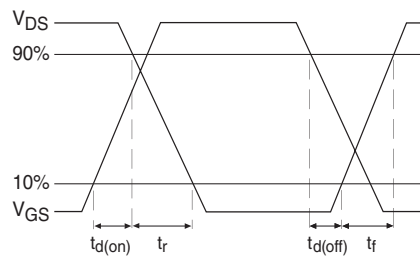HEXFET® Power MOSFETs



Fig 18a. Switching Time Test Circuit



Fig 18b. Switching Time Waveforms

## D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)

6.73 (.265)
6.35 (.250)

- A -

5.46 (.215)
5.21 (.205)

1.27 (.050)
0.88 (.035)

4

6.22 (.245)
5.97 (.235)

1.02 (.040)
1.64 (.025)

1    2    3

- B -

1.52 (.060)
1.15 (.045)

3X  0.89 (.035)
0.64 (.025)

2X  1.14 (.045)
0.76 (.030)

⊕  0.25  (.010)  Ⓜ A Ⓜ B

2.28  (.090)

4.57  (.180)

2.38 (.094)
2.19 (.086)

1.14 (.045)
0.89 (.035)

0.58 (.023)
0.46 (.018)

6.45 (.245)
5.68 (.224)

10.42 (.410)
9.40 (.370)

0.51 (.020)
MIN.

0.58 (.023)
0.46 (.018)

**LEAD ASSIGNMENTS**
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:

1  DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2  CONTROLLING DIMENSION : INCH.
3  CONFORMS TO JEDEC OUTLINE TO-252AA.
4  DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
   SOLDER DIP MAX. +0.16 (.006).

## D-Pak (TO-252AA) Part Marking Information

EXAMPLE:  THIS IS AN IRFR120
          WITH ASSEMBLY
          LOT CODE 1234
          ASSEMBLED ON WW 16, 1999
          IN THE ASSEMBLY LINE "A"

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
916A

12      34

PART NUMBER

DATE CODE
YEAR 9 = 1999
WEEK 16
LINE A
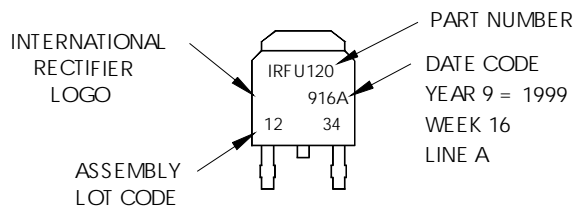
ASSEMBLY
LOT CODE

## I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



6.73 (.265)
6.35 (.250)
- A -

5.46 (.215)
5.21 (.205)

1.27 (.050)
0.88 (.035)

4

1.52 (.060)
1.15 (.045)

6.22 (.245)
5.97 (.235)

1    2    3

- B -

2.28 (.090)
1.91 (.075)

9.65 (.380)
8.89 (.350)

3X  1.14 (.045)
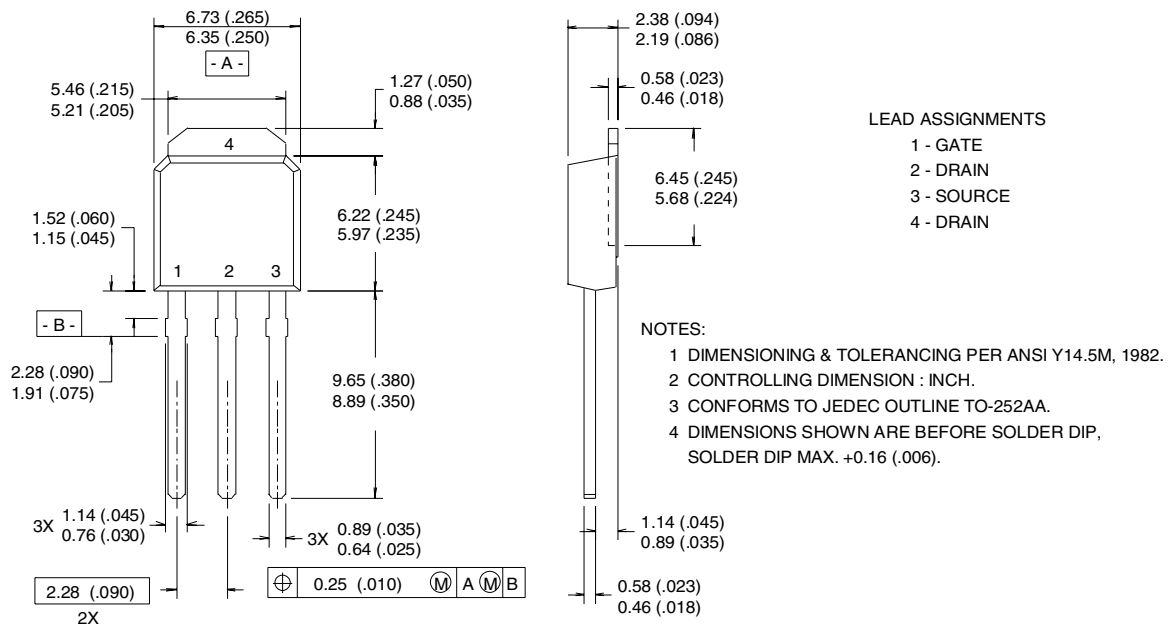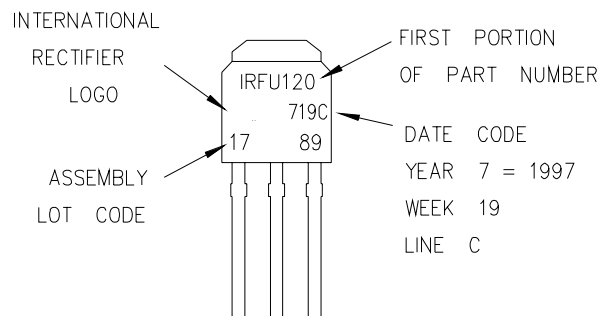0.76 (.030)

3X  0.89 (.035)
0.64 (.025)

2.28 (.090)
2X

⊕  0.25 (.010)  Ⓜ A Ⓜ B

2.38 (.094)
2.19 (.086)

0.58 (.023)
0.46 (.018)

6.45 (.245)
5.68 (.224)

1.14 (.045)
0.89 (.035)

0.58 (.023)
0.46 (.018)

LEAD ASSIGNMENTS
1 - GATE
2 - DRAIN
3 - SOURCE
4 - DRAIN

NOTES:
1  DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
2  CONTROLLING DIMENSION : INCH.
3  CONFORMS TO JEDEC OUTLINE TO-252AA.
4  DIMENSIONS SHOWN ARE BEFORE SOLDER DIP,
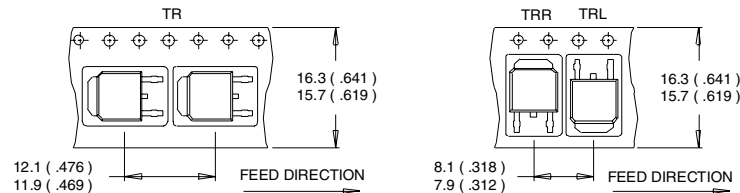   SOLDER DIP MAX. +0.16 (.006).

## I-Pak (TO-251AA) Part Marking Information

EXAMPLE:  THIS  IS  AN  IRFU120
LOT  CODE  1789
ASSEMBLED  ON  WW  19,  1997
IN  THE  ASSEMBLY  LINE  "C"

INTERNATIONAL
RECTIFIER
LOGO

IRFU120
719C
17    89

ASSEMBLY
LOT  CODE

FIRST  PORTION
OF  PART  NUMBER

DATE  CODE
YEAR  7  =  1997
WEEK  19
LINE  C

## D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)

TR

16.3 ( .641 )
15.7 ( .619 )

12.1 ( .476 )
11.9 ( .469 )

FEED DIRECTION

TRR    TRL

16.3 ( .641 )
15.7 ( .619 )

8.1 ( .318 )
7.9 ( .312 )

FEED DIRECTION

NOTES :
1.  CONTROLLING DIMENSION : MILLIMETER.
2.  ALL DIMENSIONS ARE SHOWN IN MILLIMETERS ( INCHES ).
3.  OUTLINE CONFORMS TO EIA-481 & EIA-541.

$\varnothing$ 13 INCH

16 mm
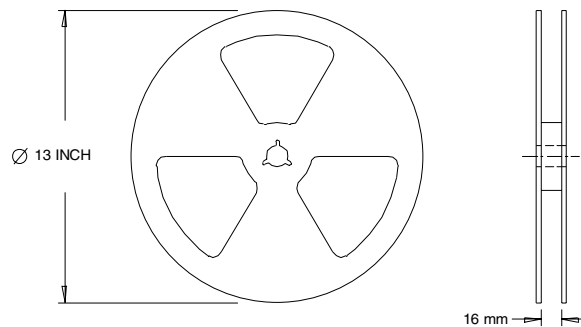
NOTES :
1. OUTLINE CONFORMS TO EIA-481.

**Notes:**

① Repetitive rating;  pulse width limited by
max. junction temperature. (See fig. 11).

② Limited by $T_{Jmax}$, starting $T_J$ = 25°C,
L = 0.45mH, $R_G$ = 25Ω, $I_{AS}$ = 30A, $V_{GS}$ =10V.
Part not recommended for use above this
value.

③ $I_{SD}$ ≤ 30A, di/dt ≤ 280A/μs, $V_{DD}$ ≤ $V_{(BR)DSS}$,
$T_J$ ≤ 175°C.

④ Pulse width ≤ 1.0ms; duty cycle ≤ 2%.

⑤ $C_{oss}$ eff. is a fixed capacitance that gives the same charging time
as $C_{oss}$ while $V_{DS}$ is rising from 0 to 80% $V_{DSS}$ .

⑥ Limited by $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive
avalanche performance.

⑦ This value determined from sample failure population. 100%
tested to this value in production.

⑧ When mounted on 1" square PCB ( FR-4 or G-10 Material ).
For recommended footprint and soldering techniques refer to
application note #AN-994.