



62783

LINEAR INTEGRATED CIRCUIT

8CH HIGH-VOLTAGE SOURCE DRIVER

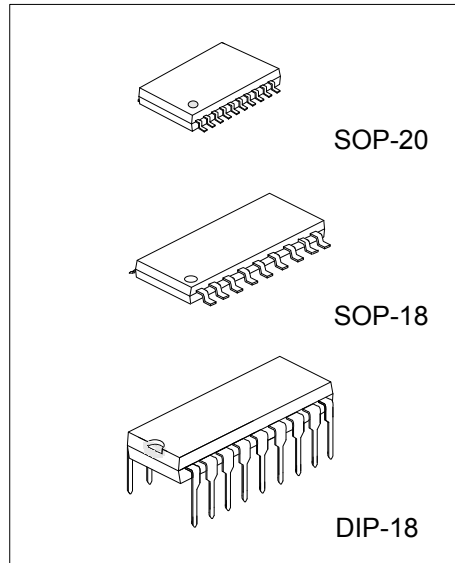
DESCRIPTION

The UTC 62783 consists of eight source current transistor array combination and it is suitable for fluorescent display applications.

The UTC 62783 is ideal for uses, such as relay, hammer and lamp drivers.

FEATURES

- *High output voltage: $V_{CC} = 50V$ (MIN.)
- * Output current (single output) $I_{OUT} = -500mA$ (MIN.)
- * Output clamp diodes and single supply voltage
- * Input compatible with various types of logic
- * TTL, 5V CMOS

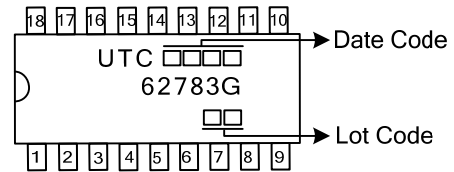
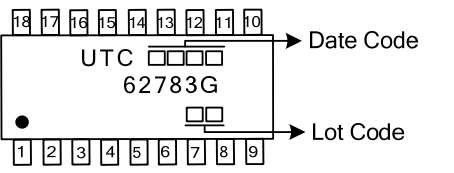
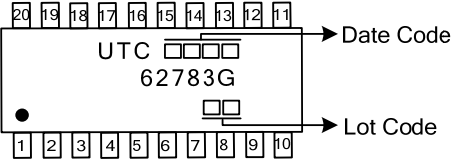


ORDERING INFORMATION

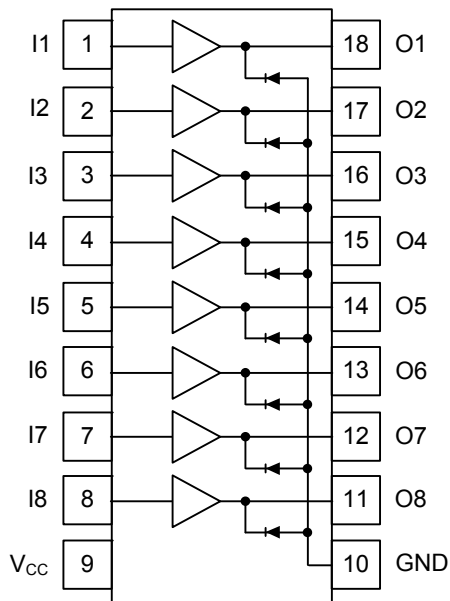
Ordering Number	Package	Packing
62783G-D18-T	DIP-18	Tube
62783G-S18-T	SOP-18	Tube
62783G-S18-R	SOP-18	Tape Reel
62783G-S20-T	SOP-20	Tube
62783G-S20-R	SOP-20	Tape Reel

<p>62783G-D18-T</p> <p>(1) Packing Type</p> <p>(2) Package Type</p> <p>(3) Green Package</p>	<p>(1) T: Tube, R: Tape Reel</p> <p>(2) D18: DIP-18, S18: SOP-18, S20: SOP-20</p> <p>(3) G: Halogen Free and Lead Free</p>
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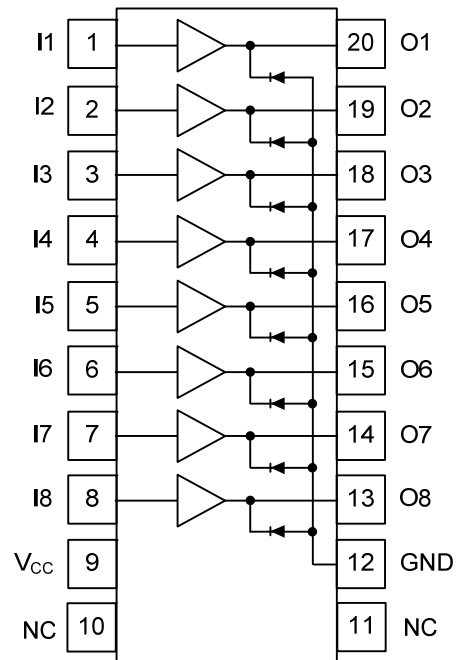
MARKING

Packing	MARKING
DIP-18	 <p>Diagram showing the marking on a DIP-18 package. The top edge has pins 18, 17, 16, 15, 14, 13, 12, 11, 10. The bottom edge has pins 1, 2, 3, 4, 5, 6, 7, 8, 9. The marking includes 'UTC' followed by three empty boxes, '62783G', and two empty boxes. Arrows point to the top three boxes as 'Date Code' and the bottom two boxes as 'Lot Code'.</p>
SOP-18	 <p>Diagram showing the marking on an SOP-18 package. The top edge has pins 18, 17, 16, 15, 14, 13, 12, 11, 10. The bottom edge has pins 1, 2, 3, 4, 5, 6, 7, 8, 9. The marking includes 'UTC' followed by three empty boxes, '62783G', and two empty boxes. A dot is located at the bottom left corner. Arrows point to the top three boxes as 'Date Code' and the bottom two boxes as 'Lot Code'.</p>
SOP-20	 <p>Diagram showing the marking on an SOP-20 package. The top edge has pins 20, 19, 18, 17, 16, 15, 14, 13, 12, 11. The bottom edge has pins 1, 2, 3, 4, 5, 6, 7, 8, 9, 10. The marking includes 'UTC' followed by three empty boxes, '62783G', and two empty boxes. A dot is located at the bottom left corner. Arrows point to the top three boxes as 'Date Code' and the bottom two boxes as 'Lot Code'.</p>

■ PIN CONFIGURATION



DIP-18/SOP-18

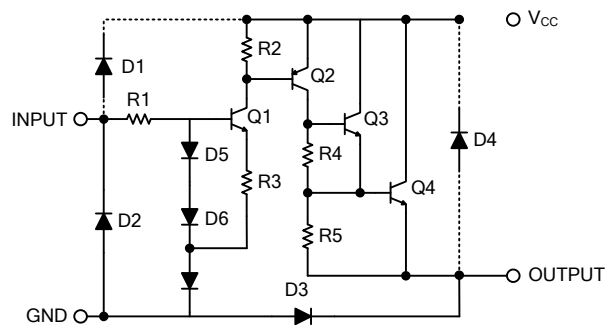


SOP-20

■ PIN DESCRIPTION

PIN NO.		PIN NAME	DESCRIPTION
DIP-18/ SOP-18	SOP-20		
1	1	I1	Input Of CH1
2	2	I2	Input Of CH2
3	3	I3	Input Of CH3
4	4	I4	Input Of CH4
5	5	I5	Input Of CH5
6	6	I6	Input Of CH6
7	7	I7	Input Of CH7
8	8	I8	Input Of CH8
9	9	V _{CC}	Power Supply
10	12	GND	Ground
11	13	O8	Output Of CH8
12	14	O7	Output Of CH7
13	15	O6	Output Of CH6
14	16	O5	Output Of CH5
15	17	O4	Output Of CH4
16	18	O3	Output Of CH3
17	19	O2	Output Of CH2
18	20	O1	Output Of CH1
-	10, 11	NC	Not connected

■ SCHEMATICS (EACH DRIVER)



R1	R2	R3	R4	R5
10k Ω	20k Ω	2.6k Ω	10k Ω	5k Ω

Note: The input and output parasitic diodes (D1 & D4) cannot be used as clamp diodes

■ **ABSOLUTE MAXIMUM RATING** ($T_A = 25^\circ\text{C}$, unless otherwise specified)

PARAMETER	SYMBOL	RATINGS	UNIT
Supply Voltage	V_{CC}	50	V
Input Voltage	V_{IN}	15	V
Clamp Diode Reverse Voltage	V_R	50	V
Output Current	I_{OUT}	-500	mA/ch
Clamp Diode Forward Current	I_F	500	mA
Power Dissipation	DIP-18	1470	mW
	SOP-18/SOP-20	960	
Derated Above 25°C		7.7	mW/ $^\circ\text{C}$
Operating Temperature	T_{OPR}	-40~+85	$^\circ\text{C}$
Storage Temperature	T_{STG}	-55~+150	$^\circ\text{C}$

Note: Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

■ **RECOMMENDED OPERATING CONDITIONS** ($T_A = -40 \sim +80^\circ\text{C}$)

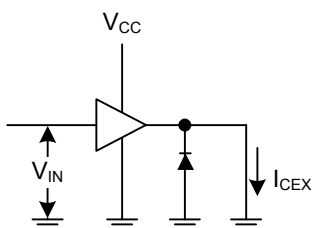
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Supply Voltage	V_{CC}				50	V
Output Current	I_{OUT}	$T_A=85^\circ\text{C}$, $T_J=120^\circ\text{C}$, $T_P=25\text{ms}$	Duty=10%		-180	mA/ch
			Duty=50%		-38	mA/ch
Input Voltage	V_{IN}				12	V
Input Voltage	Output On	$V_{IN(ON)}$	2.0	5.0	15	V
	Output Off	$V_{IN(OFF)}$	0		0.8	V
Clamp Diode Reverse Voltage	V_R				35	V
Clamp Diode Forward Current	I_F				400	mA
Power Dissipation	DIP-18	P_D			520	mW
	SOP-18				350	
	SOP-20				350	

■ **ELECTRICAL CHARACTERISTICS** ($T_A = 25^\circ\text{C}$)

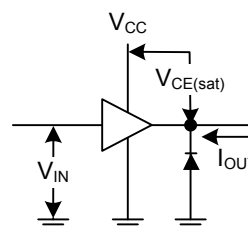
PARAMETER	SYMBOL	TEST CIRCUIT	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Output Leakage Current	I_{CEX}	1	$V_{CC} = V_{CC(MAX)}$, $V_{IN} = 0.4\text{V}$			100	μA
Output Saturation Voltage	$V_{CE(SAT)}$	2	$V_{IN} = V_{IN(ON)}$, $I_{OUT} = -350\text{mA}$			2.0	V
			$V_{IN} = V_{IN(ON)}$, $I_{OUT} = -225\text{mA}$			1.9	V
			$V_{IN} = V_{IN(ON)}$, $I_{OUT} = -100\text{mA}$			1.8	V
Input Current	$I_{IN(ON)}$	3	$V_{IN} = 2.4\text{V}$		36	52	μA
			$V_{IN} = 3.85\text{V}$		180	260	μA
Supply Current	$I_{CC(ON)}$	3	$V_{IN} = V_{IN(ON)}$, $V_{CC} = 50\text{V}$			2.5	mA/ch
Input Voltage	$V_{IN(ON)}$	4	$V_{CE} = 2.0\text{V}$			2.0	V
	$V_{IN(OFF)}$		$I_{OUT} = -500\mu\text{A}$	0.8			V
Clamp Diode Reverse Current	I_R	5	$V_R = 50\text{V}$			50	μA
Clamp Diode Forward Voltage	V_F	6	$I_F = 350\text{mA}$			2.0	V
Turn-On Delay	t_{ON}	7	$V_{CC} = V_{CC(MAX)}$, $R_L = 125\Omega$ $C_L = 15\text{pF}$, $R_L = 88\Omega$		0.15		μs
Turn-Off Delay	t_{OFF}				4.5		μs

■ TEST CIRCUITS

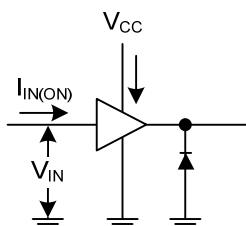
1. I_{CEX}



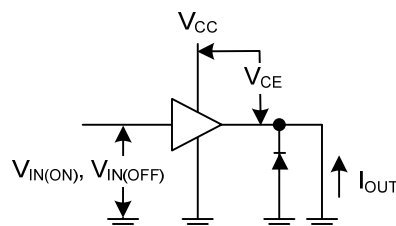
2. $V_{CE(SAT)}$



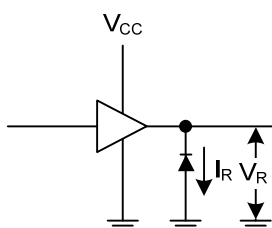
3. $I_{IN(ON)}$, I_{CC}



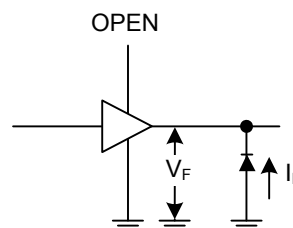
4. $V_{IN(ON)}$, $V_{IN(OFF)}$



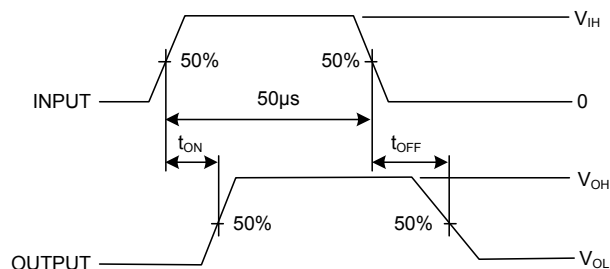
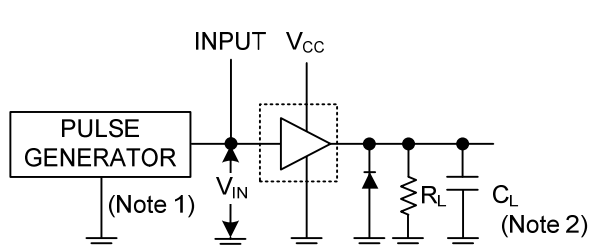
5. I_R



6. V_F



7. t_{ON} , t_{OFF}



Notes: 1. Pulse width 50 μ s, duty cycle 10% Output impedance 50 Ω , $t_r \leq 5$ ns, $t_f \leq 10$ ns

2. C_L includes probe and jig capacitance

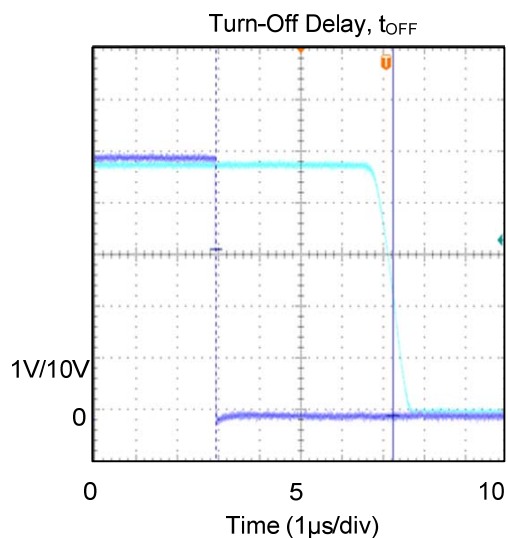
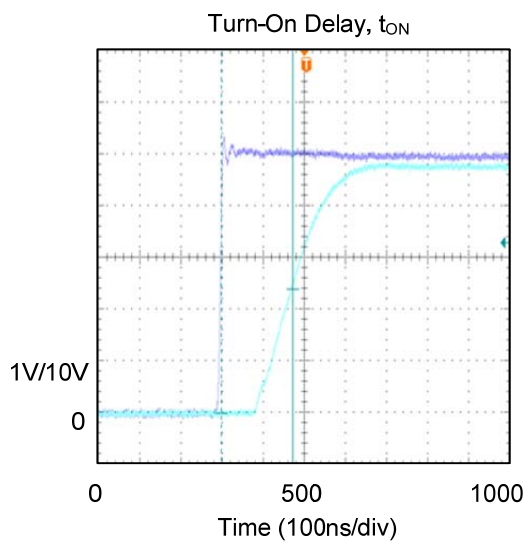
■ PRECAUTIONS FOR USING

This circuit does not integrate protection circuits such as over-current and overvoltage protectors.

Thus, the IC may be damaged if excess current or voltage is occurred to the IC. Make sure the IC design is fine so that excess current or voltage will not be applied to the IC.

You must take extreme care to the design of the output line, V_{CC} and GND line because IC may be destroyed under the condition of short-circuit between outputs, air contamination fault, or fault by improper grounding.

■ TYPICAL CHARACTERISTICS



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