MAS6181B

AM Receiver IC

- **Dual Band Receiver IC**
- **High Sensitivity**
- **Very Low Power Consumption**
- **Wide Supply Voltage Range**
- **Power Down Control**
- **Control for AGC On**
- **High Selectivity by Crystal Filter**
- **Fast Startup Feature**

DESCRIPTION

The MAS6181 AM-Receiver chip is a highly sensitive, simple to use AM receiver specially intended to receive time signals in the frequency range from 40 kHz to 100 kHz. Only a few external components are required for time signal receiving. The circuit has preamplifier, wide range automatic gain control, demodulator and output comparator built in. The output signal can be processed directly by an additional digital circuitry to extract the data from the received signal. The control for AGC (automatic gain control) can be used to switch AGC on or off if necessary.

The MAS6181 supports receiving two different frequency signals by two selective crystal filters and an integrated switch to switch between two antenna frequencies. It has differential input for improved common mode disturbance rejection.

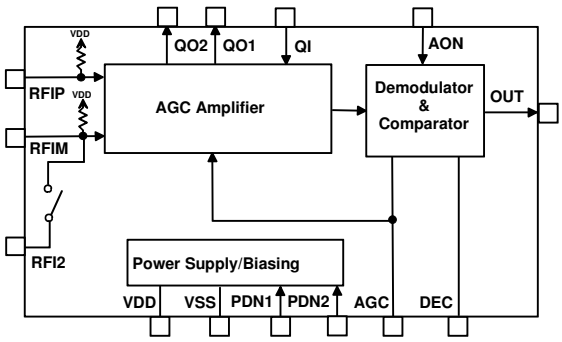
FEATURES

- Dual Band Receiver IC
- Highly Sensitive AM Receiver
- Wide Supply Voltage Range from 1.1 V to 3.6 V
- Very Low Power Consumption
- Power Down Control
- Fast Startup
- Only a Few External Components Necessary
- Control for AGC On
- Wide Frequency Range from 40 kHz to 100 kHz
- High Selectivity by Quartz Crystal Filter
- Differential Input

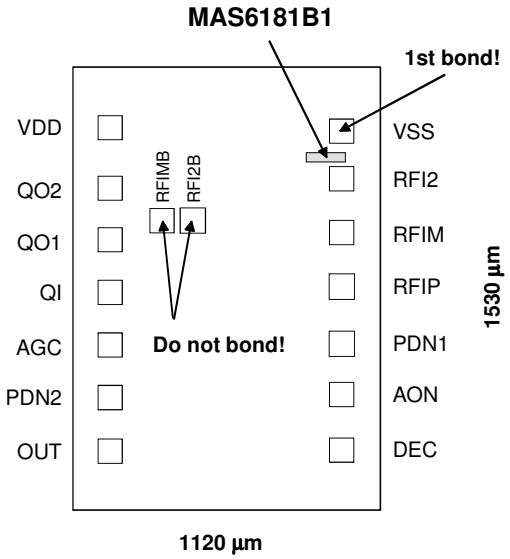
APPLICATIONS

- Multi Band Time Signal Receiver WWVB (USA), JJY (Japan), DCF77 (Germany), MSF (UK), HBG (Switzerland) and BPC (China)

BLOCK DIAGRAM



PAD LAYOUT



DIE size = 1120 x 1530 µm; rectangular PAD 80 µm x 80 µm

Note: Because the substrate of the die is internally connected to VSS, the die has to be connected to VSS or left floating. Please make sure that VSS is the first pad to be bonded. Pick-and-place and all component assembly are recommended to be performed in ESD protected area.

Note: Coordinates are pad center points where origin has been located in bottom-left corner of the silicon die.

Pad Identification	Name	X-coordinate	Y-coordinate	Note
Power Supply Voltage	VDD	126 µm	1332 µm	
Quartz Filter Output for Crystal 2	QO2	126 µm	1132 µm	
Quartz Filter Output for Crystal 1	QO1	126 µm	962 µm	
Quartz Filter Input for Crystals	QI	126 µm	788 µm	
AGC Capacitor	AGC	126 µm	614 µm	
Power Down/Frequency Selection Input 2	PDN2	126 µm	440 µm	1
Receiver Output	OUT	126 µm	263 µm	2
Demodulator Capacitor	DEC	994 µm	266 µm	
AGC On Control	AON	994 µm	450 µm	3
Power Down/Frequency Selection Input 1	PDN1	994 µm	618 µm	1
Positive Receiver Input	RFIP	994 µm	807 µm	4
Negative Receiver Input	RFIM	994 µm	985 µm	4
Test pad RFIMB	RFIMB	298 µm	1025 µm	5
Test pad RFI2B	RFI2B	400 µm	1025 µm	5
Receiver Input 2 (for Antenna Capacitor 2)	RFI2	994 µm	1163 µm	
Power Supply Ground	VSS	994 µm	1321 µm	

Notes:
1) PDN1 = VDD and PDN2 = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down controlled to power on
2) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - The output is a current source/sink with $|I_{OUT}| > 5$ µA
   - At power down the output is pulled to VSS (pull down switch)
3) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (normal operation)
   - Unused AON pad can be left unconnected due to internal pull-up with current < 1 µA. Pull up current is switched off at power down.
4) Receiver inputs RFIP and RFIM have both 1.4 MΩ biasing resistors towards VDD
5) RFIMB and RFI2B pads are left unconnected. They are only for wafer level testing purposes

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Conditions	Min	Max	Unit
Supply Voltage	V_{DD}-V_{SS}		-0.3	3.6	V
Input Voltage	V_{IN}		V_{SS}-0.3	V_{DD}+0.3	V
Operating Temperature	T_{OP}		-40	+85	°C
Storage Temperature	T_{ST}		-55	+150	°C

Stresses beyond those listed may cause permanent damage to the device. The device may not operate under these conditions, but it will not be destroyed.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 1.5V, Temperature = 27℃ unless otherwise noted

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Operating Voltage	V_{DD}		1.10	1.5	3.6	V
Current Consumption	I_{DD}	VDD=1.5 V, Vin=0 µVrms VDD=1.5 V, Vin=20 mVrms VDD=3.6 V, Vin=0 µVrms VDD=3.6 V, Vin=20 mVrms	 31 24	66 40 68 42	 85 65	µA
Stand-By Current	I_{DDoff}				0.1	µA
Input Frequency Range	f_{IN}		40		100	kHz
Minimum Input Voltage	$V_{IN\ min}$			0.4	1	µVrms
Maximum Input Voltage	$V_{IN\ max}$		20			mVrms
Receiver Input Resistance Receiver Input Capacitance	R_{RFI} C_{RFI}	f=40kHz...77.5 kHz		600 1.1		kΩ pF
RFI2 Switch On Resistance RFI2 Switch Off Capacitance	R_{ON2} C_{OFF2}	VDD=1.4 V		5 20	15	Ω pF
Input Levels $\|I_{IN}\|$<0.5 µA	V_{IL} V_{IH}		 V_{DD}-0.35		0.35	V
Output Current V_{OL}<0.2 V_{DD};V_{OH}>0.8 V_{DD}	$\|I_{OUT}\|$		5			µA
DCF77 Output Pulses	T_{100ms} T_{200ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms, see note below!		95 195		ms
MSF Output Pulses	T_{100ms} T_{200ms} T_{300ms} T_{500ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms, see note below!		120 220 320 520		ms
WWVB Output Pulses	T_{200ms} T_{500ms} T_{800ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms, see note below!		200 500 800		ms
JJY60 Output Pulses	T_{200ms} T_{500ms} T_{800ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms, see note below!		210 505 800		ms
JJY40 Output Pulses	T_{200ms} T_{500ms} T_{800ms}	1 µVrms ≤ V_{IN} ≤ 20 mVrms, see note below!		200 495 790		ms
Startup Time	T_{Start}	Fast Start-up, Vin=0.4 µVrms Fast Start-up, Vin=20 mVrms		1.3 3.5		s
Output Delay Time	T_{Delay}			50	100	ms

Note: Stand-by current consumption may increase if V_{IH} and V_{IL} differ from VDD and GND respectively.
Note: See Note 6: Time Signal Software's Pulse Width Recognition Limits and Table 5 on page 9!

FREQUENCY SELECTION

The power down control and frequency selection using internal antenna's tuning capacitor switch (RFI2) are achieved by two digital control pins PDN1 and PDN2. The control logic is presented in table 1.

Table 1. Frequency selection and power down control

PDN1	PDN2	RFI2 Switch	Description
High	High	Open	Power down
High	Low	Open	Antenna frequency 1
Low	High	Closed	Antenna frequency 2, RFI2 capacitor connected in parallel with antenna
Low	Low	Closed	Antenna frequency 2, RFI2 capacitor connected in parallel with antenna

If frequency 1 is selected the RFI2 switch is open (non conductive). Antenna frequency is determined by antenna inductor L_{ANT} (see Typical Application on page 5), antenna capacitor C_{ANT1} and parasitic capacitances related to antenna coil, inputs RFIP, RFIM and RFI2 (see Antenna Tuning Considerations below). Frequency 1 is the highest frequency of the two selected frequencies.

If frequency 2 is selected then RFI2 switch is closed to connect C_{ANT2} to pin RFIM in parallel with ferrite antenna and tune it to frequency 2. Frequency 2 is the lowest frequency of the two selected frequencies.

It is recommended to switch the device to power down for at least 50ms before switching to another frequency. This guarantees fast startup in switching to another frequency. During minimum 50ms power down time the AGC capacitor voltage is completely pulled to VDD to initialize proper startup conditions for the AGC. Without the described proper fast startup control the startup time can be several minutes. With fast startup it is shortened typically to a few seconds.

ANTENNA TUNING CONSIDERATIONS

The ferrite bar antenna having inductance L_{ANT} and parasitic coil capacitance C_{COIL} is tuned to two reception frequencies f_1 and f_2 by parallel capacitors C_{ANT1} and C_{ANT2}. The receiver input stage and internal antenna capacitor switches have capacitances C_{RFI} and C_{OFF2} which affect the resonance frequencies. C_{OFF2} is switch capacitance when switch is open. When the antenna switch is closed the off capacitance is shorted by on resistance of the switch and it is effectively eliminated. Following relationships can be written for the two tuning frequencies.

Frequency f_1 (highest frequency):

$C_{TOT1} \sim C_{COIL}+C_{ANT1}+C_{RFI}+C_{OFF2}$, assuming $C_{ANT2} >> C_{OFF2}$

$$f_1 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT1}}}$$

Frequency f_2 (lowest frequency):

$C_{TOT2}=C_{COIL}+C_{ANT1}+C_{ANT2}+C_{RFI}$

$$f_2 = \frac{1}{2\pi\sqrt{L_{ANT} \cdot C_{TOT2}}}$$

TYPICAL APPLICATION

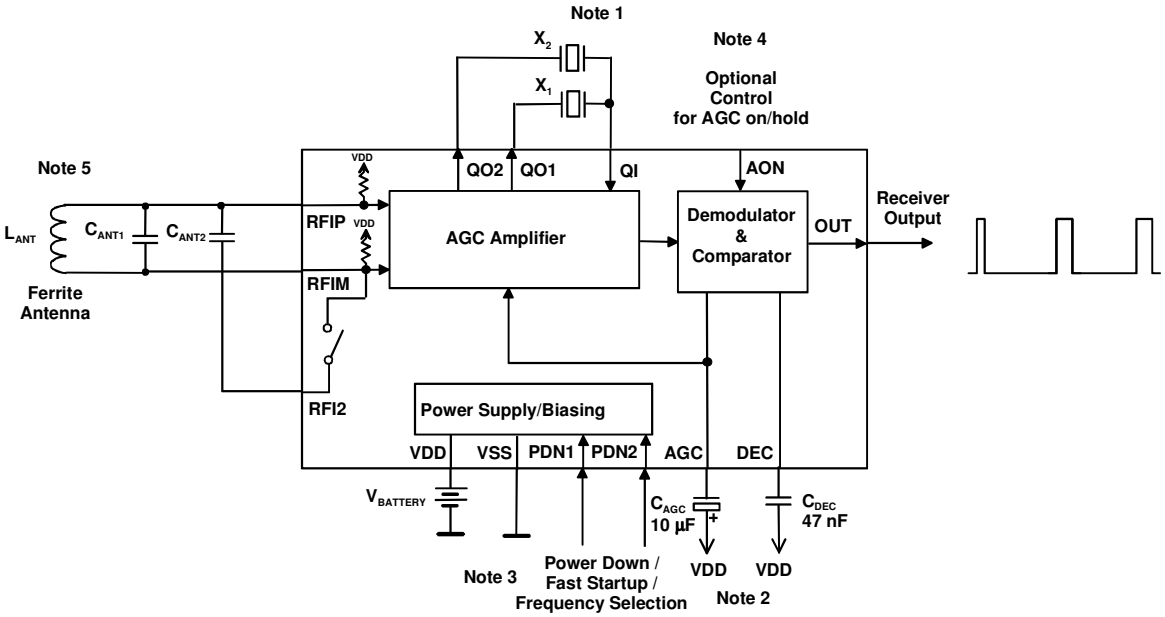


Figure 1. Application circuit of dual band receiver MAS6181

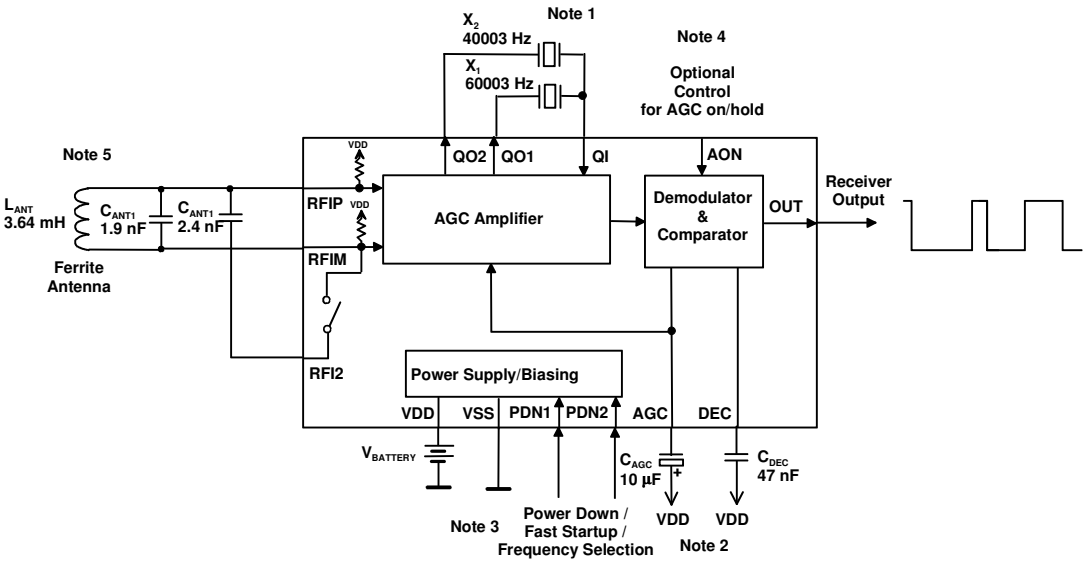


Figure 2. Example circuit of dual band receiver MAS6181 for JJY 60 kHz and 40 kHz frequencies

TYPICAL APPLICATION (Continued)

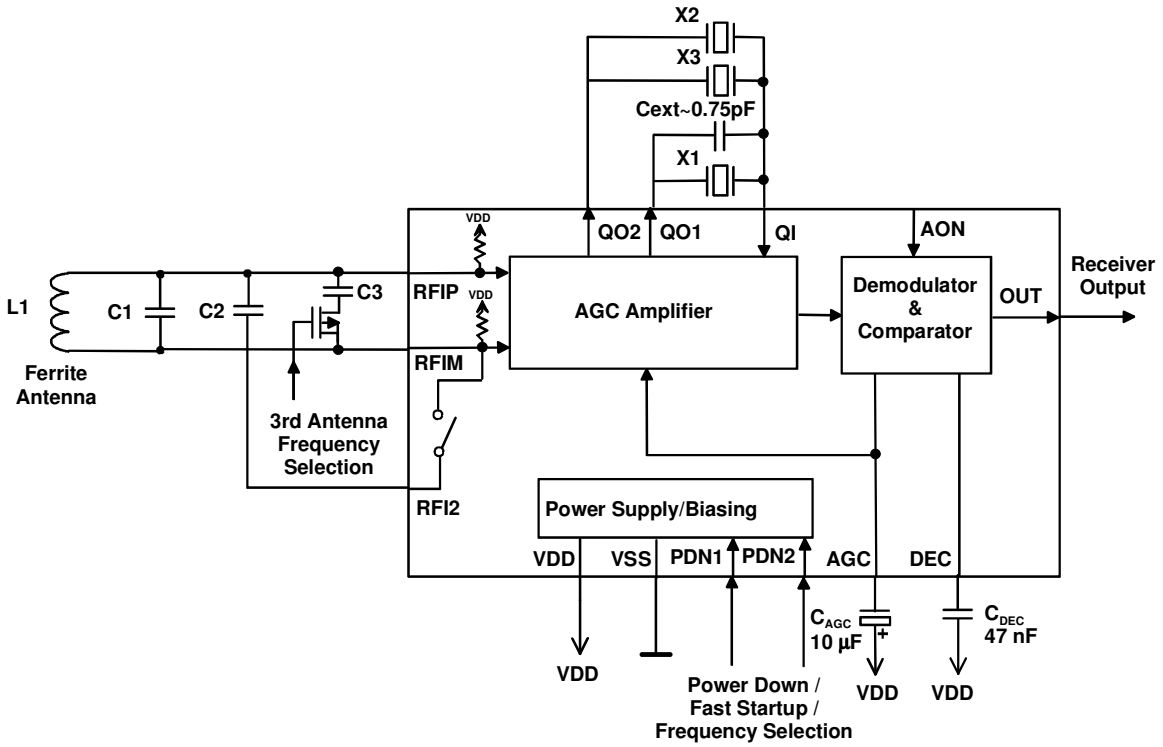


Figure 3. Application circuit of MAS6181 in tri band receiver configuration

TYPICAL APPLICATION (Continued)

Note 1: Crystals
The crystals as well as ferrite antenna frequencies are chosen according to the time signal system (Table 2). The reason why the crystal frequency is about 3 Hz higher than the signal frequency is that the crystal is operated without the loading capacitor. Without loading capacitor the actual resonance frequency is about 3 Hz lower than with load thus 77.503 kHz crystal resonates at 77.500 kHz when no loading capacitor is used.

Table 2. Time Signal System Frequencies

Time Signal System	Location	Antenna Frequency	Recommended Crystal Frequency
DCF77	Germany	77.5 kHz	77.503 Hz
HBG	Switzerland	75 kHz	75.003 kHz
MSF	United Kingdom	60 kHz	60.003 kHz
WWVB	USA	60 kHz	60.003 kHz
JJY	Japan	40 kHz and 60 kHz	40.003 kHz and 60.003 kHz
BPC	China	68.5 kHz	68.505 kHz

The parasitic shunt capacitance C_0 of the two crystals should be as similar to each other as possible since they are used to cancel each other. Large shunt capacitance mismatch between the two crystals can lead to non-ideal filter characteristics and wide noise band-width. Effectively this means lower sensitivity performance.

It should be noted that grounded crystal package has reduced shunt capacitance. This value is about 85% of floating crystal shunt capacitance. For example crystal with 1pF floating package shunt capacitance can have 0.85pF grounded package shunt capacitance. PCB traces of crystal and external compensation capacitance should be kept at minimum to minimize additional parasitic capacitance which can cause capacitance mismatching.

When using MAS6181B1 it does not matter which of the two frequency crystals is connected to QO1 pin and which to QO2 pin.

Table 3 below presents some crystal suppliers having suitable crystals for time signal receiver application.

Table 3. Crystal Suppliers and Crystal Types in Alphabetical Order for Time Signal Receiver Application

Supplier	Crystal Type	Dimensions	Web Link
Citizen	CFV-206	ø 2.0 x 6.0	http://www.citizen.co.jp/tokuhan/quartz/
Epson Toyocom	C-2-Type C-4-Type	ø 1.5 x 5.0 ø 2.0 x 6.0	http://www.epsontoyocom.co.jp/english/
KDS Daishinku	DT-261	ø 2.0 x 6.0	http://www.kds.info/index_en.htm
Microcrystal	MS3V-T1R	1.45 x 1.45 x 6.7	http://www.microcrystal.com/
Seiko Instruments	VTC-120	ø 1.2 x 4.7	http://www.sii-crystal.com

Note 2: AGC Capacitor
The 10µF AGC and 47nF DEC capacitors must have low leakage currents due to very small signal currents through the capacitors. The insulation resistance of these capacitors should be at minimum several 100 MΩ. Also probes with at least several 100 MΩ impedance should be used for voltage probing of the AGC and DEC pins to not disturb their operation. Tantalum capacitors have lower leakage than the electrolyte capacitors. In case of using electrolyte type AGC capacitor the capacitor voltage rating should be at least 25 V for sufficiently low leakage. The DEC capacitor can be low leakage chip capacitor since its capacitance value is small.

It is recommended to connect both AGC and DEC capacitors to VDD (see application figures 1 and 2) although VSS connection is also possible. The VDD connection provides better supply noise immunity because the signals and AGC gain are referenced to VDD. Additionally leakage currents are minimized in this connection because in power down the AGC pin voltage is pulled to VDD (to minimum AGC gain) providing zero voltage over the AGC capacitor.

TYPICAL APPLICATION (Continued)

Note 3: Power Down / Fast Startup Control
Both power down and fast startup is controlled using the PDN pin. The device is in power down (turned off) if PDN1 = PDN2 = VDD and in power up with other three PDN1 and PDN2 control bit combinations (see table 1 on page 4). Fast startup is triggered automatically when moving from power down to power up. The VDD must have been high before moving from power down to power up to guarantee proper operation of fast startup circuitry. Additionally the device should have been kept in power down state at least 50ms before power up. This guarantees that the AGC capacitor voltage has been completely pulled to VDD during power down. The startup time without proper fast startup control can be several minutes. With fast startup it is shortened typically to a few seconds.

Note 4: Optional Control for AGC On/Hold
AON control pin has internal pull up which turns AGC circuit on all the time if AON pin is left unconnected. Optionally AON control can be used to hold and release AGC circuit. Stepper motor drive of analog clock or watch can produce disturbing amount of noise which can shift the input amplifier gain to non optimal level. This can be avoided by controlling AGC hold (AON=VSS) during stepper motor drive periods and releasing AGC (AON=VDD) when motors are not driven. The AGC should be in hold only during disturbances and kept on other time released since due to leakage the AGC can still change slowly when in hold.

Note 5: Ferrite Antenna
The ferrite antenna converts the transmitted radio wave into a voltage signal. It has an important role in determining receiver performance. Recommended antenna impedance at resonance is around 100 kΩ.
Low antenna impedance corresponds to low noise but often also to small signal amplitude. On the other hand high antenna impedance corresponds to high noise but also large signal. The optimum performance where signal-to-noise ratio is at maximum is achieved in between.
The antenna should have also some selectivity for rejecting near signal band disturbances. This is determined by the antenna quality factor which should be approximately 100. Much higher quality factor antennas suffer from extensive tuning accuracy requirements and possible tuning drifts by the temperature.

Antenna impedance R_{ant} can be calculated using equation 1 where f_{res}, L, Q_{ant} and C are resonance frequency f_{res}, coil inductance, antenna quality factor and antenna tuning capacitor respectively. Antenna quality factor Q_{ant} is defined by ratio of resonance frequency f_{res} and antenna bandwidth B (equation 2).

$$R_{ant} = 2\pi \cdot f_{res} \cdot L \cdot Q_{ant} = \frac{Q_{ant}}{2\pi \cdot f_{res} \cdot C} = \frac{1}{2\pi \cdot B \cdot C} \qquad \textbf{Equation 1.}$$

$$Q_{ant} = \frac{f_{res}}{B} \qquad \textbf{Equation 2.}$$

Table 4 below presents some antenna suppliers for time signal application.

Table 4. Antenna Suppliers and Antenna Types in for Time Signal Application

Supplier	Antenna Type	Dimensions	Web Link
Micro Analog Systems Oy	A10X60-77.5K222PY A10X100-77.5K222PY A3.5X4X15-7.87MH A2X3X21-0.92MH A3.75X3.75X23.6-0.92MH	ø 10 x 60 mm ø 10 x 100 mm 3.5 x 4 x 15 mm 2 x 3 x 21 mm 3.75x3.75x23 mm	http://www.mas-oy.com/en/products/radio-controlled-clock-rcc/antennas/
HR Electronic GmbH	60716 (60 kHz) 60708 (77.5 kHz)	ø 10 x 60 mm	http://www.hrelectronic.com/
Hitachi Metals	AN-T702Sxx AN-T702Mxx AN-T702Lxx	19 x 5.5 x 6.3 mm 28 x 5 x 5 mm 50 x 5 x 5 mm	http://www.hitachi-metals.co.jp/e/prod/prod06/p06_12.html
Premo	RCA-SMD-77A (77.5 kHz) RCA-SMD-60A (60 kHz)	75 x 15 x 6.3 mm	http://www.grupopremo.com/
Sumida	ACL80A (40 kHz)	ø 10 x 80 mm	www.sumida.co.jp/jeita/XJA021.pdf

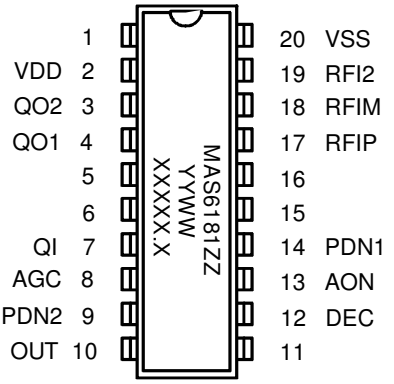
TYPICAL APPLICATION (Continued)

Note 6: Time Signal Software's Pulse Width Recognition Limits
The typical output pulse width specifications are presented in the electrical characteristics section on page 3. Due to process variations the typical output pulse width can differ from these. Additionally the output pulse widths can vary even more depending on the receiving antenna signal strength versus noise and disturbance conditions. That is why it is important that the time signal decoding software has appropriate tolerance limits for managing the output pulse width variations successfully. The table 5 presents recommended software pulse width tolerance limits for recognizing pulses of different time signals.

Table 5. Recommended Software Pulse Width Recognition Limits for Different Time Signals

Parameter	Symbol	Min	Max	Unit
DCF77 Output Pulses	T_{100ms} T_{200ms}	40 140	130 250	ms
MSF Output Pulses	T_{100ms} T_{200ms} T_{300ms} T_{500ms}	50 170 280 400	160 270 380 600	ms
WWVB Output Pulses	T_{200ms} T_{500ms} T_{800ms}	100 400 700	300 600 900	ms
JJY60 Output Pulses	T_{200ms} T_{500ms} T_{800ms}	100 400 700	300 600 900	ms
JJY40 Output Pulses	T_{200ms} T_{500ms} T_{800ms}	100 400 700	300 600 900	ms

MAS6181 SAMPLES IN PDIP-20 PACKAGE



Top Marking Definitions:
YYWW = Year Week
XXXXX.X = Lot Number
ZZ = Sample Version

PIN DESCRIPTION

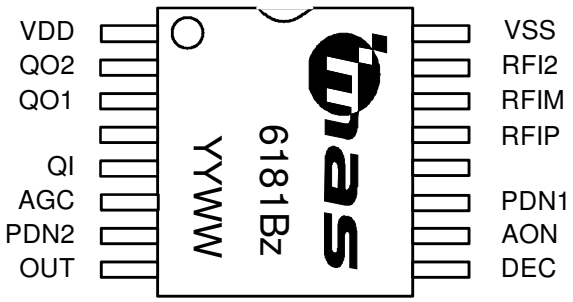
Pin Name	Pin	Type	Function	Note
	1	NC		
VDD	2	P	Positive Power Supply	
QO2	3	AO	Quartz Filter Output for Crystal 2	
QO1	4	AO	Quartz Filter Output for Crystal 1	
	5	NC		1
	6	NC		1
QI	7	AI	Quartz Filter Input for Crystal	
AGC	8	AO	AGC Capacitor	
PDN2	9	DI	Power Down/Frequency Selection Input 2	2
OUT	10	DO	Receiver Output	3
	11	NC		
DEC	12	AO	Demodulator Capacitor	
AON	13	DI	AGC On Control	4
PDN1	14	DI	Power Down/Frequency Selection Input 1	2
	15	NC		
	16	NC		
RFIP	17	AI	Positive Receiver Input	5
RFIM	18	AI	Negative Receiver Input	5
RFI2	19	AI	Receiver Input 2 (for Antenna Capacitor 2)	
VSS	20	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

Notes:

1) Pins 5 and 6 between QO1 and QI must be connected to VSS to eliminate DIL package lead frame parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) PDN1 = VDD and PDN2 = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down controlled to power on
3) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - The output is a current source/sink with $|I_{OUT}| > 5$ µA
   - At power down the output is pulled to VSS (pull down switch)
4) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (normal operation)
   - Unused AON pad can be left unconnected due to internal pull-up with current < 1 µA. Pull up current is switched off at power down.
5) Receiver inputs RFIP and RFIM have both 1.4 MΩ biasing resistors towards VDD

PIN CONFIGURATION & TOP MARKING FOR PLASTIC TSSOP-16 PACKAGE



Top Marking Definitions:
z = Version Number
YYWW = Year Week

PIN DESCRIPTION

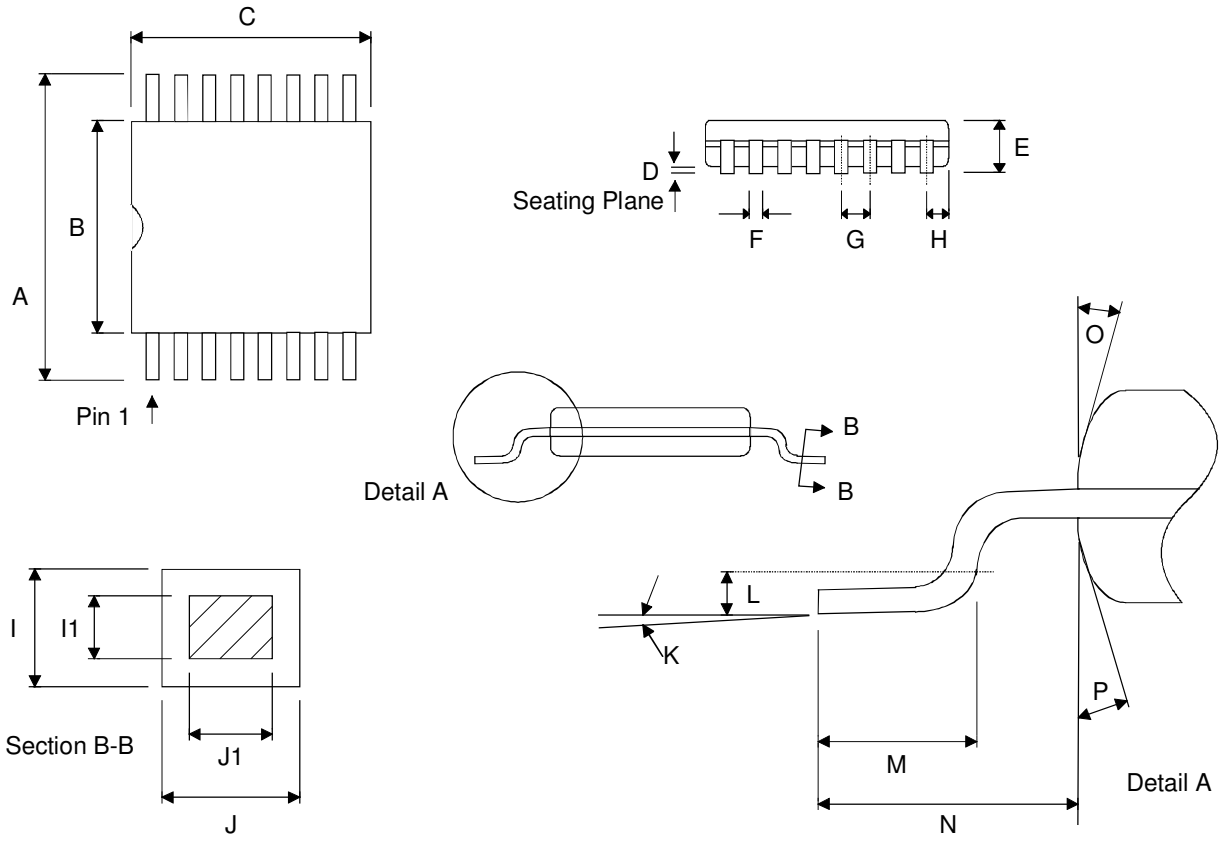
Pin Name	Pin	Type	Function	Note
VDD	1	P	Positive Power Supply	
QO2	2	AO	Quartz Filter Output for Crystal 2	
QO1	3	AO	Quartz Filter Output for Crystal 1	
	4	NC		1
QI	5	AI	Quartz Filter Input for Crystal and External Compensation Capacitor	
AGC	6	AO	AGC Capacitor	
PDN2	7	DI	Power Down/Frequency Selection Input 2	2
OUT	8	DO	Receiver Output	3
DEC	9	AO	Demodulator Capacitor	
AON	10	DI	AGC On Control	4
PDN1	11	DI	Power Down/Frequency Selection Input 1	2
	12	NC		
RFIP	13	AI	Positive Receiver Input	5
RFIM	14	AI	Negative Receiver Input	5
RFI2	15	AI	Receiver Input 2 (for Antenna Capacitor 2)	
VSS	16	G	Power Supply Ground	

A = Analog, D = Digital, P = Power, G = Ground, I = Input, O = Output, NC = Not Connected

Notes:

1) Pin 4 between QO1 and QI must be connected to VSS to eliminate TSSOP package lead frame parasitic capacitances disturbing the crystal filter performance. All other NC (Not Connected) pins are also recommended to be connected to VSS to minimize noise coupling.
2) PDN1 = VDD and PDN2 = VDD means receiver off
   - Fast start-up is triggered when the receiver is after power down controlled to power on
3) OUT = VSS when carrier amplitude at maximum; OUT = VDD when carrier amplitude is reduced (modulated)
   - The output is a current source/sink with $|I_{OUT}| > 5$ µA
   - At power down the output is pulled to VSS (pull down switch)
4) AON = VSS means AGC off (hold current gain level); AON = VDD means AGC on (normal operation)
   - Unused AON pad can be left unconnected due to internal pull-up with current < 1 µA. Pull up current is switched off at power down.
5) Receiver inputs RFIP and RFIM have both 1.4 MΩ biasing resistors towards VDD

PACKAGE (TSSOP-16) OUTLINES



Dimension	Min	Max	Unit
A	6.40 BSC		mm
B	4.30	4.50	mm
C	5.00 BSC		mm
D	0.05	0.15	mm
E		1.10	mm
F	0.19	0.30	mm
G	0.65 BSC		mm
H	0.18	0.28	mm
I	0.09	0.20	mm
I1	0.09	0.16	mm
J	0.19	0.30	mm
J1	0.19	0.25	mm
K	0°	8°	
L	0.24	0.26	mm
M (The length of a terminal for soldering to a substrate)	0.50	0.75	mm
N	1.00 REF		mm
O	12°		
P	12°		

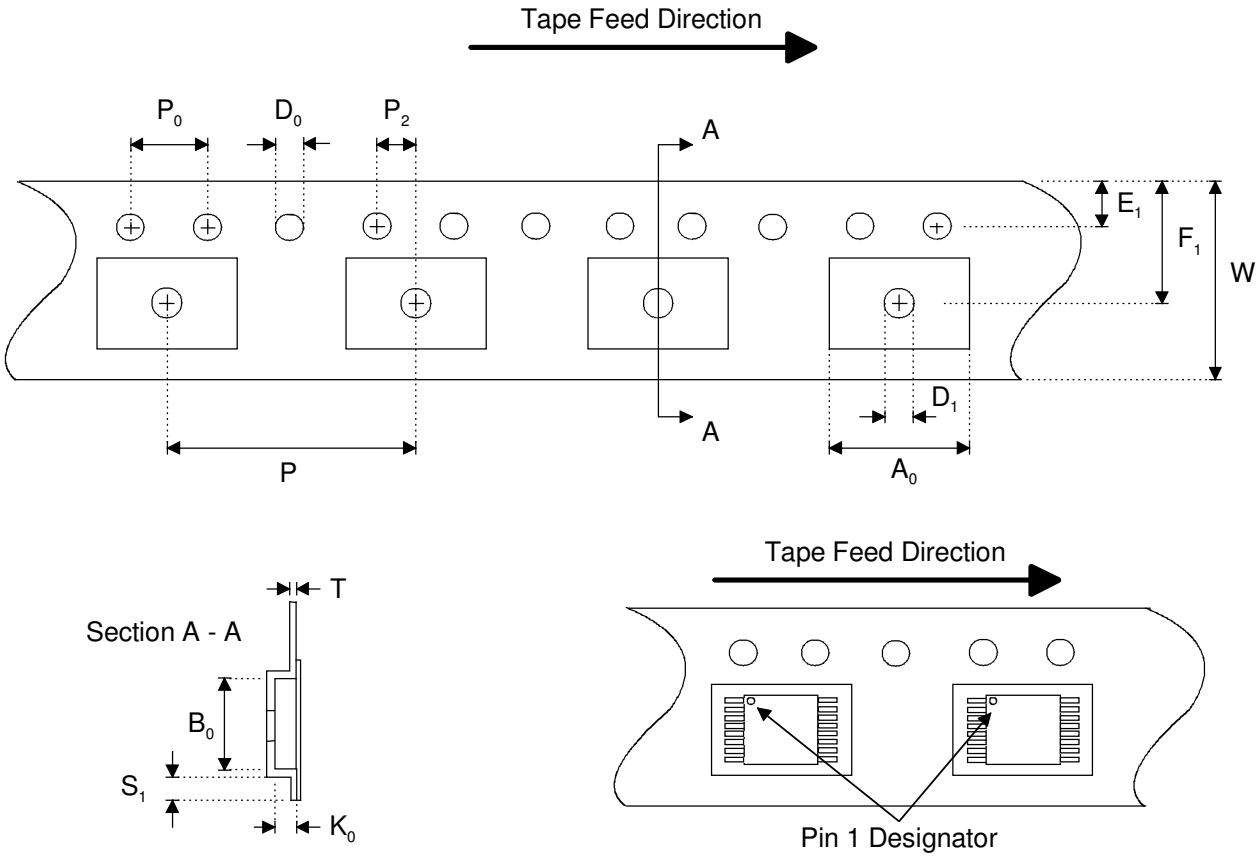
Dimensions do not include mold flash, protrusions, or gate burrs.
All dimensions are in accordance with JEDEC standard MO-153.

SOLDERING INFORMATION

◆ **For Pb-Free, RoHS Compliant TSSOP-16**

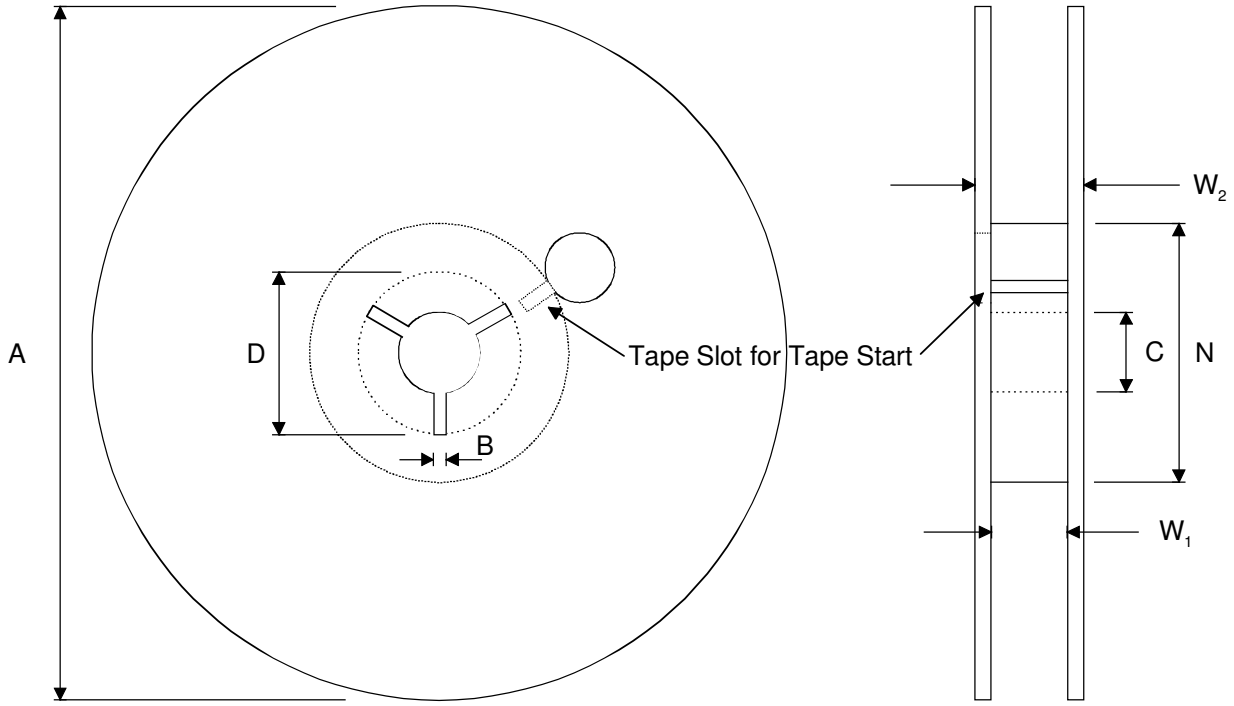
Resistance to Soldering Heat	According to RSH test IEC 68-2-58/20
Maximum Temperature	260°C
Maximum Number of Reflow Cycles	3
Reflow profile	Thermal profile parameters stated in IPC/JEDEC J-STD-020 should not be exceeded. http://www.jedec.org
Seating Plane Co-planarity	max 0.08 mm
Lead Finish	Solder plate 7.62 - 25.4 µm, material Matte Tin

EMBOSSED TAPE SPECIFICATIONS



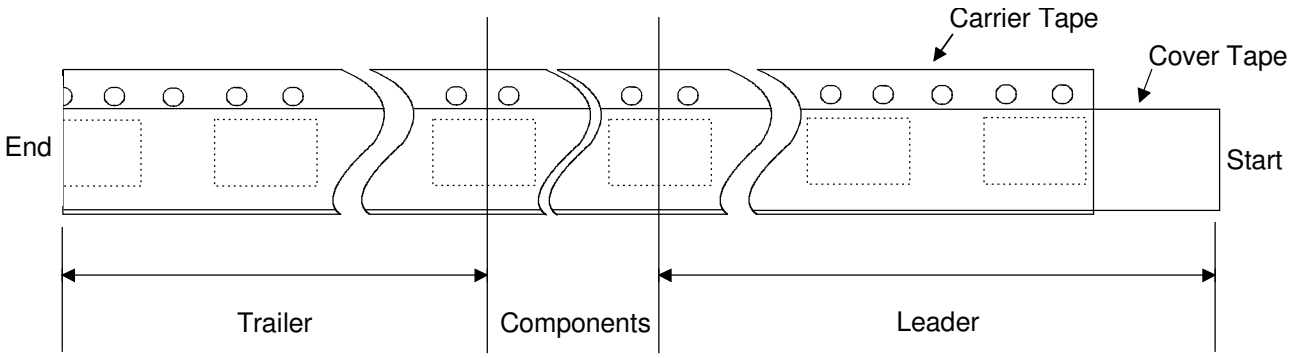
Dimension	Min	Max	Unit
A_0	6.50	6.70	mm
B_0	5.20	5.40	mm
D_0	1.50 +0.10 / -0.00		mm
D_1	1.50		mm
E_1	1.65	1.85	mm
F_1	7.20	7.30	mm
K_0	1.20	1.40	mm
P	11.90	12.10	mm
P_0	4.0		mm
P_2	1.95	2.05	mm
S_1	0.6		mm
T	0.25	0.35	mm
W	11.70	12.30	mm

REEL SPECIFICATIONS



2000 Components on Each Reel

Reel Material: Conductive, Plastic Antistatic or Static Dissipative
Carrier Tape Material: Conductive
Cover Tape Material: Static Dissipative



Dimension	Min	Max	Unit
A		330	mm
B	1.5		mm
C	12.80	13.50	mm
D	20.2		mm
N	50		mm
W_1 (measured at hub)	12.4	14.4	mm
W_2 (measured at hub)		18.4	mm
Trailer	160		mm
Leader	390, of which minimum 160 mm of empty carrier tape sealed with cover tape		mm
Weight		1500	g

ORDERING INFORMATION

Product Code	Product	Description
MAS6181B1TC00	Dual Band AM-Receiver IC with Differential Input	EWS-tested wafer, diameter 8”, thickness 395 µm ± 5%.
MAS6181B1UC06	Dual Band AM-Receiver IC with Differential Input	TSSOP-16, Pb-free, RoHS compliant, Tape & Reel

Contact Micro Analog Systems Oy for other wafer thickness options.

◆ The formation of product code

An example for MAS6181B1TC00:

MAS6181	**B**	**1**	**TC**	**00**
Product name	Design version	Capacitance option: C_C = 0.75 pF	Package type: TC = 400 µm thick EWS tested wafer	Delivery format: 00 = undiced wafer 05 = dies on tray 06 = tape & reel 08 = in tube

LOCAL DISTRIBUTOR

MICRO ANALOG SYSTEMS OY CONTACTS

Micro Analog Systems Oy Kutomotie 16 FI-00380 Helsinki, FINLAND	Tel. Int. +358 10 835 1100 Telefax +358 10 835 1119 http://www.mas-oy.com